

1722A/1752A

INSTRUMENT CONTROLLER

1711A/AA Communication/Measurement System (See Section 10)
1722A/AP Instrument Controller (See Section 11)

Service Manual

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PN 732156 SEPTEMBER 1984, REV. 2. 3/92
PN 759050 (Text Only)
PN 909932 (Service Manual and OEM Manual)
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1722A/1752A Instrument Controller

Section 1

Introduction

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1-1. THE 1722A INSTRUMENT CONTROLLER

The 1722A Instrument Controller is a microcomputer used to control other instruments and test equipment. The 1722A can be controlled by either a Touch-Sensitive Overlay or a removable keyboard that connects at the front panel with a DIN plug. Specifications for the 1722A are presented in Table 1-1. See the 1722A System Guide for a detailed discussion of the 1722A's capabilities and operation.

1-2. THE 1752A DATA ACQUISITION SYSTEM

The Fluke 1752A Data Acquisition System is a microcomputer-based system for use in analog and digital measurement and control applications. The 1752A, like the Fluke 1722A, also functions as a powerful instrument controller designed to support IEEE-488 instrumentation systems.

The standard 1752A comes with one 1752A-010 Analog Measurement Processor. Through the use of additional optional plug-in modules, the system can measure or output dc currents and voltages, measure time and frequency of analog and TTL signals, count events with a bi-directional totalizer, and interface with digital signals.

The 1752A also features a touch-sensitive display, which can replace the keyboard for command entry. Specifications for the 1752A are presented in Table 1-1. Information and specifications for the 1752A options are available in Section 6 of this manual and in the 1752A Data Acquisition and Control manual. For a detailed discussion of 1752A operation and capabilities, see the 1752A System Guide.

NOTE

In most respects, the 1752A hardware does not differ from the 1722A hardware. In this manual, the 1752A is treated as a superset of the 1722A. Except where noted, all references to the 1722A also apply to the 1752A.

1-3. PHYSICAL LAYOUT

The 1722A consists of seven modules mounted on a common chassis which also accepts a number of optional modules. The seven modules are:

- Single-Board Computer (SBC)
- Video/Graphics/Keyboard Interface (VGK)
- Programmer's Keyboard
- Power-Up Assembly (PUP)
- Power Supply (Original Equipment Manufacture)
- Video Monitor (Original Equipment Manufacture)
- Floppy Disk Drive (Original Equipment Manufacture)

The modules and options (if any) are connected by the motherboard and interconnecting cables within the chassis. The Touch-Sensitive Overlay is installed over the face of the CRT.

An optional carrying strap is mounted on the left side. Four feet are mounted on the bottom cover. The two feet at the front are adjustable for easy viewing, and the two at the back are fixed.

1-4. POWER REQUIREMENTS

The 1722A operates on 230V ac or 115V ac, either 50 Hz or 60 Hz depending on customer specification. However, internal adjustments must be made to change the line voltage requirement. (See Access Procedures in Section 3.)

Table 1-1. Specifications

CRT DISPLAY

Scanning Method	Non-interlaced raster scan.
Refresh Rate	50 to 60 Hz, selectable.
Character Memory	1280 bytes of dedicated display memory. 16 lines of 80 characters.
CRT Screen	High-contrast green phosphor, low profile, rectangular. 8.6 cm x 20.3 cm (3.4 in x 8.0 in).
Character Capacity	16 x 80 cells, or 8 x 40 cells.
Standard Character Set	96 standard ASCII characters, graphics characters, match, and other useful symbols.
Character Cell	7 x 9 dots in an 8 x 14 dot matrix.

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Table 1-1. Specifications (cont)

Character Enhancements	Reverse video, blinking, underlining, and highlighting.
Cursor	Blinking, underline, block, or suppressed.
Raster Size	7.6 cm x 19 cm (3.0 x 7.5 in).
Graphics Screen Capacity	640 x 224 pixels
Graphics Memory Capacity	64K bytes (2048 x 256 pixels). Independent of main memory.
Display Alignment	Character with respect to touch-sensitive grid at 25°C after 30 minute warmup: ±1.5 character horizontal ±0.5 character vertical Change in character positions over the operating temperature range: 1 character horizontal 0.5 character vertical

DISK DRIVE

R/W Heads	2 per disk drive
Tracks	80 (40 per side)
Track Density	48 tracks per inch
Rotational Speed	300 RPM
Disk Error Rates	
RECOVERABLE	1 per 10 ⁹ bits read
NON-RECOVERABLE	1 per 10 ¹² bits read
Recording Format	
BYTES PER SECTOR	512
SECTORS PER TRACK	10
ENCODING METHOD	MFM (double density)
Total Formatted Storage	409,600 bytes per disk

ENVIRONMENTAL

Operating

WITH DISK MEDIA	10°C to 40°C (50°F to 104°F) 20% to 80% RH humidity (non-condensing)
WITHOUT DISK MEDIA	10°C to 40°C (50°F to 104°F) 5% to 90% RH humidity (non-condensing)

Storage

WITH DISK MEDIA	10°C to 52°C (50°F to 126°F)
	8% to 80% humidity (non-condensing)
WITH INTERNAL HARD DRIVE	-40°C to 60°C (-40°F to 140°F)
	8% to 80% humidity (non-condensing)
WITHOUT DISK MEDIA	-40°C to 60°C (-40°F to 140°F)
OR INTERNAL HARD DRIVE	5% to 90% humidity (non-condensing)

EMI and RFI Emissions.....Tested to FCC Part 15, Subpart J, Class B; VDE 0871, Class B; CISPR 11-1975

Shock and Vibration

WITHOUT INTERNAL HARD DRIVE

Shock (Non-Operating) As per MIL-T-28800, Class 5: 1/2 sineshock of 20G, 11 ms duration.
Vibration (Operating, As per MIL-T-28800, Class 5: 5-55 Hz;
not accessing floppy disk) 0.13" displacement; peak acceleration @55 Hz of 2.0G.

WITH INTERNAL HARD DRIVE

Shock (Non-Operating) As per MIL-T-28800, Class 5: 1/2 sine shock of 20G, 11 ms duration.

Vibration (Non-Operating) 5 to 17 Hz: 0.020" (double amplitude); 18 to 500 Hz: 4.0G peak acceleration @500 Hz of 4.0G.

Vibration (Operating) 5 to 22 Hz: 0.010" (double amplitude); 23 to 500 Hz: 0.15Gs (without non-recoverable errors).

Table 1-1. Specifications (cont)

GENERAL

Dimensions 13 cm H x 43 cm W x 55 cm L (plus feet) (5.228 in H x 17.0 in W x 21.6 in L).
See Figure 1-1.

Weight

CONTROLLER 15.5 kg (34 lbs)

KEYBOARD 1.4 kg (3 lbs)

Power 175W max.

VOLTAGE 90-132 ac, 47-63 Hz (use 3A time delay slow blow 250V fuse.)


180-264 ac, 47-63 Hz (use 2A time delay slow blow 250V fuse.)

POWER DISSIPATION 175W max.

DC TOLERANCE $\pm 5\%$

NOTE: Specifications for the Analog Measurement Processor (Option 1752A-010) are located in Section 6. The Analog Measurement Processor is standard equipment with the 1752A.

NOTES:

1.  THESE HOLES USED FOR MOUNTING OF FEET. CAN BE USED FOR NON-STRUCTURAL INSTRUMENT MOUNTING.
2. ALLOW 4-INCHES MINIMUM AT REAR AND CRT SIDE OF INSTRUMENT FOR AIRFLOW.

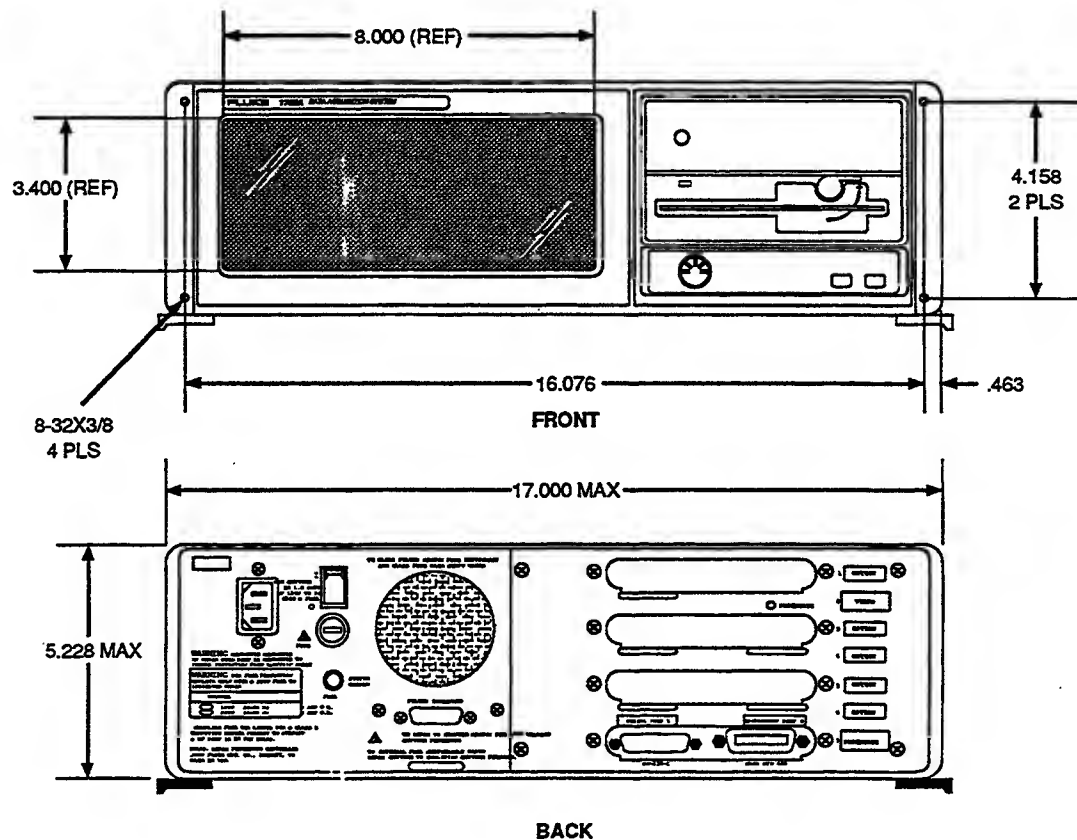
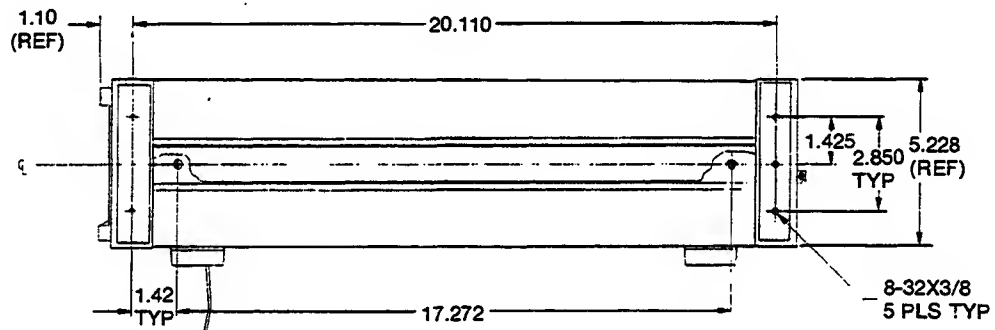
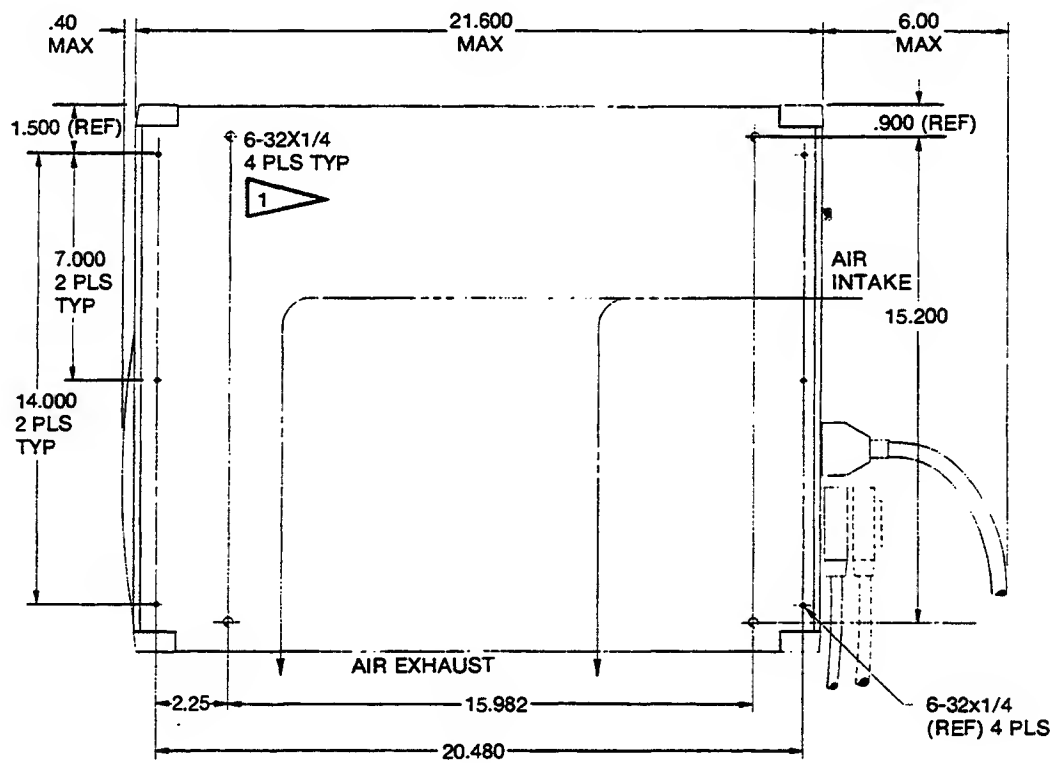


Figure 1-1. Dimensions

INTRODUCTION



SIDE



BOTTOM

Figure 1-1. Dimensions (cont)

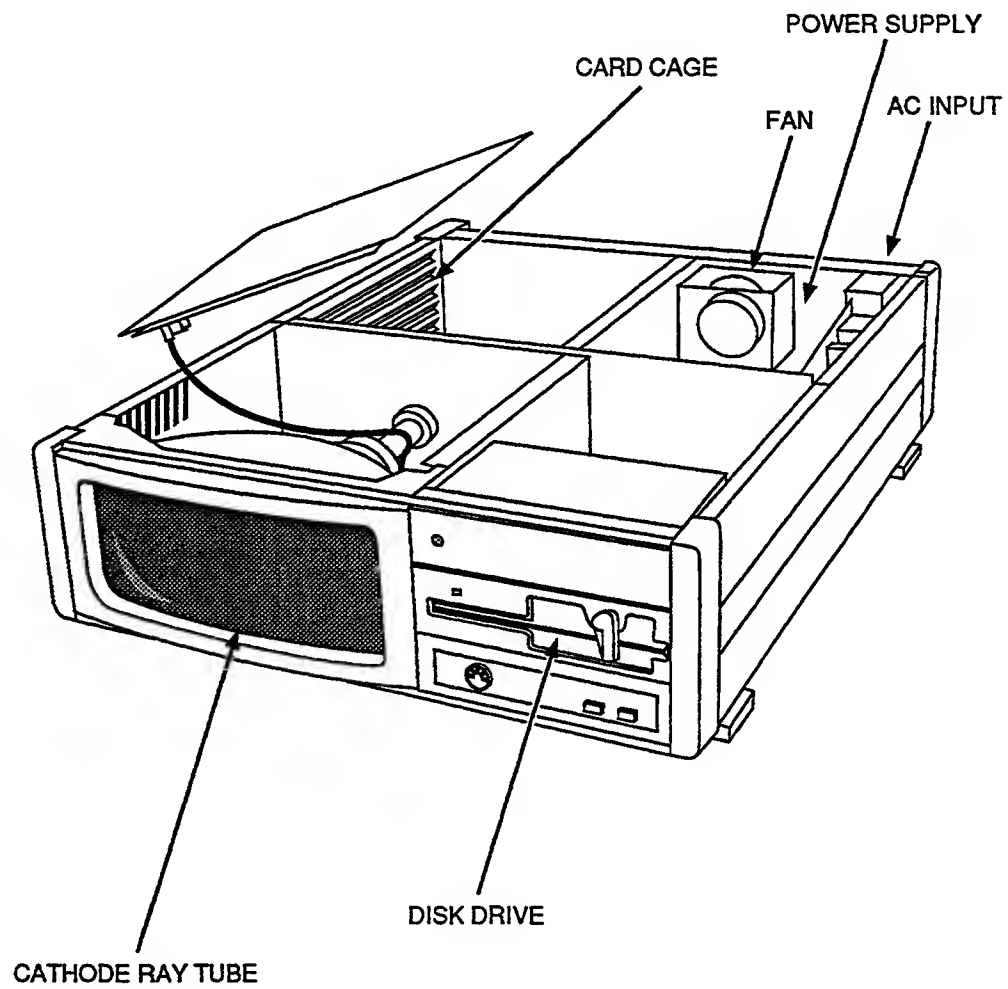
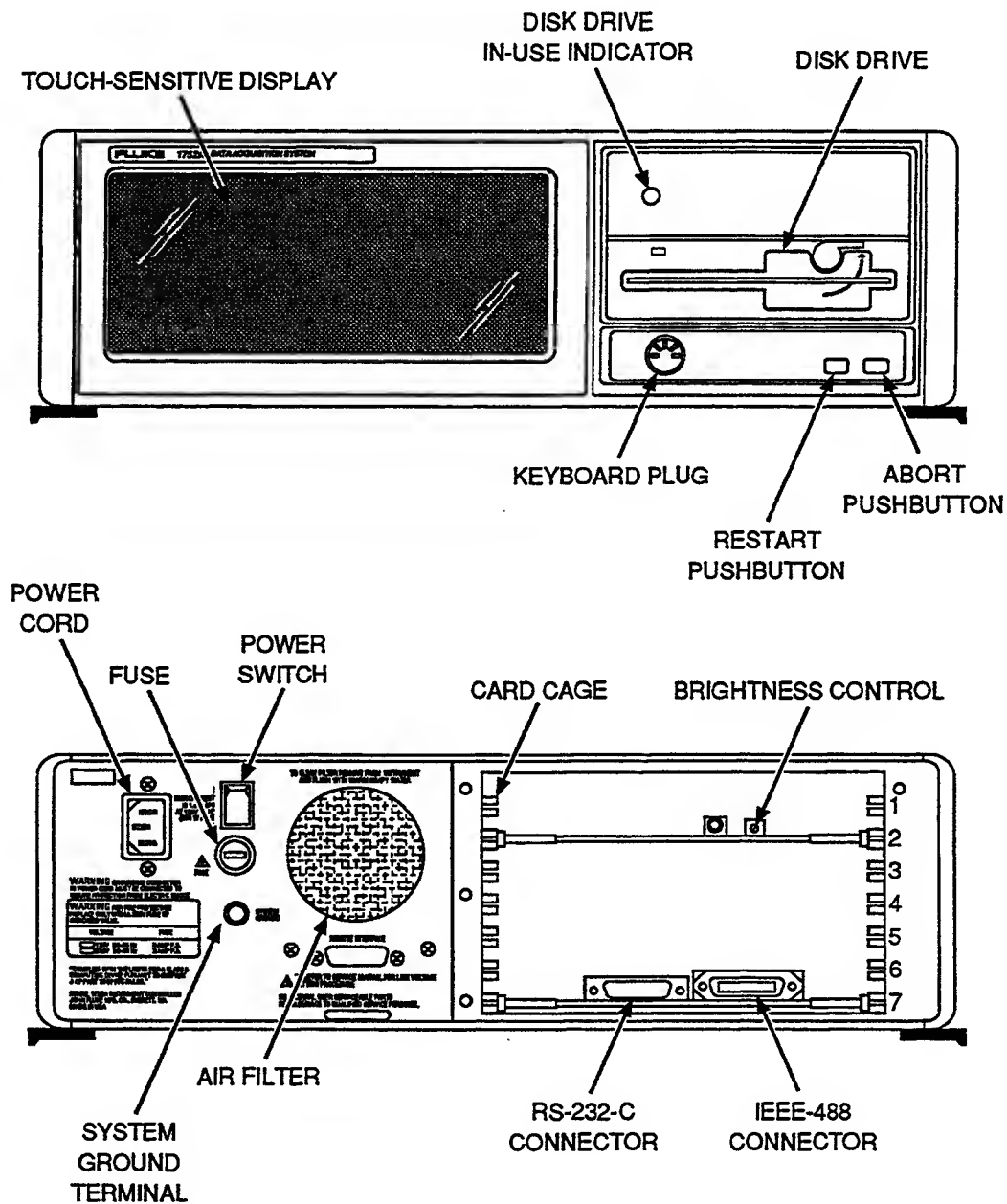


Figure 1-2. Physical Layout

INTRODUCTION



Slots	1722A	1752A
Single Board Computer	7	Same
Video/Graphics Keyboard Interface	2	Same
RAM Expansion Option	1,3,4,5,6	Same
Bubble Memory Option	1,3,4,5,6	Same
Parallel Interface Option	1,3,4,5	Same
Dual Serial Interface Option	1,3,4,5	Same
IEEE-488/RS-232-C Interface Option	4,5	Same
Analog Measurement Processor		1,3,4,5
Analog Output		1,4,5
Counter/Totalizer		4,5
Mainframe Interface Assembly		1,3,4,5

Figure 1-2. Physical Layout (cont)

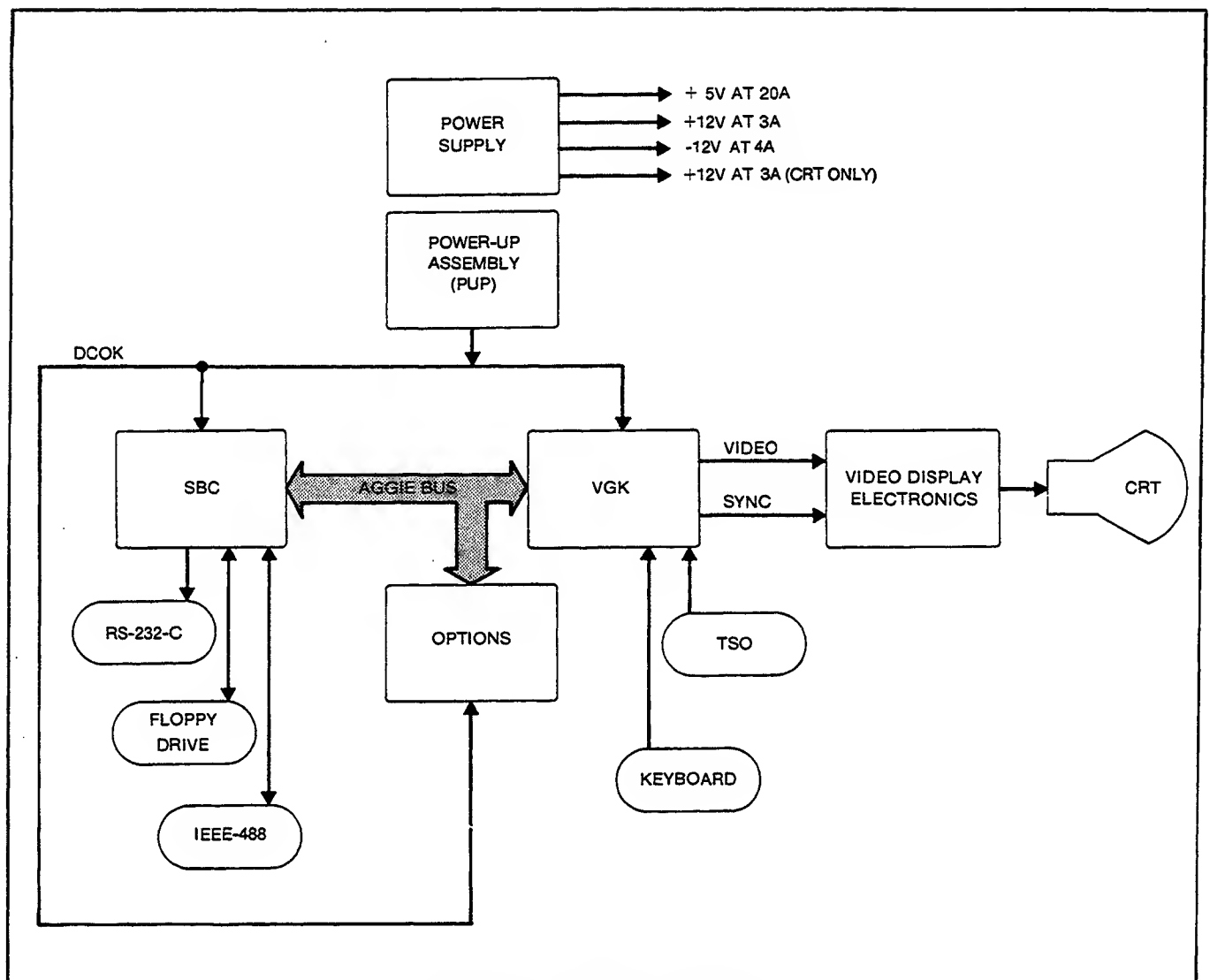


Figure 1-3. Overall Block Diagram

Section 2

Theory of Operation

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2-1. INTRODUCTION

2-2. Bus Architecture

Compatibility with other Fluke products and the demands of the Texas Instruments TMS99105 Microprocessor require a complex system bus structure that addresses not only devices requiring 18 address lines but those requiring 22 address lines as well. This bus, which is really two buses sharing address lines, is referred to as both the ARGUS bus and the AGGIE bus. The ARGUS bus consists of 18 address lines and two control lines. The AGGIE bus, a superset of the ARGUS bus, consists of 22 address lines and two control lines. All of the address lines available to the ARGUS bus are also available to the AGGIE bus in addition to four address lines available only to the AGGIE bus.

When the Microprocessor wishes to address a device on the ARGUS bus, it sends out an address on 18 lines of the bus and also sends out a signal named ADVAL- to indicate that a memory or I/O cycle is taking place on the ARGUS bus. The selected device must respond with a signal known as ADACK-.

When the Microprocessor wishes to address devices on the AGGIE bus, it sends out a signal known as AGVAL- along with the address. Here again, the selected device must respond with ADACK-. In this case, the Microprocessor uses all 22 address lines.

2-3. Description of Distinctive Devices

2-4. TMS99105 16-BIT MICROPROCESSOR

The Single-Board Computer (SBC) uses a Texas Instruments TMS99105 Microprocessor. The distinguishing features of the Microprocessor are:

- Multiplexed Address and Data Buses
- Bit or Byte Addressing Capability
- Communications Register Unit (CRU) I/O Addresses
- Off-Chip Workspace Located in RAM.
- Macrostore Memory Space
- 16 Interrupt Priority Levels

2-5. Memory Space Addressing

The Microprocessor's instruction set uses a 16-bit byte-address to address memory as 16-bit words or 8-bit bytes. The Microprocessor chip, however, addresses memory as 16-bit words only. It can address 32768 words of memory using a 15-bit address. When an instruction operates on a

byte of data, the Microprocessor addresses the whole word in which the byte is contained.

2-6. Memory Mapping

It is possible to address more than 32K words of memory by using an external memory mapper to increase the number of address bits. The Microprocessor has features that support memory mapping. Status bit 8 (ST8) of the Microprocessor's status register is called the Map-Select-Status Bit (M). This bit is used to enable or disable an external memory mapper. The code and data for application programs is placed in the memory space accessed through the memory mapper.

2-7. CRU I/O Space

The TMS 99105A can do bit- or word-oriented I/O using CRU (Communications Register Unit) I/O instructions. The CRU I/O instructions can address 32768 I/O locations. The lower 16384 locations are used for bit-oriented I/O and the upper 16384 are used for word-oriented I/O. An I/O operation which takes place in the lower 16384 I/O locations is called a serial CRU I/O operation. An I/O operation that takes place in the upper 16384 I/O locations is called a parallel CRU I/O operation. The most-significant bit (MSB) of the I/O address selects which type of operation will occur.

Although 16 locations are needed for each word in the serial CRU I/O space, only one location is needed for each word in the parallel CRU I/O space. Thus, the serial CRU I/O space may have up to 1024 16-bit registers, and the parallel CRU I/O space may have up to 16384 16-bit registers.

When a CRU instruction reads a word from an address in the lower half of the I/O space, the bits of the word are read one at a time from 16 addresses until the 16 bits of the word have been read. When a CRU instruction reads a word from an address in the upper half of the I/O space, the bits are read in parallel from one address.

2-8. Macrostore Memory

The architecture of the TMS99105A defines a memory space called Macrostore that allows new instructions to be added to the Microprocessor's instruction set. This memory space is addressed as 4096 word locations and is separate from the Microprocessor's normal memory space. A typical application for Macrostore is to define a set of floating-point arithmetic functions for use by higher level languages.

2-9. Interrupts

The TMS99105A has 16 interrupt levels. These levels are arranged so that a lower level interrupt service routine may not interrupt a higher level routine. When an

interrupt request occurs, the Microprocessor branches through an interrupt table to the interrupt-service routine for the level making the request. Since a Memory Mapper is used, the interrupt table is stored in lower memory so that it can be addressed with the mapper disabled.

2-10. PROGRAMMABLE ARRAY LOGIC DEVICES (PALs)

A PAL is a fuse-programmed device that replaces discrete logic devices such as AND gates, OR gates, flip flops, and counters. A single 20-pin PAL can replace from 4 to 12 TTL logic packages. PALs are used in the SBC to reduce the number of chips on the pcb.

PALs can be thought of as a collection of AND gates, OR gates, flip-flops, and inverters that haven't been connected together. The connections are made by programming the device.

There are two types of PALs: combinational and registered. Combinational PALs are used to replace combinational logic like AND, OR, NAND, NOR gates and inverters. They are generally used for applications such as address decoders and control logic.

Registered PALs are often used to generate the timing signals required to interface a device to a microprocessor. Their AND/OR array is similar to combinational PALs, but the array's outputs connect to D-type flip-flops. The outputs of the D-type flip-flops connect to the PAL's output pins and are inputs to the AND/OR array, making it possible to replace sequential logic such as counters, shift registers, flip-flops, and state machines with PALs.

2-11. DYNAMIC MEMORY

The dynamic RAM chip stores data bits as charges on capacitors in the chip. The charges will leak off the capacitors with time and must be restored periodically to preserve the data. This restoration is called refreshing the RAM. Each RAM chip automatically refreshes 256 bits of the memory when RAS- (Row Address Select) is pulsed low. To completely refresh the RAM, RAS- must be pulsed low with 256 different address inputs. This refreshes the RAM because each address input refreshes 256 different bits. Thus, all locations are refreshed ($256 \times 256 = 65536$). The RAM must be completely refreshed every 4 ms so that the RAM does not lose any data. This means that RAS- must occur for 256 different address inputs within 4 ms, or once every 15.6 μ s.

2-12. MEMORY MAPPER

Memory mapping is a technique that increases the amount of memory a microprocessor can address. A typical microprocessor has only 16 address lines, which can address a maximum of 64K bytes. The SBC, however,

provides for a memory space of 4M bytes, requiring 22 address lines. Since the Microprocessor can directly address only 65,536 bytes of memory, a SN74LS612 memory mapper chip (U73) is used to allow the Microprocessor to address the larger memory space. The memory mapper is programmed by the software to select which 64K-byte part of the 4M-byte address space the Microprocessor addresses.

The 4M-byte address space is called the physical-address space. The amount of memory the Microprocessor can directly address is called the logical-address space. When the mapper is disabled, the Microprocessor always addresses the lowest 64 kilobytes of the physical-address space. When the mapper is enabled, the Microprocessor can address any 64K-byte part of the physical-address space.

The address space is divided into "pages" and does not need to be contiguous or in sequence. The logical-address space is divided into 16 pages, and the physical-address space is divided into 1024 pages. Each page is 4096 bytes long. The Microprocessor may address any 16 of the 1024 physical-memory pages at any given time. The 1722A system software reloads the mapper with new page addresses to select another part of the physical-address space.

2-13. Introduction to 1722A Modules

2-14. POWER-UP MODULE (PUP)

The Power-Up Assembly performs the following functions:

- Senses the ABORT and RESTART buttons on the front panel
- Monitors the power supply voltages
- Distributes power to the fan
- Resets devices connected to the DCOK (system reset) line

2-15. SINGLE-BOARD COMPUTER (SBC)

The SBC is the central microprocessor and control unit for the 1722A. It is, as the name implies, a complete computer on a single board. It contains the TMS99105 Microprocessor, its support logic, RAM, ROM, serial and parallel I/O and all other devices found on any microcomputer.

The architecture of the SBC and the entire 1722A is tied closely to the demands of the TMS99105 design. The TMS99105 is an outgrowth of the TI 9900-Series Microprocessor. Unlike its predecessor it uses a multiplexed address and data bus. But like the 9900 Series, it uses off-chip memory for its workspace. And like the 9900, the 99105 uses an unusual I/O logic.

Not only does the 99105 address I/O devices as memory locations, but it also addresses a separate field known as a Communications Register Unit (CRU). The CRU is a third use of the ARGUS/AGGIE system bus. It utilizes the lowest 12 address lines in conjunction with three control signals, CRUIN, CRUOUT, and CRUCLK. The CRU space can be addressed either as individual bits or as words up to 16 bits wide. From the point of view of the TMS99105, other modules exist as addresses within this CRU space. When the TMS99105 talks to other modules, the data transmitted must occur serially over the CRUIN or CRUOUT lines. Data does not appear on the multiplexed bus and is not loaded into off-chip data registers during a CRU I/O cycle.

2-16. VIDEO/GRAPHICS/KEYBOARD INTERFACE (VGK)

The VGK is the interface between the SBC (Single-Board Computer) and the operator. It controls the video display, the TSO (Touch-Sensitive Overlay), and the programmer's keyboard. In addition to the 16 lines of 80 characters, the VGK also displays a graphic image with 224 rows of 640 dots.

User software, running on the SBC, sends characters and graphics commands to the VGK that specify the image on the screen. The VGK sends character codes to the SBC when the operator pushes keys on the keyboard or touches the TSO. The application software must receive and interpret these data.

2-17. KEYBOARD

The keyboard is a detachable unit that connects at the front panel with a DIN plug. Data transmission between the keyboard and the VGK uses the serial format used with RS-232-C compatible equipment (format not defined by the RS-232-C specification). The keyboard is a microcomputer-based device that uses the Intel 8748 Microcomputer and communicates with a UART in the VGK's CRU space. The keyboard executes a loop routine that scans the keyboard for key closures. When the keyboard Microprocessor finds a closed key, it sends a serial byte to the UART on the VGK board, which in turn generates the interrupt for the VGK Microprocessor.

2-18. POWER SUPPLY (OEM)

Schematics and parts lists for the Power Supply are provided in Section 9. The Power Supply regulates and supplies the following voltages to circuitry in the 1722A:

- +12.1V dc ($\pm 2.5\%$)
- -12.1V dc ($\pm 2.5\%$)
- +5.1V dc ($\pm 2\%$)

2-19. VIDEO MONITOR (OEM)

Detailed information is located in the OEM manual provided in Section 9.

2-20. FLOPPY DISK DRIVE (OEM)

Detailed information is located in the OEM manual provided in Section 9.

2-21. POWER-UP ASSEMBLY (PUP) THEORY OF OPERATION

The Power-Up Assembly performs the following:

- Controls power-up reset
- Controls ABORT and RESTART functions
- Monitors the power supply voltages
- Distributes power to the fan

2-22. Functional Description

The PUP controls the system reset functions during power-up, normal operation, and power-down.

On power-up, the PUP keeps the system in a reset state until the power supply voltages are above minimum limits. After the voltages are stable, the reset is released and the SBC Microprocessor begins executing the "boot" program that resides in EPROM. The boot sequence initializes the system hardware, invokes a system self-test, and loads the operating system into main memory from floppy disk.

During normal operation, pressing and releasing the RESTART and ABORT buttons together is equivalent to turning the power off and on. Since the self-test writes a pattern to main memory, user programs will be corrupted and e-disk configuration will be lost. Pushing both buttons is referred to as a "cold boot".

Pressing RESTART alone causes a non-maskable interrupt on the SBC, which directs the microprocessor to execute the boot program without the self-test. The system software is loaded into main memory without disturbing the contents of memory and e-disk. This is called a "warm boot".

Pressing ABORT alone causes a Level-2 interrupt on the SBC and has the same effect as typing a ^C (Control C) on the programmer's keyboard when expected by a program written in a high-level language.

At power-down, the system is reset as soon as the power supply voltages fall below minimum limits.

2-23. Circuit Description

The states of the front panel push buttons and the power supply voltage levels determine the state of the following control lines on the system bus:

- DCOK
- ABORT-
- WBOOT-

The ABORT- and WBOOT- outputs are controlled by an RS flip-flop (U1A and U1D), and the ABORT and RESTART push buttons. If either ABORT or RESTART or neither is pressed, the flip-flop remains in a reset state, and each output is controlled by its respective switch. Each switch is a normally open, momentary, single-pole switch, with one side connected to logic common. The other side of the switch is pulled up by a 10 k Ω resistor and filtered by a 0.22 μ F capacitor. The contact closures are debounced by the RC time constant and U3, which has a Schmitt trigger input.

The supply voltages are monitored by two comparators that compare the supply voltages with reference voltages. The reference voltages are supplied by a 6.2V zener diode (VR1) and a current-limiting resistor (R1).

The +12V dc supply is halved by voltage divider Z1 and Z3 and is filtered by C1. This halved supply voltage is compared by part of U2 with the 5.4V dc reference voltage (half of the 10.8V trip voltage). The 5.4V dc reference is derived from zener (Z1) by R4 and Z3. Resistors R2, R3, and R7 provide hysteresis protection from noise.

The +5V power supply is filtered by Z1 and C2 and is compared by part of U2 with the 4.75V reference derived from zener VR1 by R5 and Z3. The outputs of both comparators are wired-OR and are high when the supply voltages are above the trip points.

2-24. Circuit Operation

On power-up, current flows from +5V through a 1 k Ω resistor (Z1 pins 7 and 8) into the base of Q1, which clamps DCOK low. When the supply voltages are above their respective thresholds, the open collector outputs of U2A and U2B turn off and allow C5 to charge through R8. The output of U2C goes low 200 ms later when C5 has charged to the 1V threshold. The output of U4B is turned off and C10 charges through Z2-4. When the voltage on C10 reaches 3.1V, 50 ms later, the output of U2D turns on and turns Q1 off. The DCOK line is then pulled high by Z2-2.

On power-down, the comparators rapidly discharge C5 and C10 and allow Q1 to clamp DCOK low, resetting the system hardware.

When the ABORT and RESTART buttons are pushed together, the flip-flop formed by U1A and U1D is set by U3B, disabling the ABORT- and WBOOT- outputs and forcing the DCOK output low through U4B, U2D, and Q1. When both buttons are released, U4A resets the flip-flop and DCOK returns high.

When the ABORT button is pushed, the ABORT- output goes low. The ABORT signal is buffered and inverted by U3D, enabled through U1C by the flip-flop formed by U1A and U1D, inverted again by U3C, and changed to an open collector output by U4C.

When the RESTART button is pushed, the WBOOT- output goes low. The RESTART signal is buffered and inverted by U3A, enabled through U1B by U1A and U1D, and is presented to the bus as a TTL signal.

2-25. SINGLE-BOARD COMPUTER THEORY OF OPERATION

2-26. Introduction

The Single-Board Computer(SBC) is a multi-layer circuit card which contains all the components necessary to the operation of a microcomputer, including a floppy disk drive interface, serial and parallel I/O and a system bus interface. The SBC mounts in the card cage of the 1722A. It has one 72-contact card-edge connector, one 44-contact card-edge connector, an external RS-232-C connector, and an external IEEE-488 connector. A simplified block diagram of the SBC is shown in Figure 2-1.

The SBC is based on the TI99105A 16-bit Microprocessor that by itself can address 32K 16-bit word locations in memory using a multiplexed address/data bus. However, through a memory mapping scheme, the SBC has a memory capacity of 3M bytes when loaded with all its memory boards. I/O operations are managed with the aid of an I/O address decoder that selects memory and peripheral devices. Peripherals are accessed through IEEE-488 and RS-232-C ports. Other sections of the 1722A controller are accessed using the ARGUS/AGGIE bus. The memory consists of BOOT EPROM, Macrostore RAM, Dynamic RAM on the SBC, and additional memories provided as options on separate boards. PALs (Programmable Array Logic devices) are used extensively in place of discrete logic chips to reduce the number of components.

2-27. Functional Description of SBC Operation

For the following discussion, refer to the detailed block diagram in Figure 2-2.

2-28. BUS STRUCTURE

NOTE

Texas Instruments reverses the order in which the address and data bits are labeled. Thus, data bit D0 is the most significant data bit, and D15 is the least significant. Keep this in mind as you examine the schematics for the SBC.

The 1722A uses two buses: the ARGUS bus and the AGGIE bus. The ARGUS bus is a memory and I/O bus used in the 1720A, 1722A, and other products. The AGGIE bus was developed for the 1722A, incorporating the original ARGUS bus but adding four address lines and some additional control lines. The new address lines allow the AGGIE bus to address up to 1.5M words of memory. Both buses occupy the same physical space; the AGGIE bus is a superset of the ARGUS bus.

The ARGUS bus design is closely tied to the architecture of the TMS9900 Microprocessor. It uses a 16-bit parallel-data bus for memory and parallel I/O. Memory and

parallel I/O are addressed using a 17-bit word address; thus, 128K words of memory or parallel I/O can be addressed on the ARGUS bus.

The ARGUS bus can address bit-oriented I/O up to 4K bits. I/O on the ARGUS bus is usually called CRU I/O. The CRU I/O bus and parallel memory bus share the same address bus, with the CRU I/O bus using the 12 least-significant bits of the address bus.

The AGGIE bus is a superset of the ARGUS bus, and was designed to increase the memory address space and bus speed for the SBC. All of the signals available on the ARGUS bus are also available on the AGGIE bus, allowing the use of existing ARGUS-bus cards on the AGGIE bus. The four new address lines and the control signals are used by AGGIE-bus memory cards but are not used by any existing or future ARGUS-bus cards.

The SBC Microprocessor (U75) uses a multiplexed address and data bus that is applied to the inputs of the Address Latch (U78 and U84) and Data Buffer (U76 and U85).

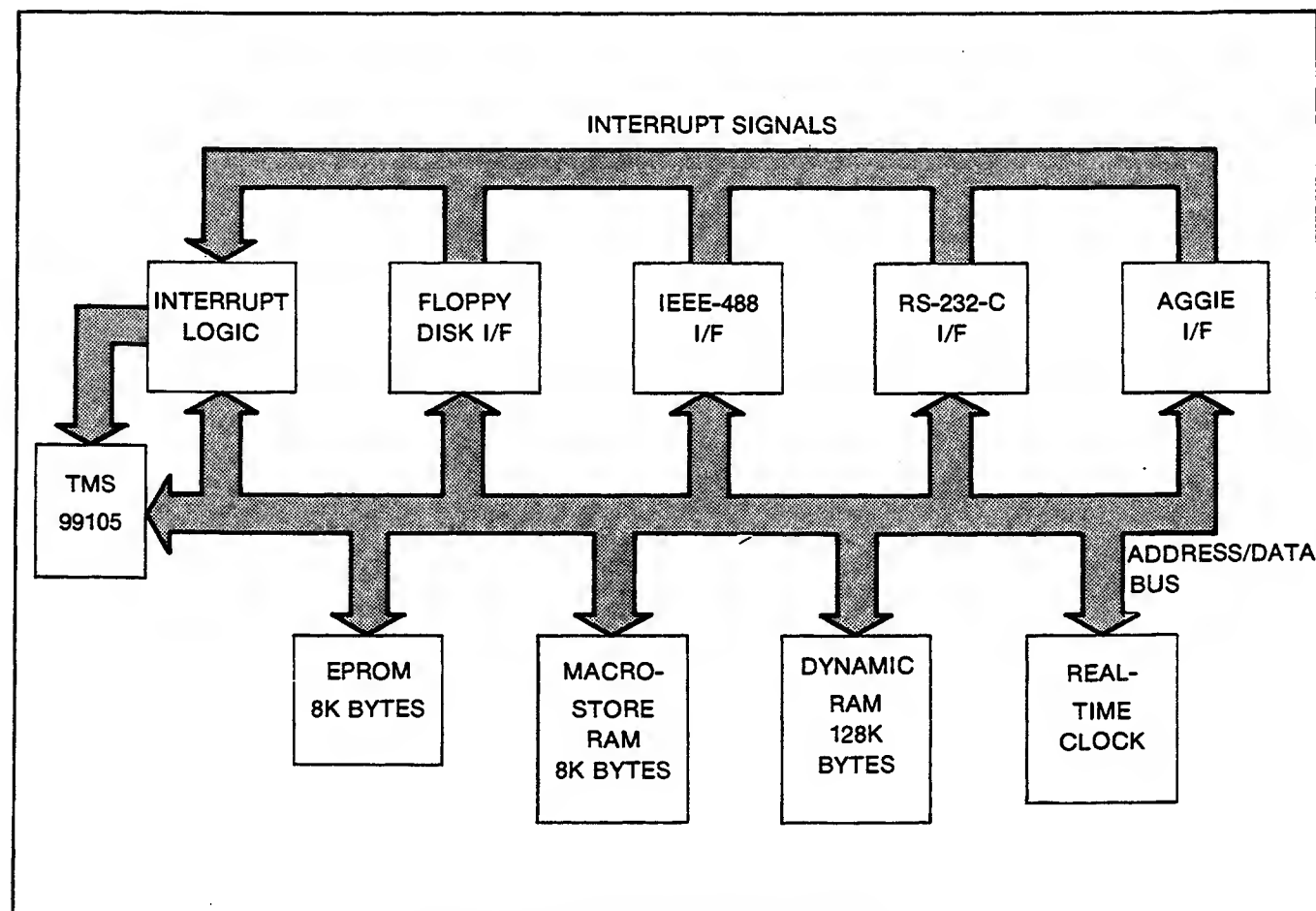


Figure 2-1. Simplified SBC Block Diagram

THEORY OF OPERATION
SINGLE-BOARD COMPUTER(SBC)

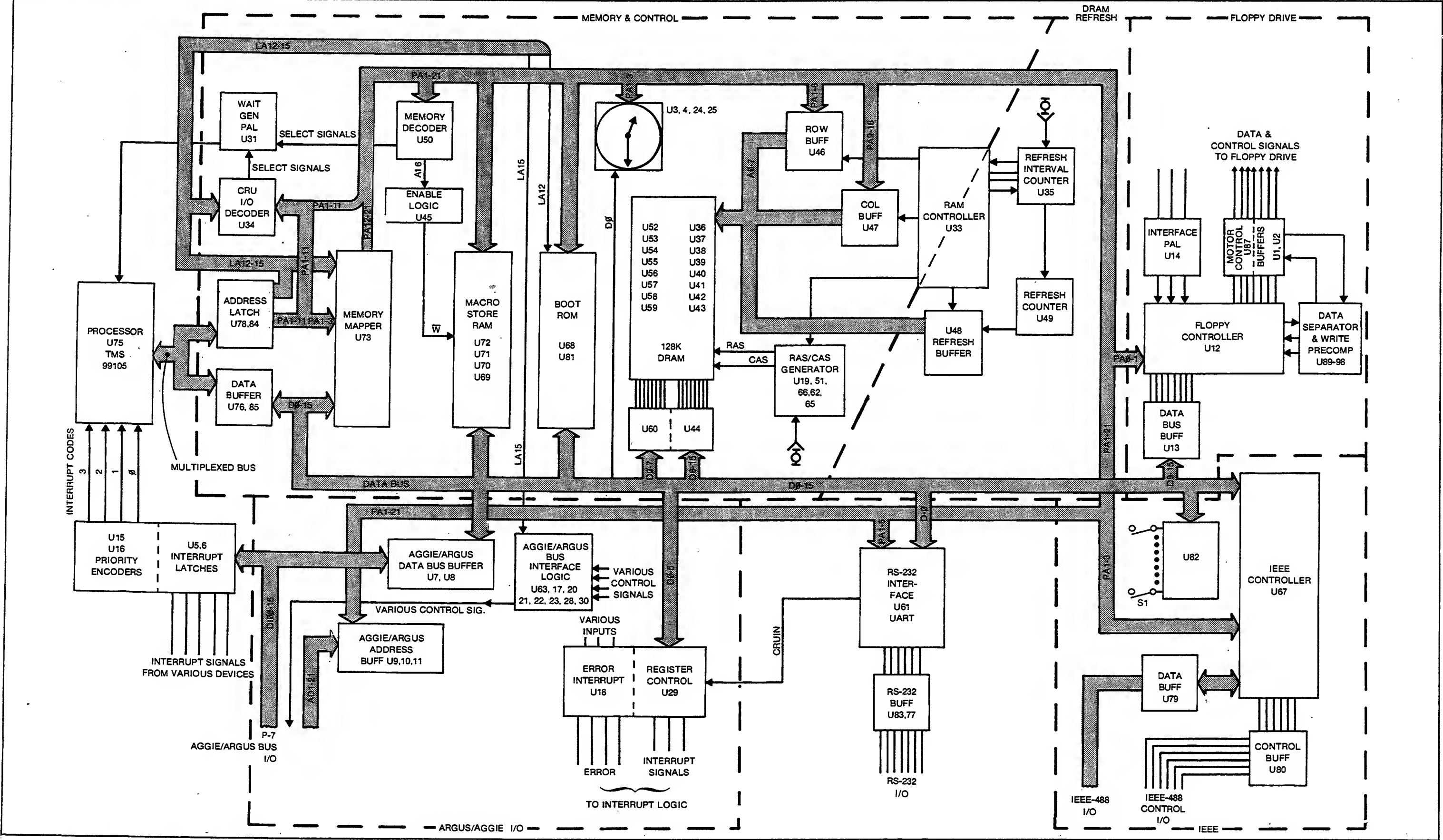


Table 2-1 shows the bus status codes the Microprocessor emits while it is operating. The memory cycle codes are emitted during memory cycles, and the I/O transfer codes are emitted during CRU I/O cycles. The AUMSL and AUMS codes are emitted when the Microprocessor is performing an internal operation, or when the Macrostore memory is being addressed. The DEN- and WE- signals are used to detect which type of cycle is occurring.

Figure 2-3 shows the timing of the memory and I/O cycles occurring on the bus.

2-29. DATA BUS

Sixteen bits of parallel data are buffered in U76 and U85 and sent over the Data Bus to the various devices requiring data. There is an additional Bus Buffer (U7 and U8) that drives the AGGIE bus.

2-30. ADDRESS BUS

NOTE

For timing diagrams of the AGGIE bus, see Figures 2-7, 2-8, and 2-9 later in this section.

The address bus is more complex than the data bus and is discussed in conjunction with memory mapping and CRU I/O operations. The address output of the Microprocessor is latched into U78 and U84 when they are enabled. When the memory mapper is disabled, the four most-significant bits of the address pass straight through the mapper, allowing the lowest 64K bytes of memory to be addressed directly.

2-31. MEMORY MAPPER

In order to address a specific 64K-byte part of the physical-address space, the SN74LS612 memory mapper (U73) must be programmed by the software, using CRU I/O instructions. The memory mapper is selected by the CRU I/O Decoder (U34). When the mapper is enabled, the four most-significant bits of the Microprocessor's address bus select the contents of one of 16 twelve-bit registers. The contents of the registers are loaded by the software into the mapper via the data bus.

The contents of the selected register provide the 10 most-significant bits of the physical address. When selected, these registers drive the 10 new address lines. Combined with the 12 lower address lines, the 10 new lines make up the 22 lines the AGGIE bus needs to address 4M bytes. The mapper can supply 12 address bits for the physical address space; however, the AGGIE SBC uses only 10 of these for address lines. The other two are used to generate write-fault and memory-error interrupts.

2-32. ADDRESS DECODING

Much of the address decoding information is buried in fuse patterns in the PALs. The address space of the SBC is conceptually divided into a logical-address space, a physical-address space, and a CRU address space. The logical-address space is that which can be directly addressed by 16 lines provided by the Microprocessor, and is limited to 64K bytes. The physical-address space is that which can be addressed through the memory mapper. It has 22 address lines that can address 4M bytes. The CRU-address space is used for I/O operations and is decoded directly from the address latch (U78 and U84).

Table 2-1. Bus Status Codes

MEM	BST 1 2 3	NAME	DESCRIPTION OF BUS ACTIVITY
0	0 0 0	SOPL	Memory Cycle (Source operand with MPILCK)
0	0 0 1	SOP	Memory Cycle (Source operand without MPILCK)
0	0 1 0	IOP	Memory Cycle (Immediate data, second op, addr)
0	0 1 1	IAQ	Memory Cycle (Instruction acquisition)
0	1 0 0	DOP	Memory Cycle (Destination operand transfer)
0	1 0 1	INTA	Memory Cycle (Interrupt acknowledge)
0	1 1 0	WS	Memory Cycle (Workspace transfer)
0	1 1 1	GM	Memory Cycle (General memory transfer)
1	0 0 0	AUMSL	Internal ALU operation or Macrostore access
1	0 0 1	AUMS	Internal ALU operation or Macrostore access
1	0 1 0	RESET	Reset (RESET- pin is pulled low)
1	0 1 1	I/O	I/O Cycle
1	1 0 0	WP	Workspace pointer update
1	1 0 1	ST	Status register update
1	1 1 0	MID	Macroinstruction detected
1	1 1 1	HOLDA	Hold acknowledge (in response to HOLD- low)

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SINGLE-BOARD COMPUTER(SBC)

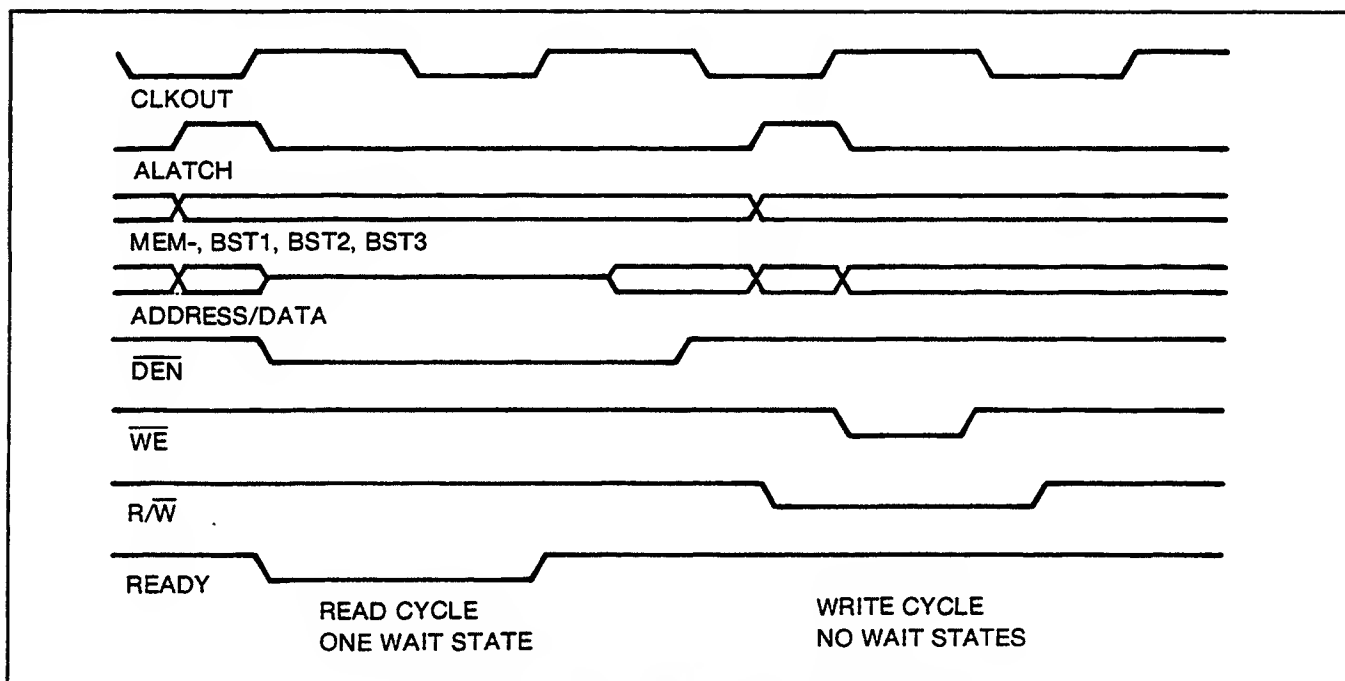


Figure 2-3. TMS99105A Memory and I/O Timing

2-33. CRU I/O Address Decoding

The CRU-I/O space of the Microprocessor has been divided into 11 address ranges. There are two address ranges within the CRU-I/O space that are used for registers inside the Microprocessor. The remaining nine address ranges are used for addressing I/O devices.

Most of the decoding is done in the CRU I/O Decoder (U34). This PAL uses the bus-status-code lines to detect a CRU I/O operation and uses address lines to select the I/O devices.

The CRU I/O Decoder directly selects the RS-232-C port, the memory mapper, the IEEE-488 interface, or the Floppy Disk Controller. It also produces two select signals that select the control register, the real-time clock register, the status and exception input, or the two ARGUS bus I/O address ranges.

2-34. Macrostore Address Decoding

When the Microprocessor accesses the Macrostore RAM (U72, U71, U70, and U69), it emits the AUMSL or AUMS bus status codes to select it. Since no address lines are decoded, the 4K words of Macrostore RAM appear eight times in the 32K words of the Macrostore address space.

The Macrostore address space on the SBC was designed to run with no wait states. The address lines for the Macrostore RAM come directly from the address latches, and do not pass through the memory mapper, eliminating the delay caused by address signals passing through the mapper.

2-35. Memory Address Decoding

The physical-memory space addressed by the SBC is divided into nine address ranges. Although the physical-memory space is divided into nine address ranges, there are only four memory devices in this range. These are the on-board dynamic RAM (U52-U59 and U36-U43), the EPROM (U68, U81), the Macrostore RAM (U69-U72), and the AGGIE/ARGUS Bus Interface (U5-U11, U15, U16, U20-U23, U28, U63, and U64).

Address decoding for the physical-memory space on the SBC uses Memory Decoder PAL (U50). This PAL produces select signals for the dynamic RAM, the ARGUS bus, the AGGIE bus, and the EPROM/Macrostore-select logic (U45, U32, and U64).

2-36. MEMORY

There are three types of memory on the SBC: EPROM, dynamic RAM, and static RAM. The Macrostore RAM is Static RAM and consists of U69, U70, U71, and U72. The Boot EPROM consists of U68 and U81. The dynamic RAM consists of sixteen 64K x 1-bit RAM chips (U52-U59 and U36-U43). The EPROM and ROM are familiar chips used on many Fluke products; however, the dynamic RAM merits some additional discussion.

2-37. Dynamic RAM

The RAM array uses 16 RAM chips, one for each data bit. A data buffer (U44, U60) is used to buffer the data between the RAM array and the data bus.

The RAM Controller (U33), a registered PAL, handles RAM refreshing and address multiplexing when the RAM is addressed.

Three buffers (U46, U47, U48) supply addresses to the RAM array. When the RAM is addressed, the column buffer (U47) supplies the eight most-significant bits of the address, and the row buffer (U46) supplies the eight least-significant bits. The 16-bit address is strobed into the array eight bits at a time. The RAS- (Row Address Select) is pulsed low to strobe in the lower eight bits and the CAS- (Column Address Strobe) input is pulsed low to strobe in the upper eight address bits. Data is written into or read from the RAM when CAS- is pulsed low. The W- input to the RAM is used to signal a read or write operation.

When the RAM must be refreshed, the Refresh Interval Counter (U35) signals the RAM Controller, and the refresh buffer (U48) supplies the refresh address.

The RAS and CAS Generator (U19, U51, U62, U65, and U66) handles the timing of the RAS- and CAS- signals, with a registered PAL and discrete logic. The dynamic RAM has two modes of operation: refresh, and read/write. These modes interact because the Microprocessor addresses the RAM at random intervals, but the RAM must be fully refreshed every 4 ms. It is probable that the Microprocessor will address the RAM when it is being refreshed, and it will be necessary to refresh the RAM while it is being addressed by the Microprocessor.

Refresh of the dynamic RAM is handled by the Refresh Interval Counter (U35) and the RAM Controller (U33). Roughly every 16 μ s, the Refresh Interval Counter (U35) signals the RAM Controller (U33) to refresh the RAM array. If a read/write operation is not taking place, then the RAM Controller (U33) enables the Refresh Buffer (U48), and signal the RAS and CAS Generator (U19, U51, U62, U65, U66), using INHIBIT and RFRRAS. The INHIBIT signal keeps the RAS and CAS generator from starting a read/write operation while the memory is being refreshed. The RFRRAS signal causes RAS- to be pulsed low. The RAM Controller (U33) then disables the Refresh Buffer (U48), increments the Refresh Address Counter (U49), and resets the Refresh Interval Counter (U35), preparing for the next refresh cycle. If a read/write operation is taking place, the RAM controller waits until the read/write cycle has finished and then goes through the above sequence.

Reading and writing to the dynamic RAM is handled by the RAS and CAS generator. The row buffer is always enabled when the RAM is not being refreshed. When the Microprocessor asserts ALATCH and MEM-, the RAS and CAS generator pulses RAS- low, which latches the eight least-significant bits of the address into the RAM chips. If the RAM select signal is active, then the RAS and CAS generator asserts RAMTRIG and pulses CAS- low. RAMTRIG causes the RAM controller to disable

the row buffer and enable the column buffer, sending the eight most-significant bits of the address to the RAM chips. Pulsing CAS- low latches data into the RAM if a write cycle is taking place, or reads data from the RAM if a read cycle is taking place. If the INHIBIT signal is active when the Microprocessor asserts ALATCH and MEM-, then the RAS and CAS generator waits until INHIBIT goes inactive before asserting RAS-, CAS-, and RAMTRIG.

2-38. INTERRUPT LOGIC

The SBC uses interrupts for most I/O operations. All I/O devices on the SBC use interrupts except the Real-Time Clock. The DCOK signal from the AGGIE bus resets the Microprocessor and all logic on the SBC during power-up. The DCOK signal also sends a non-maskable interrupt to the Microprocessor so the bootstrap code in the on-board EPROM will be executed.

2-39. Normal Interrupts

All normal interrupts are latched and priorities are assigned. The latches (U5 and U6) synchronize the interrupt requests with the Microprocessor. The Priority Encoder (U15 and U16) generates INTREQ- and the interrupt code for the highest priority interrupt. Five of the interrupts come from I/O devices on the SBC. The rest come from the AGGIE bus. A few typical AGGIE bus interrupts are shown in Table 2-2.

2-40. Error Interrupt Logic

The Error-Interrupt PAL (U18), a sequential-logic PAL, records fault conditions. This PAL causes a non-maskable interrupt when WBOOT goes active, and causes a Level-2 interrupt when any of the other inputs go active. The interrupt service routines determine which inputs went active by reading from the PAL. The PAL is connected to the data bus and is selected using the SYS-output of the CRU I/O Decoder (U34) and the EXEN-output of the Register Control PAL (U29). The software must clear the fault conditions by resetting the Error-Interrupt PAL (U18).

The inputs to the Error-Interrupt PAL and their functions are listed in Table 2-3.

The MERR and WERR signals are derived from 2 bits from the memory mapper, causing an interrupt if the software attempts to access data at an illegal logical address. MERR detects illegal addresses, and WERR write-protects memory. The mapper is programmed so that MERR or WERR goes active if an illegal page is addressed. If MERR goes active, it always causes a Level-2 interrupt. WERR causes a Level-2 interrupt only if the Microprocessor is writing to memory.

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Table 2-2. AGGIE Bus Interrupts

INPUT	INTERRUPT	FUNCTION
DI00	Level 0	AGGIE Bus Interrupt
1797DRQ	Level 1	Floppy Data Request (For Data Transfer)
Level 2	Level 2	Exception (Fault) Conditions
DI03	Level 3	AGGIE Bus Interrupt (Bubble Memory Option)
1797INT	Level 4	Floppy Interrupt Request (For Status/Errors)
DI05	Level 5	AGGIE Bus Interrupt (Parallel Interface)
DI06	Level 6	AGGIE Bus Interrupt (IEEE-488/RS-232-C Option)
9902AINT	Level 7	RS-232-C Interface Interrupt
DI08	Level 8	AGGIE Bus Interrupt (VGK Interface)
9914AINT	Level 9	IEEE-488 Interface Interrupt
DI10	Level 10	AGGIE Bus Interrupt (IEEE-488/RS-232-C Option)
DI11	Level 11	AGGIE Bus Interrupt
DI12	Level 12	AGGIE Bus Interrupt
DI13	Level 13	AGGIE Bus Interrupt
DI14	Level 14	AGGIE Bus Interrupt
DI15	Level 15	AGGIE Bus Interrupt

Table 2-3. Error Interrupts

INPUT	INTERRUPT	FUNCTION
WBOOT	NMI	Re-boot the system.
TIMEOUT	Level 2	Occurs if non-existent device is addressed.
MERR	Level 2	Occurs on illegal memory addresses.
WERR	Level 2	Occurs on write to write-protected memory.
HALT	Level 2	Occurs when AGGIE BUS HALT signal is active.
ABORT	Level 2	Occurs when AGGIE BUS ABORT signal is active.

2-41. TIME-OF-DAY CLOCK (NON-VOLATILE CLOCK)

The Non-Volatile Clock uses an NEC μ PD4990AC calendar/clock chip (U24) to keep track of the time and day, and a CMOS shift register to keep track of the year. A battery on the SBC powers the μ PD4990AC and the shift register, allowing the clock to keep time when ac power is off. The clock circuit uses a serial CRU I/O interface with the Microprocessor. The control register is selected using the CRU I/O Decoder (U34) and part of the REGISTER CONTROL PAL (U29). U29 also buffers output data from the NEC μ PD4990AC onto the data bus (not shown on the block diagram). The registers within the μ PD4990AC and the shift register are read or written one bit at a time. The control register is used to select the bits and read or write them.

2-42. I/O DEVICES

2-43. Floppy Interface

The Floppy Interface uses a WD1797 floppy-disk-controller chip (U12) to control a 5-1/4 inch disk drive. The interface is selected with an output from the CRU I/O Decoder (U34). Interface PAL (U14) and buffer (U13) are the interface between the Floppy Controller and the Microprocessor. These two devices adapt the

Microprocessor's I/O cycle timing to the Floppy Controller's read/write cycle requirements. Besides producing timing signals for the Floppy Controller, the Interface PAL (U14) also produces a 3 MHz clock signal used by the IEEE-488 Controller (U67) and the RS-232-C Interface UART (U61).

A buffer chip (U2) is used between the Floppy Controller and the disk drive. The Motor Control (U87) performs two functions. It shuts off the disk drive motor when the interface has been idle for a time, and it turns the motor on when the interface becomes active or when a new disk is inserted into the drive.

A flip-flop (U23) detects that the disk has been swapped (replaced with another disk, sometimes referred to as a media swap). The software uses this status information to decide whether to read the directory from the disk. The disk-swapped signal is read by the Microprocessor through the Register Control PAL (U29).

Write precompensation is performed by three one-shots (U90 and U93). This causes the write pulse to occur 250 ns earlier or later than nominal. It counteracts the effect of higher bit densities on the inner tracks of the disk.

Data recovery is accomplished with a phase-locked loop data separator (U89, U94, U95, U96, U97, and U98). The free-running frequency of the voltage controlled oscillator (VCO) is adjusted with a potentiometer. Refer to the calibration procedure in Section 3, Maintenance, for instructions on adjusting the VCO frequency.

NOTE

SBC assemblies marked Rev D use the WD2797 Floppy Controller which performs the functions of write precompensation and data recovery internal to the chip. There are three adjustments necessary to calibrate the WD2797 Floppy Controller. These are VCO frequency, write pulse width, and read pulse width. See Section 3 for instructions on performing these adjustments.

2-44. IEEE-488 Interface

The IEEE-488 Interface uses a TMS9914A IEEE-488 Controller chip (U67). This chip is in the parallel CRU I/O address space for the Microprocessor. The IEEE-488 is selected with an output from the CRU I/O Decoder. Two buffer chips (U79, U80) are used for logic translation between the IEEE-488 controller and the IEEE-488 bus.

A 10-position switch (S1, shown in Figure 2-4) is used to select the IEEE-488 port address and whether the port is to be a system controller. This switch also selects the baud rate for the RS-232-C port during power-up. Except for the system controller function, the switch settings are read and interpreted by the software. The switch settings are read onto the data bus whenever an input from the IEEE-488 Controller occurs. Pinouts for the IEEE-488 connector are shown in Figure 2-5.

2-45. RS-232-C Interface

The RS-232-C Interface on the SBC uses a TMS9902A Universal Asynchronous Receiver/Transmitter (UART) chip (U61). This chip is a serial CRU I/O interface for the Microprocessor. The RS-232-C Interface UART (U61) is selected by the CRU I/O Decoder and part of the Register Control PAL (U29). PAL U29 also buffers the output data from the RS-232-C Interface UART onto the data bus. Level translators convert the TTL levels used by the UART (U61) into the voltage levels required by the RS-232-C protocol. The RS-232-C connector pinouts are shown in Figure 2-6.

2-46. AGGIE/ARGUS Bus Interface

A control signal called ADVAL- signals that a memory or parallel I/O bus cycle is taking place on the ARGUS bus, and a control signal called AGVAL- is used to signal that a memory or parallel I/O cycle is taking place on the AGGIE bus. These two signals differentiate ARGUS bus cycles from AGGIE bus cycles. When a memory or

parallel I/O device is selected, it must respond with ADACK-. When a CRU bit is addressed, the device selected must respond with the CRACK- signal and supply data on the CRIN line. CRCLK- is used to latch data from CROUT into a device's register during a CRU I/O write. The AGGIE/ARGUS bus interface is selected by three signals, AGGIE-, ARGUS-, and CRU-, which are produced by address decoders U34 and U50. The AGGIE- signal selects AGGIE memory devices with the AGVAL- signal. The ARGUS- signal selects ARGUS memory devices with the ADVAL- signal. The CRU- signal selects CRU I/O or memory-mapped I/O on the ARGUS bus.

The data from the Microprocessor is buffered onto the AGGIE bus by buffers U7 and U8. Buffer U21 buffers the CRIN and CROUT signals from the AGGIE bus to the most- and least-significant bits of the Microprocessor data bus for serial CRU I/O. The buffers are enabled and disabled by the buffer-control-logic PAL (U20). The AGGIE bus PAL (U20) enables data bus buffers U7 and U8 when it receives the ARGUS or AGGIE signals from the CRU I/O decoder (U34) in conjunction with the R/W signal from the Microprocessor.

The physical-address lines from the memory mapper and the Microprocessor are buffered onto the bus by U9, U10, and U11. Two of the address lines, signals AD16 and AD17, are altered by the Memory Decoder (U50) for compatibility with the ARGUS bus because the ARGUS bus sets AD16 and AD17 high for memory-mapped I/O.

2-47. TIMING

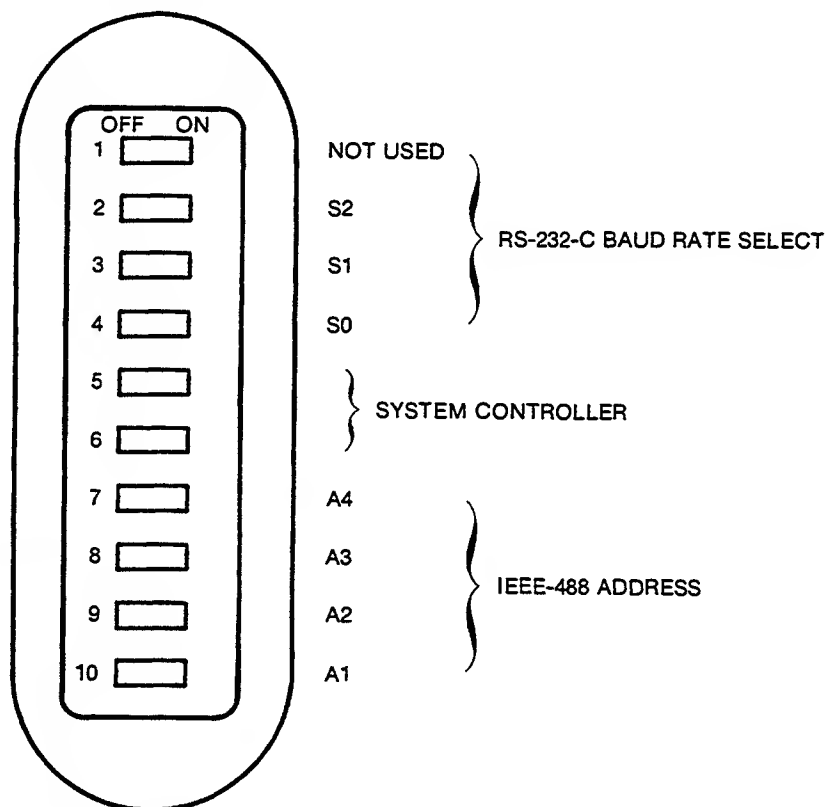
2-48. Wait State Generator

The WAITGEN PAL (U31) is a registered PAL that is clocked by the CLKOUT signal from the Microprocessor. It can be thought of as a timer with the timeout period set by its inputs to 0, 1, 2, 3, or a variable number of clock cycles.

All Microprocessor cycles begin with ALATCH and end with READY. The READY signal to the Microprocessor is delayed by the Waitgen PAL (U31). This PAL is used to cause wait states in the Microprocessor's timing when a device is addressed. Wait states are necessary because not all devices can accept or supply data within one memory cycle.

Ready signals from the dynamic RAM and AGGIE bus interface are used to cause a variable number of wait states. The dynamic RAM usually causes one wait state, but more may be required to handle memory refreshing. The AGGIE bus will cause a variable number of wait states from 3 on up depending upon the device addressed on the bus. Select signals from the CRU I/O Decoder (U34) and Memory Decoder (U50) cause 0, 1, 2, or 3 wait states.

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SINGLE-BOARD COMPUTER(SBC)



SWITCH SETTING										FUNCTION
1 —	2 S2	3 S1	4 S0	5 SC	6	7 A4	8 A3	9 A2	10 A1	
x	unused									
								IEEE-488 ADDRESS		
				0 0 0 0				0		
				0 0 0 1				1		
				"						
				"						
				1 1 1 1				15		
				IEEE-488 CONTROLLER						
	0 0						System Controller			
	1 1						Idle Controller			
	BAUD RATE									
	0 0 0						110			
	0 0 1						300			
	0 1 0						600			
	0 1 1						1200			
	1 0 0						2400			
1 0 1						4800				
1 1 0						9600				
1 1 1						19200				
NOTE: 1 = on; 0 = off.										

Figure 2-4. IEEE-488/RS-232-C Switch (S1)

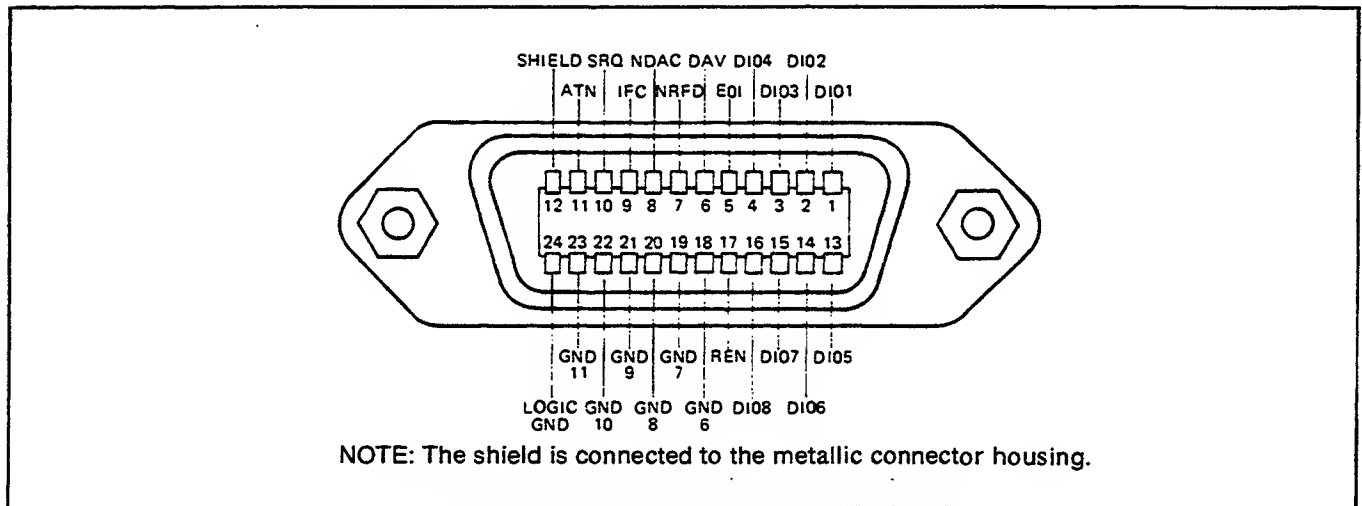


Figure 2-5. IEEE-488 Connector Pinouts

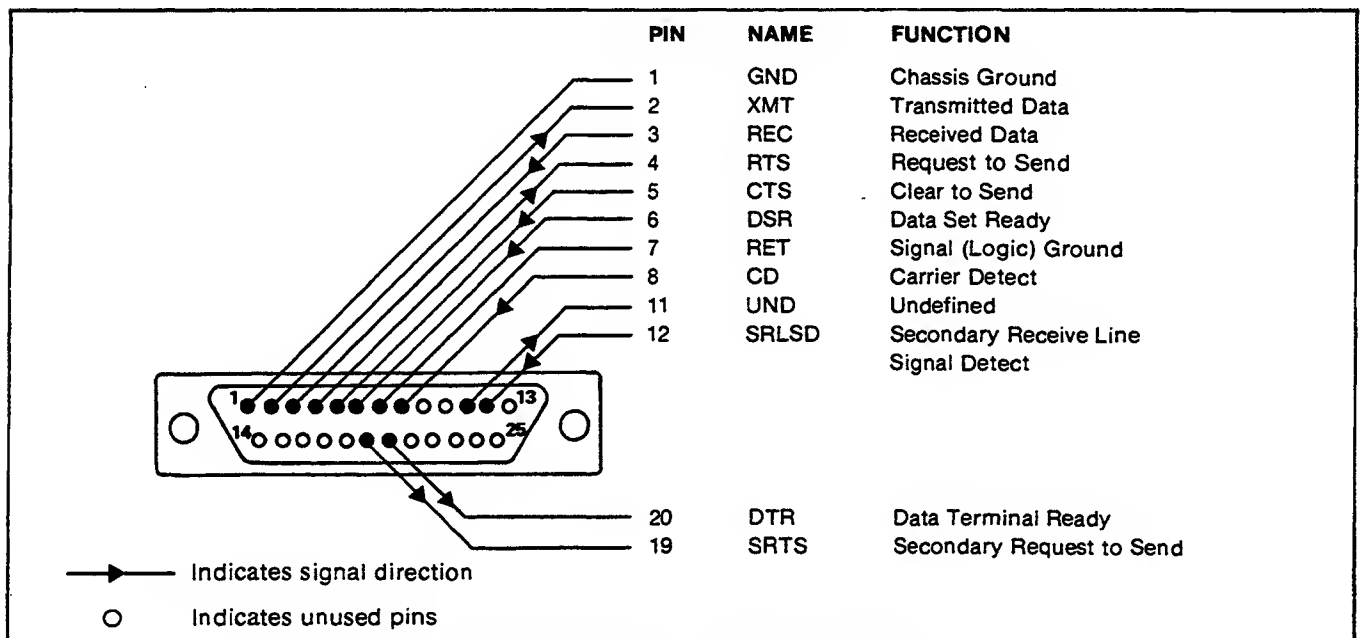


Figure 2-6. RS-232-C Connector Pinouts

The OTHER signal from the CRU I/O Decoder occurs whenever a non-memory or non-I/O cycle is detected. These cycles occur when the Microprocessor is performing an internal operation or a Macrostore operation and require no wait states. The bus status codes for these are AUMSL, AUMS, RESET, WP, ST, MID, and HOLDA.

2-49. AGGIE Bus Timing

Bus-control signals are controlled by a State Machine using a sequential-logic PAL (U22) and two flip-flops (U23, U30). The State Machine (U22) causes RINT- to go active. When RINT- is active, interrupt requests may be placed on the data lines.

The Timeout Counter (U63) ends a memory or I/O cycle when the Microprocessor is waiting for a ready signal that never occurs, due to a faulty or non-existent device.

A device selected for parallel I/O using the AGVAL- or ADVAL- signal must respond with the ADACK- signal when it is ready to complete a bus cycle. If a device does not respond with ADACK-, the timeout counter causes the cycle to end and causes a timeout interrupt. The ADACK- signal may be used to insert wait states up to the limit set by the timeout counter.

A device selected for serial CRU I/O must respond with CRACK-. If a device does not respond with CRACK-, the bus cycle completes normally, but no data is read or

THEORY OF OPERATION

VIDEO/GRAPHICS/KEYBOARD INTERFACE(VGK)

written. The CRU- signal causes the ADVAL- signal to go active when the Microprocessor is doing a parallel CRU I/O operation. Otherwise, the CRU- signal causes CRIN, CROUT, CRCLK-, and CRACK- to be used for serial CRU I/O operations.

Figures 2-7 through 2-10 show typical timing diagrams for bus cycles as follows:

- Figure 2-7 shows timing for AGGIE memory devices.
- Figure 2-8 shows timing for ARGUS bus memory and I/O cycles.
- Figure 2-9 shows timing for a serial CRU I/O bus cycle.
- Figure 2-10 shows timing for interrupts.

Table 2-4 shows the AGGIE bus pinouts.

2-50. VIDEO/GRAPHICS/KEYBOARD INTERFACE (VGK)

2-51. Introduction

The VGK provides an interface between the SBC (Single-Board Computer) and the TSO (Touch-Sensitive Overlay), the programmer's keyboard, and the video display.

One major function of the VGK is to control the CRT. Codes received by the VGK from the SBC cause characters and graphics to be displayed. The circuitry on the VGK converts the image specification into the sync and video signals that are sent to the video monitor.

The other primary function of the VGK is to provide input from the user. The 1722A can be controlled by either the TSO or the removable programmer's keyboard. The VGK includes circuitry to detect key closures on the TSO and the keyboard. These user inputs are sent to the SBC as character codes over a serial link.

A block diagram of the VGK is shown in Figure 2-11. To describe the operation of the VGK it is helpful to divide its circuitry into five sections:

- The general-purpose microprocessor system
- The ARGUS-bus interface
- The TSO and keyboard interface
- The character display
- The graphics display

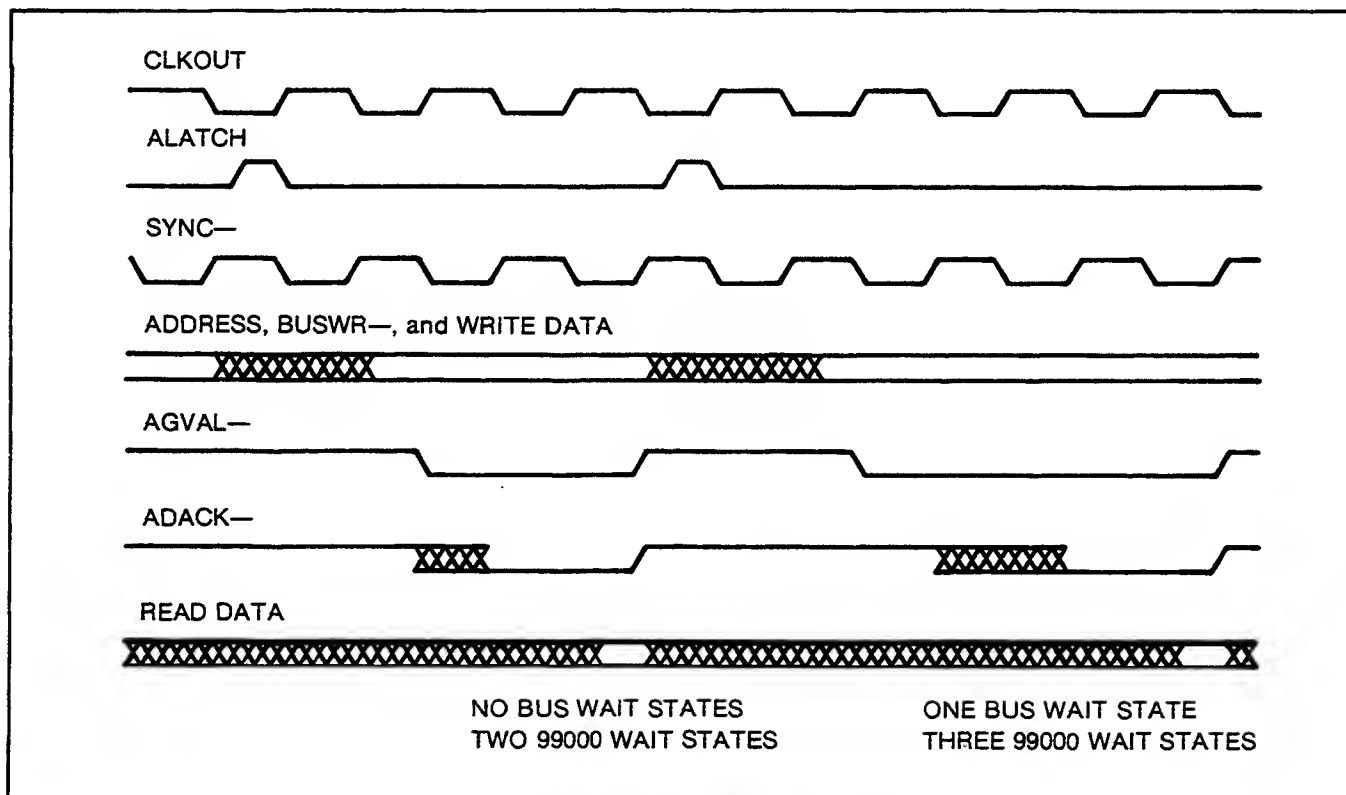
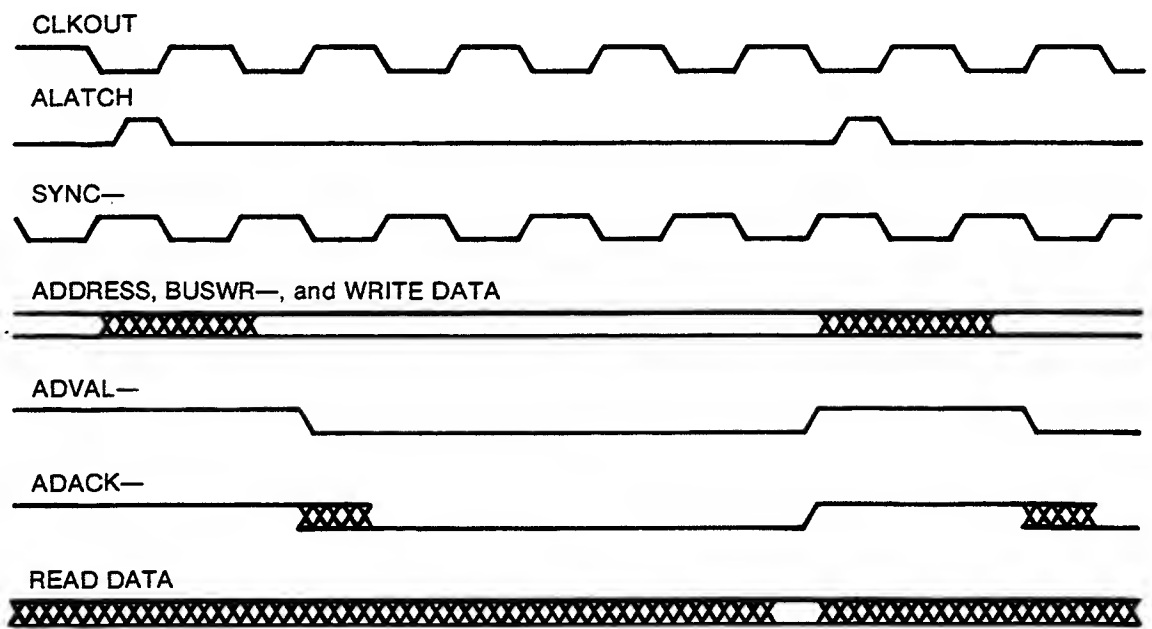
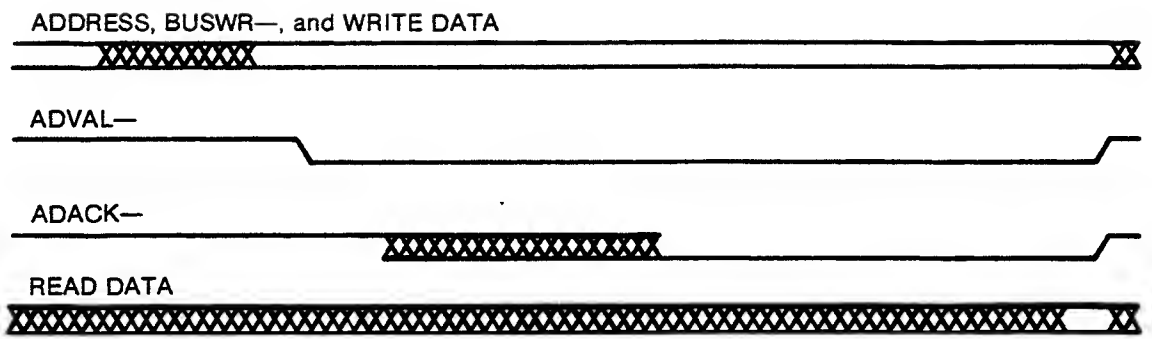


Figure 2-7. AGGIE Bus Memory Timing



A. NO BUS WAIT STATES



B. ONE BUS WAIT STATE

Figure 2-8. ARGUS Bus Memory and I/O Cycle Timing

THEORY OF OPERATION
VIDEO/GRAPHICS/KEYBOARD INTERFACE(VGK)

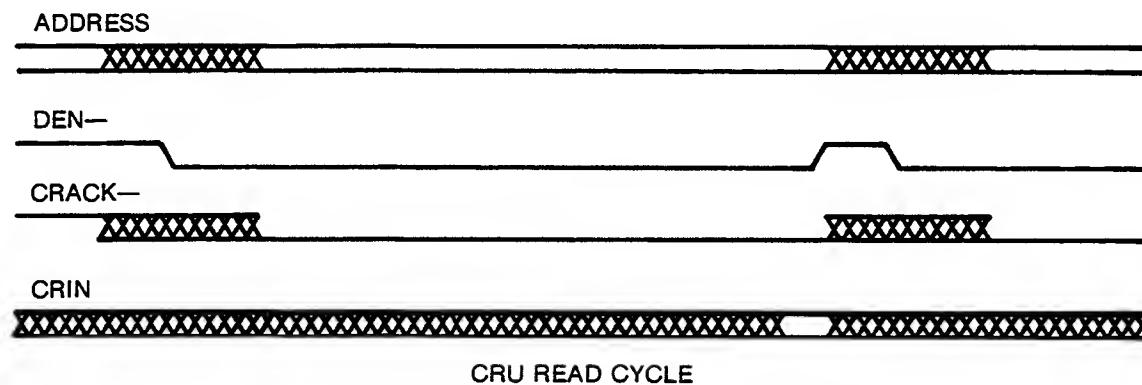
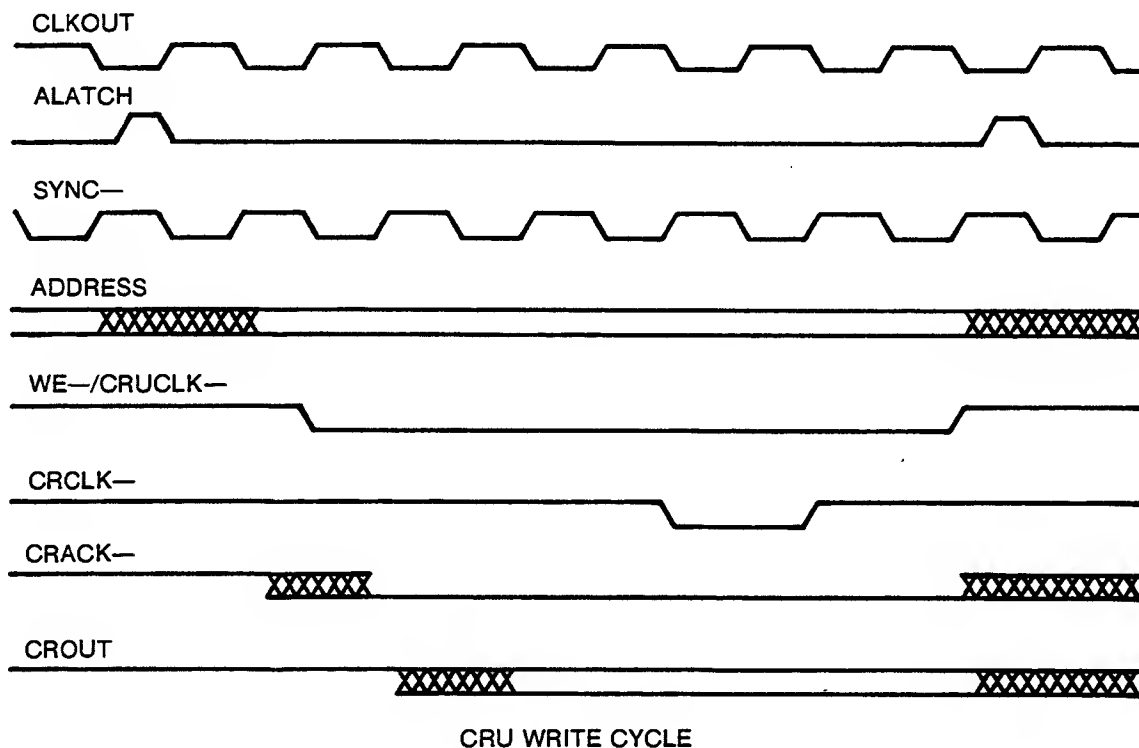


Figure 2-9. ARGUS Bus CRU Cycle Timing

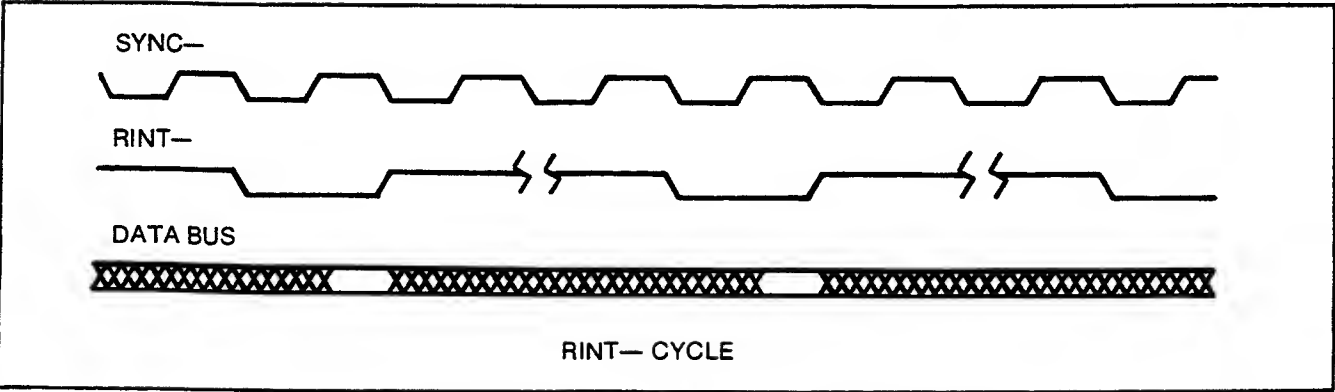


Figure 2-10. AGGIE Bus Interrupt Timing

Table 2-4. AGGIE Bus Pinout

NAME	PIN	PIN	NAME
LCOM	1	2	LCOM
LCOM	3	4	LCOM
+5VB	5	6	+12VB
AD19	7	8	AD18
AD17	9	10	AD16
BUSWR-	11	12	HALT-
RQOUT-	13	14	RQIN-
GRIN-	15	16	GROUT-
ADVAL-	17	18	BMODE-
LCOM	19	20	ABORT
DI15	21	22	DI14
DI13	23	24	DI12
DI11	25	26	DI10
DI09	27	28	DI08
DI07	29	30	DI06
DI05	31	32	DI04
DI03	33	34	DI02
DI01	35	36	DI00
LCOM	37	38	RINT-
CRIN	39	40	CROUT
CRCLK-	41	42	CRACK-
AGVAL-	43	44	ADACK-
AD21	45	46	AD20
AD15	47	48	AD14
AD13	49	50	AD12
AD11	51	52	AD10
AD09	53	54	AD08
AD07	55	56	AD06
AD05	57	58	AD04
AD03	59	60	AD02
AD01	61	62	AD00
-5VB	63	64	DCOK
LCOM	65	66	LCOM
SYNC	67	68	-12V
+5V	69	70	+5V
+12V	71	72	+12V

2-52. The Microprocessor

The VGK is controlled by a TMS-9995 microprocessor (U30). The circuitry that surrounds it provides address decoding and buffering for the RAM, EPROM, and I/O devices.

2-53. ADDRESS LOGIC

The 16 address lines from the microprocessor are buffered by U19 and U38. The upper two bits are decoded by the two halves of U16. One section is enabled by a low level on MEMEN-, and is used to decode memory and register references. The other half of U16 is enabled when MEMEN- is high for CRU transfers.

The memory enable signals from U16 (pins 4-7) divide the memory space into sections for ROM, RAM, and registers. The RAM (U28) is used by the processor for I/O buffers and other variables. It is a 2K-by-8 device, with unmarked jumpers to allow expansion to a larger device in the future. The firmware is contained in a 8K-by-8 EPROM (U29). If more code space is required, cutting a trace and installing a jumper will allow the use of a 16K-by-8 device.

The address PAL (U18) decodes, at least partially, all other memory addresses in the system. It is enabled during the upper fourth of the memory addresses (A15 and A14 high) and uses DBIN-, WE-, and A13-A10 to decode several sections. Further decoding is performed for each section by selectors U48, U20, and U78. Table 2-5 shows the VGK memory map.

Most memory and registers may be accessed by the microprocessor at any time, but some require special synchronization. To accomplish this, the addressing PAL uses the RDY output to extend certain processor cycles. This signal is synchronized to the microprocessor clock by U14, and is connected to the READY line (pin 23) of the processor. When READY is high, the software proceeds from one instruction to another at full speed. When READY is low, the processor stops to wait for a slow device.

THEORY OF OPERATION
VIDEO/GRAPHICS/KEYBOARD INTERFACE (VGK)

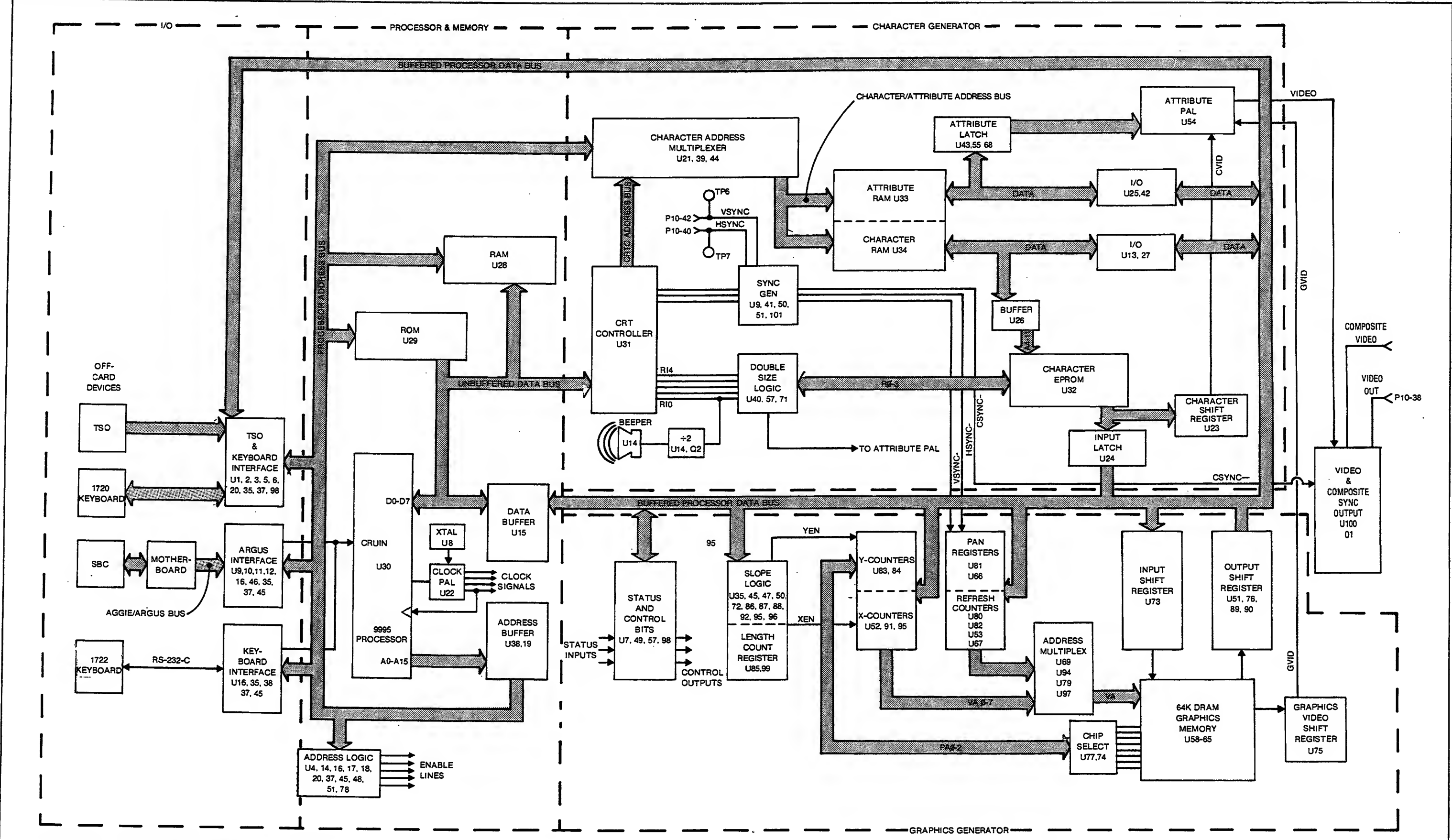


Figure 2-11. VGK Block Diagram

Table 2-5. VGK Memory Map

CRU BASE ADDR	DEVICE
8000	Host UART
C000	KB UART

MEMORY BASE ADDR	ADDRESS LINES				READ REGISTER OR DEVICE	WRITE REGISTER OR DEVICE
	fedc	ba98	7654	3210		
fc00	1111	11--	---	---	attr latch (U42)	attr latch (U25)
fa07	1111	101-	---	-111	-	xl (U91,93)
fa06	111	101-	---	-110	-	xh (U52)
fa05	111	101-	---	-101	-	yl (U83,84)
fa04	1111	101-	---	-100	-	cl (U85,99)
fa03	1111	101-	---	-011	-	ml (U72)
fa02	1111	101-	---	-010	-	mh (U92)
fa01	1111	101-	---	-001	-	pan-y (U66)
fa00	1111	101-	---	-00	-	pan-x (U81)
f400	1111	01--	---	---	CRTC- (U31)	CRTC- (U31)
e603	1110	011-	---	--11	gdot (U89)	gdot (U73)
e602	1110	011-	---	--10	clra (U87,96)	led (U1)
e601	1110	011-	---	--01	crom (U24)	ctrl2 (U7)
e600	1110	011-	---	--00	status (U98)	ctrl1 (U49)
e400	1110	010-	--**	****	KB (U3,6,37)	—
d000	1101	-***	****	****	attr (U42)	attr (U25)
c000	1100	-***	****	****	char (U27)	char (U13)
8000	10--	---	---	---	-	-
4000	01--	-***	****	****	RAM (U28)	RAM (U28)
0000	00-*	****	****	****	ROM (U29)	ROM (U29)
Legend: * address bit is decoded in the device - address bit is ignored						

For example, the CRTC (CRT controller) requires more time to accept new data than other registers on the VGK. When the CPU writes to the CRTC the addressing PAL brings the RDY line low. When the write cycle is complete, the CRTC RDY line is set to a logic high level (by circuitry that is explained later). CRTC RDY informs the addressing PAL that the transfer is complete and the RDY line is returned to a high level so that the processor can proceed.

In-line resistor R12 allows the RDY signal to be overridden for testing purposes. By pulling TP3 ("READY")

low, the processor will stop on the current instruction. If TP3 is held high, the processor will continue at full speed even during accesses which should be delayed.

2-54. DATA INPUT AND OUTPUT

The data bus of the microprocessor is connected directly to the system RAM, EPROM, and the CRT controller (U31). This direct connection is faster and reduces the load on the outputs of the VLSI devices. Data transfers with other devices are buffered through U15. The addressing PAL (U18) disables the buffer when it is not needed.

In addition to the system RAM and EPROM, the microprocessor can access a number of hardware registers. Two of these registers, U7 and U49, are eight-bit latches used for controlling individual signal lines. For example, the BEEP line (U7, pin 19) enables U14, which divides an output of the CRTC by two to produce a 3-kHz tone for the speaker on the motherboard. Transistor Q2 buffers the divider output.

The status register (U98) is an eight-bit input port used to read the logic value on individual signal lines. Four of these are connected to user selectable jumpers (JPR-1). When no jumper is present the line is pulled high by a 10-k Ω resistor (Z2). When a jumper is installed, the line is grounded and the software reads a logic low. The function of the jumpers is defined by the software; they are all normally open.

2-55. ARGUS Interface

2-56. DATA COMMUNICATION

The 1722A Single-Board Computer (SBC) communicates with the VGK through a serial link. There are two UART chips on the VGK which are connected together "back-to-back." The transmitter output of each UART is tied to the receiver input of the other. One UART (U10) is in the SBC CRU space, and the other UART (U46) is in the CRU space of the VGK microprocessor. This arrangement allows the two independent systems to communicate without synchronization. It has the further advantage of simplifying the SBC boot procedure. If the VGK is missing or defective, the SBC communicates through the external RS-232-C port simply by addressing a different UART.

The ARGUS interface consists of three-and-one-half chips that connect the host UART (U10) to the bus. U12 is a buffer that provides CRUOUT, SYNC, DCOK and the bit address lines to U10. The 3-MHz clock required by the UART is derived by dividing the SYNC signal by two in U9. The remaining logic is contained in the ARGUS interface PAL (U11). This PAL performs the following functions:

- It decodes the CRU board address and returns the open collector CRU acknowledge.
- It gates the tristated CRUIN- signal.
- It inverts and buffers CRUCLK.
- It gates the UART interrupt onto D8 during RINT using an open collector driver.

The other UART (U46) is a CRU device of the VGK microprocessor. The CRU address space is decoded into four sections by U16. MEMEN- is inactive (high) during a CRU access. It is inverted by U35 (pin 6) and is used to enable U16 (pin 15).

The clock input to the UART is connected to the CLKOUT signal from the microprocessor (buffered by U37). This signal is the dot clock divided by four, which results in a frequency of about 3.2 MHz. The two UARTs have internal dividers set to appropriate values so they can exchange data at 19200 bits per second.

When the UART (U46) has sent or received a character, it interrupts the VGK microprocessor by asserting INT- (pin 1) low. The interrupt output lines from this UART and the one for the 1722A keyboard are ORed together by U45 so that either one can get attention from the processor.

2-57. POWER-ON PRESET

The other function of the ARGUS interface is the power-on preset. The DCOK signal is held low during power-up by a circuit in the 1722A power supply. DCOK does not become active until all of the dc voltages in the system are in-range and stable. DCOK is also forced low by an operator-initiated cold reset (explained in the section describing the Power-Up Module). This signal is used to force the VGK into a known, safe state.

The DCOK signal is buffered by U12 and is used to perform the following functions:

- Clear U1 to turn off the CLICK line.
- Clear U7 to disable GREN and CHEN to turn off the display before the microprocessor clears it.
- Clear U49 to disable BEEP to avoid unwanted noise.
- Restart the microprocessor.

All other control lines can be initialized by the software. Resistor R11 isolates the CPU reset from DCOK. When TP2 is grounded, the microprocessor is reset but the other devices connected to DCOK are unaffected.

2-58. TSO and Programmer's Keyboards

The VGK includes two keyboard interfaces. When the VGK board is plugged into a 1722A, the Y1700 Programmer's Keyboard may be attached to the 5-pin DIN connector on the front panel. When the VGK board is installed in a 1720A, a 24-pin connector is provided for the Y1720 keyboard.

2-59. 1722A KEYBOARD INTERFACE

The 1722A keyboard is a microprocessor-controlled subsystem which communicates with the host over a TTL-level serial link. The VGK processor is connected to the keyboard through a 9902A UART (U36). Most of the communication is from the keyboard to the VGK over the

"FROMKB" line (pin 37 of the application connector, P10). A code is sent every time a key is pushed. There is also a status byte that is sent every one or two seconds. A resistor pulls FROMKB high to inhibit false characters when the keyboard is disconnected.

There are a few codes which are sent from the VGK to the remote keyboard over the "TOKB" line (pin 39 of P10). These commands are used to turn the remote LEDs on and off. The Page-Mode and Caps-Lock LEDs are controlled by the VGK firmware, while other LED lines, which may be used by remote controls, are set and reset by user software. Resistor R14 is in series with TOKB because pin 39 of connector P10 is grounded when the VGK is installed in a 1720A. Refer to Table 11-1 in Section 11 of this manual for LED codes. Order option 17XXA-300/AA for the rear panel Remote Interface connector.

2-60. 1720A KEYBOARD INTERFACE

When the VGK board is installed in the 1720A, the Model Y1720 keyboard is used. This keyboard does not have an on-board microprocessor; therefore, it uses a different circuit on the VGK board.

Each key on the Model Y1720 keyboard is addressed as part of an eight-bit field within the CRU space of the VGK Microprocessor. Each key is a bit in the eight-bit field and can be either 0 or 1 depending upon whether the key is depressed. The address and bit position of the keys is shown in Table 2-6.

To read the state of a particular bank of keyboard switches, the microprocessor performs a dummy read at

the associated address. The address is latched into U3 and sent to the keyboard on PSK0-3. These lines are decoded into nine open-collector column strobes on the keyboard. A closed switch connects a column output to a row input (KR0-7). These inputs are gated onto the VGK data bus by U6 and U37. Low bits at the input to U6 indicate a closed key. Z2 pulls open inputs high. After the input lines have had time to settle, a second read is performed at the same location to determine which keys are closed.

The Caps Lock and Page Mode LEDs are driven from a buffered latch (U7). The key clicker and the seven external LEDs are driven from buffered latch (U1) followed by a bus buffer (U2). The signals from the shift and control keys are pulled to ground when the associated key is closed. These signals are pulled up by Z2 and read into the Microprocessor through U98.

2-61. TOUCH-SENSITIVE OVERLAY (TSO)

The TSO consists of a 10-by-6 array of contacts, with 10 columns and 6 rows. Each column is mapped into a byte of memory beginning at E430. When the processor reads from one of the TSO addresses, the four low-order bits are latched into U3. These bits are decoded into one of 10 column outputs by U5. Touching the TSO causes a contact closure that connects a column output to a row input, pulling it to ground, as with the Model Y1720 keyboard. The row inputs are pulled up by Z1 and detected by the CMOS inputs of U6. Z3 is provided for static protection of the CMOS inputs, which are used to allow higher TSO contact resistance.

Table 2-6. Keyboard Map

BANK	ADDRESS	KEY REPRESENTED BY BIT							
		7	6	5	4	3	2	1	0
0	E40C	1	<esc>	Q	<tab>	<cap>	—	Z	<nxt>
1	E40D	3	2	E	W	S	A	C	X
2	E40E	5	4	T	R	F	D	B	V
3	E40F	7	6	U	Y	H	G	M	N
4	E41C	9	8	O	I	L	J	"	,
5	E41D	—	0	[P	:	K	<pag>	?
6	E41E	—	+]		"	—	<spc>
7	E41F	<up>	<bak>	<lt>	—)	<rt>	<ln>	—
8	E42C	<dl>	<dn>	<dlc>	<rt>	—	—	—	—
9	E42D	—	—	—	—	—	—	—	—

Where:

<esc> = escape
<tab> = tab
<cap> = caps lock
<nxt> = next page
<spc> = space bar

<lt> = left arrow
<up> = up arrow
<bak> = back space
<dn> = down arrow
<rt> = right arrow

<lf> = line feed
<dl> = delete line
<cr> = carriage return
<dlc> = delete character
<pag> = page mode

2-62. Character Display

The VGK supports 16 lines of 80 characters. Each character position on the screen has a corresponding location in the character memory. Two independent processes are involved in the character display: memory update and screen refresh. The VGK microprocessor stores data into the character memory as a result of commands from the SBC. At the same time, the contents of the character memory is continuously read and translated into bit patterns which are placed on the screen.

2-63. CHARACTER-GENERATING ROM

Each character is displayed on the screen in a cell eight dots wide by 14 dots high. The dot pattern for each character is stored in 16 bytes of the 4K-by-8 character-generating EPROM (U32). The four lowest address bits are used to indicate the current scan row. The upper eight address bits choose one of 256 characters. The user has access to two software selectable 128-character sets.

The contents of the character-generating EPROM can be read by the VGK processor. A latch (U24) stores the output of the EPROM (U32) when the cursor is displayed. U57 is a one-bit flag which indicates that the cursor has been active since U24 was last read. To read a given scan row of a character pattern, the character is placed under the cursor, which is programmed to be active on the desired scan row. A dummy read of U24 is performed to clear U57. Later, when the output of U57 is active again, U24 contains the datum of interest.

2-64. CHARACTER TIMING

To display one row of 80 characters on the screen, the corresponding memory locations are read 14 times, once for each scan row in the character cell. As the CRT scans the top row of a line of characters, the VGK places the required bit pattern on the video output. There are 640 active pixels on each scan row; that is, eight dots for each of 80 characters. When the CRT refreshes the next row, the dot pattern will be the second row of the same characters. This process is illustrated in Figure 2-12.

The CRTC (CRT Controller) provides the read addresses to the character RAM and EPROM. Each line of characters is read 14 times while the row outputs count from 0 to 13. The CRTC also provide HSYNC and VSYNC outputs to control the monitor.

The display must be refreshed 60 times each second (50 Hz in Europe) so that stray magnetic fields from near-by power transformers do not cause the display to roll. The refresh speed indirectly determines the dot clock frequency. The monitor requires about 42 scan rows for vertical retrace; this, added to the 224 displayed scan rows (16 lines with 14 scan lines each), makes 266 scan rows in

1/60th of a second. This density implies a horizontal frequency of 15.960 kHz. The monitor requires 20 character-times for horizontal retrace. These 20, added to the 80 displayed characters, result in 100 character-times in every scan row, or one character every 627 ns. Finally, 8 dots in each character implies a dot rate of 12.77 MHz.

The crystal oscillator (U8) on the VGK runs at 25.54 MHz. This signal is divided in half in the clock PAL (U22) to generate DCLK, the clock used to shift data to the monitor.

The bits for a new character are sent to the monitor every 627 ns. Three steps are involved in this process. First, a character code is read from the memory (U34). The code is latched (U26) along with the current row address (U40) from the CRTC to form the address for the character generating EPROM. The bit pattern is read out of the EPROM (U32) and loaded into the character shift register (U23). Each bit is then shifted through the attribute PAL (U54) and out to the monitor. Each of these steps is on part of a three stage pipeline, so while one character is being shifted to the monitor, the EPROM is looking up the pattern for the next character and the RAM is looking up the code for the character after the next.

2-65. ATTRIBUTES

In parallel with the character RAM, there is an attribute memory (U33) with one byte associated with each character cell on the screen. Attributes modify the appearance of the characters.

There are five user selectable attributes, each controlled by one of the bits in the attribute memory:

- Inverse – Black character on a white background
- Flashing – Character blinks on and off once per second
- Highlight – Brighter display
- Underline – A line is drawn under the character
- Opaque – The graphics image is inhibited

The underline position is fixed in the double-size PAL (U40) and the blink rate for flashing characters is software-controlled at pin 15 of U7.

The attributes are read at the same time as the corresponding character, and they keep step in the pipeline as they are latched in U43 and U55. While the bit pattern for a given character is shifting through the attribute PAL (U54), the associated attribute bits are present at the inputs to the PAL.

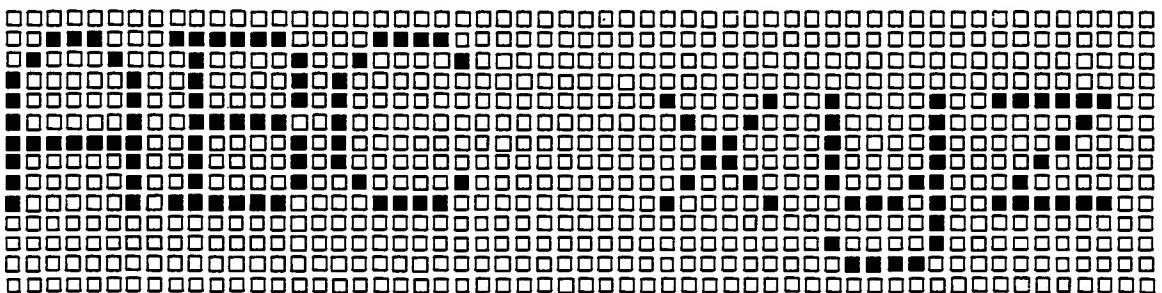
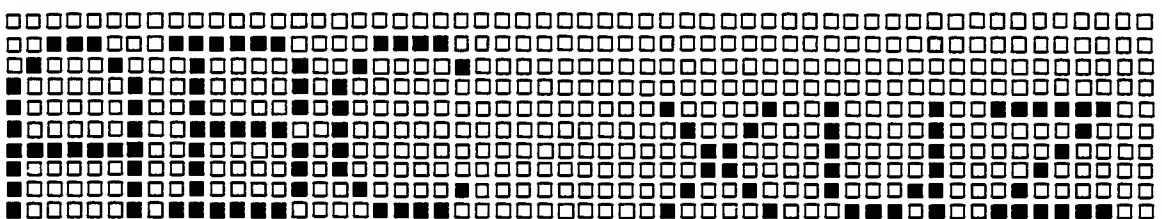
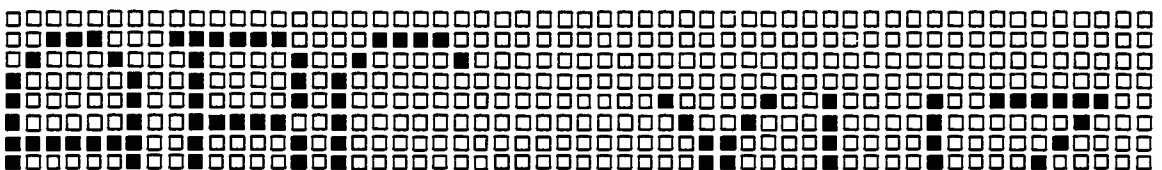
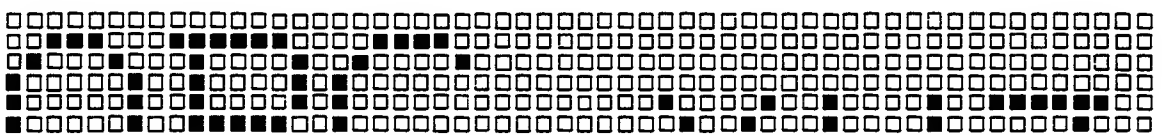
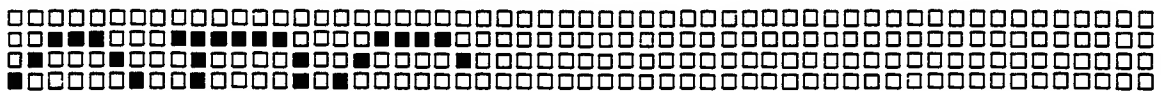
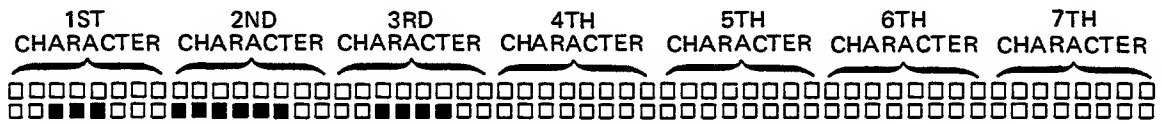


Figure 2-12. Character Row Display

THEORY OF OPERATION

VIDEO/GRAPHICS/KEYBOARD INTERFACE(VGK)

In addition to the five user-selectable attributes, there are two others which are used by the firmware. One bit is used to inhibit the first stage of the attribute pipeline from latching new data. This allows the attributes associated with one character to affect subsequent characters regardless of the actual values of their attributes. This is used to implement the field attribute mode which is explained in the 1722A System Guide.

The other firmware-controlled attribute is used in field attribute mode to inhibit the current visual attributes from affecting a given character. A character with this bit set is displayed normally even if attributes are applied to the field that it is in. This is used to force character graphics to be displayed without attributes, primarily for compatibility with the 1720A.

The attribute PAL combines the inputs shown in Table 2-7 to generate the video output for the VGK. This output is buffered by U100 and sent to the monitor through the brightness control, R6. Figure 2-13 shows the

combination of character and graphic images in the attribute PAL.

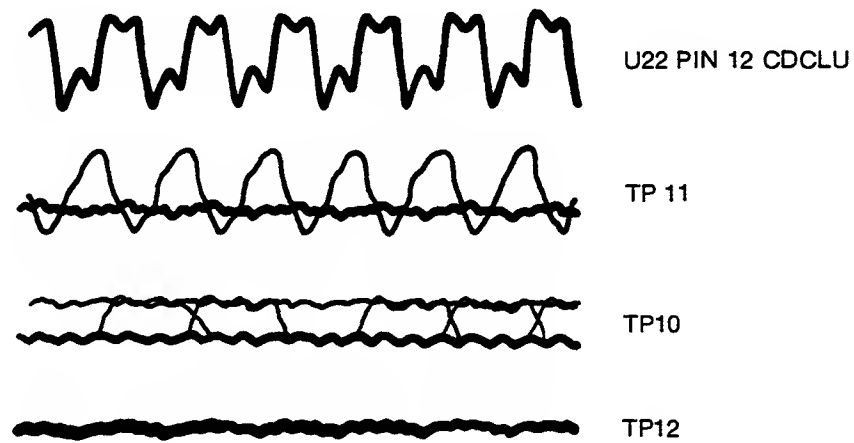
2-66. DOUBLE SIZE

Another feature of the display is that it can be converted to eight lines of 40 characters that are twice as high and twice as wide as normal characters. To double the height, the CRTC is programmed for 28 scan rows per character and the double-size PAL (U40) divides the row outputs (R0-R4) by two.

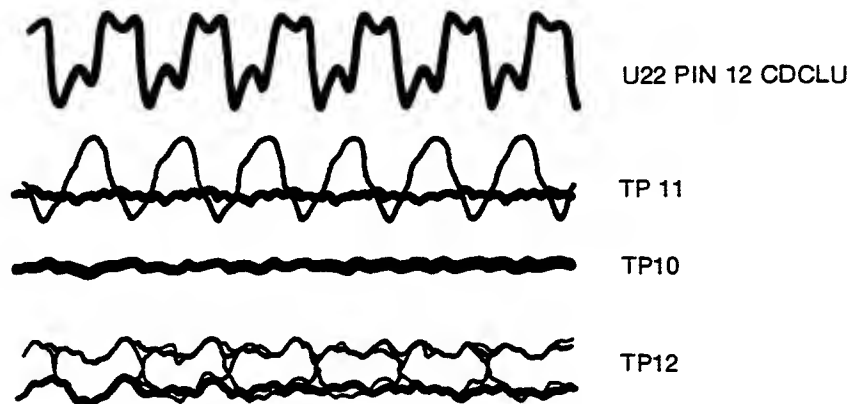
Double width is achieved by dividing the character dot clock, CDCLK, rate by two in the clock PAL (U22, pin 12), and loading the character shift register (U23) half as often. The load-enable pulses are qualified by the output of U57 (pin 6), which is forced high during normal-size but divides the character clock by two when DBLSZ is active. U57 is also used to enable the loading of the second stage attribute latch (U68) to double the width of the cursor.

Table 2-7. Attribute Inputs

INPUT	FUNCTION
CVID	Character Video: Bit pattern from shift register (U23) loaded from character-generating ROM (U32).
UNDER2	Underline Attribute: Active during one scan line of underlined character. This signal is ORed with the character bit pattern.
BLINK	Blink Attribute: Active during selected characters and when blink clock (BLCLK), a software-controlled bit, is active. Disables character and underline dots. Normally, the software toggles the blink clock at a steady rate, causing selected characters to flash.
REV	Reverse Video Attribute: Inverts the character images so the background is white and high bits are black.
HIGHT	Highlight Attribute: Inhibits modulation of the video signal to allow full intensity.
CUR2	Cursor: Active in only one character cell on the screen; selected by the value in the cursor register of the CRTC. Causes video image to be inverted. Normally this signal blinks at a slow rate to highlight the next location for character entry.
GVID	Graphics Video: Serial bit stream from Graphics memory. Normally ORed with modified character video.
OPAQUE	Opaque Attribute: Inhibits graphic image in selected character cell to avoid obliterating the text.
ATTREN	Attribute Enable: Simultaneously controls the four 1720A-compatible attributes: underline, blink, reverse video, and highlight. This is used to implement non-transparent attributes and to inhibit attributes on character graphics. This is only required for 1720A compatibility.
DCLK	Dot Clock: 50% duty cycle shift clock used to modulate the video output to provide normal intensity. Highlight is achieved by inhibiting this modulation.
DE2	Display Enable: Used to blank the screen during horizontal and vertical retrace.



A. CHARACTERS BUT NO GRAPHICS



B. GRAPHICS BUT NO CHARACTERS

Figure 2-13. Video Signals at Attribute PAL (U54)

2-67. COMPOSITE VIDEO OPTION

A phono plug is provided on the rear of the VGK to drive external monitors. This connector provides the composite video output, which is a combination of HSYNC, VSYNC, and VIDEO, according to an industry standard.

The basic timing of the sync signals comes from the CRT controller chip. The width and position of the pulses is programmed by the firmware. Several chips are required to combine the two sync pulses into CSYNC-. The general level of CSYNC- (U50, pin 9) follows VSYNC- (U9, pin 9). The set and reset pins on U50, however, are driven by the input and output of shift register U101, to insert pulses so that the falling edge of HSYNC- maintains a uniform spacing. The formation of CSYNC from HSYNC and VSYNC is illustrated by Figure 2-14.

2-68. CHARACTER-MEMORY ACCESS

The character memory can be accessed twice in the 627 ns character period. The screen refresh process loads a new character into the pipeline during the last half of this time. This allows the VGK microprocessor to update the memory during the first half of the character cycle. When CCLK (U22, pin 14) is low, the processor is allowed to access the character and attribute memories. This period is called the processor access window. When CCLK is high, the character address comes from the CRT

controller. The address bits are multiplexed between these two sources by U21, U39 and U44.

The character memory timing must be synchronized to the display, which means that the processor may be delayed. The timing is controlled by two flip flops from U4 and U17. Both flip flops are forced to a reset condition between processor memory cycles when WE- or DBIN- are high. When a read or write begins, C1 (U4, pin 5) is set high by the falling edge of CCLK, which marks the beginning of a processor access window. If the firmware is addressing a synchronized address, the address PAL brings the RDY line low to stall the TMS-9995. When C1 becomes active, the CHREN- line goes low to enable the transfer. The processor access window closes when the rising edge of CCLK causes C2 (U17, pin 5) to be set. With this, the address PAL deactivates CHREN- and raises the RDY line, allowing the processor to continue.

When the VGK microprocessor writes to the character RAM, U13 buffers the data. U27 latches the data that is read from the character RAM during the processor access window. The read data is latched because the processor does not actually receive the data until its READY line is high and the RAM has begun reading a character for the screen. U25 and U42 perform similar functions for accessing the attribute RAM. When data is written to the attribute RAM, U25 latches it. As an aid to the firmware, whenever a value is written to the character memory, the current attributes are stored in the corresponding location in the attribute RAM.

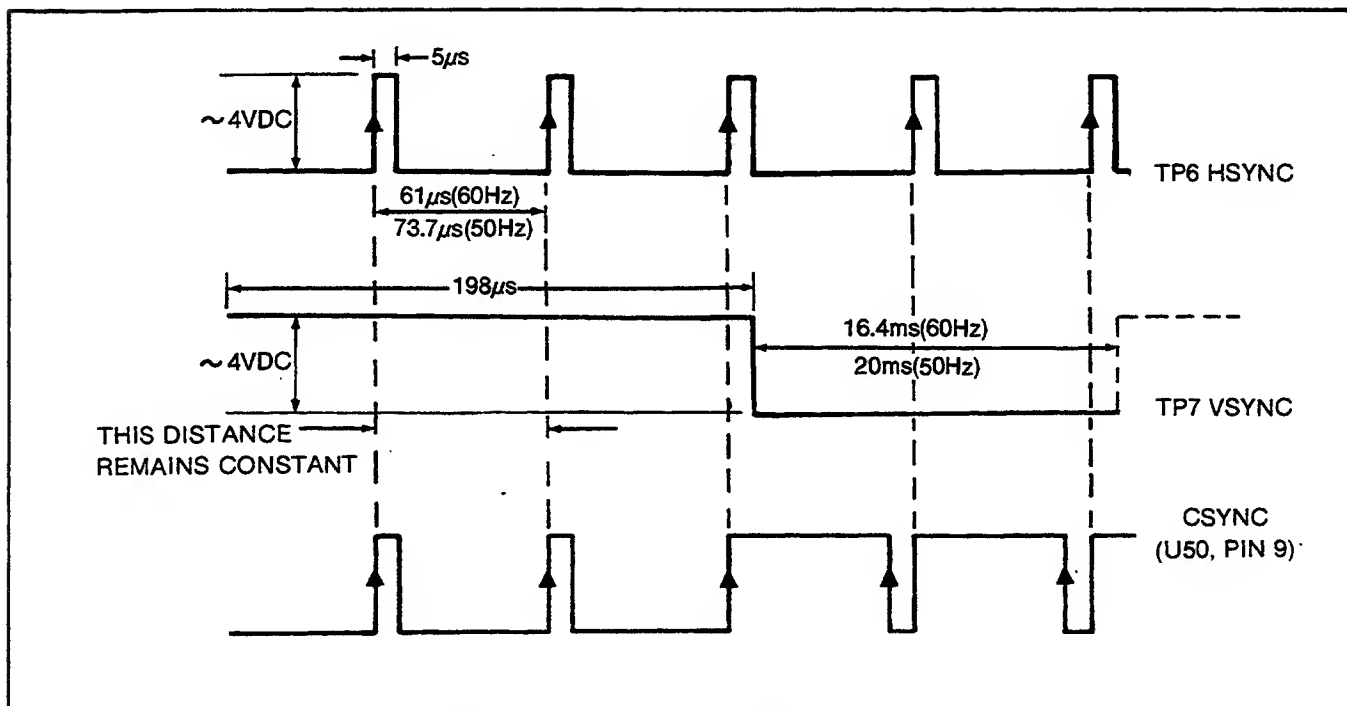


Figure 2-14. Horizontal and Vertical Sync Pulses

2-69. PROGRAMMING THE CRTC

To program the CRTC, the microprocessor writes to one of two eight-bit registers. The RS input (register select, pin 24, U31) determines which register is modified. To access the CRTC registers, the microprocessor writes to address F400 or F401. These addresses are decoded by the address PAL (U18) and cause a logic low on CRTCEN- (CRT controller enable) which is connected to the CS- (chip select, pin 25, U31) input on the CRTC. Writing to the CRT controller takes more time than accessing memory, so the address PAL stops the processor when one of the CRTC addresses is recognized. The timing of the access cycle is controlled by hardware, similar to that used to synchronize accesses to the character memory. The CRTCEN- signal enables a timing chain (U4 and U17) which activates the enable input (pin 23, U31) at the beginning of the next CLKOUT- cycle. One CLKOUT- cycle after that, the CRTCRDY is activated, which causes the address PAL to raise the READY signal, allowing the microprocessor to continue with the next instruction. This system guarantees that the CS- signal will precede the enable signal and that the enable will be active for the required time. A timing diagram of this sequence is shown in Figure 2-15.

2-70. Graphics Display

The VGK provides bit-addressable graphics over the 640-by-224 dot area of the screen. The graphic image is independent of the character display logic. The video bit stream from the graphics portion of the board is combined with the character image in the attribute PAL (U54) right before it is sent to the monitor.

The graphics subsection is divided into display logic and update logic. The display logic reads one byte from the graphics bit plane every character cycle (627 ns). This datum is loaded into a shift register (U75) and is sent to

the attribute PAL. The update logic is called the vector generator. This circuit writes to the graphics memory, one bit at a time, to draw straight lines of programmable length and direction. The VGK microprocessor must access the graphics memory through the vector generator. After this specialized logic is programmed, it can draw a line on the screen 10 times faster than the processor could without it.

2-71. GRAPHICS MEMORY TIMING

The dot clock frequency of 12.77 MHz is determined by the display requirements. The crystal oscillator runs at twice this rate to guarantee a 50% duty cycle on DCLK. The higher speed gives greater resolution to the clock PAL, which contains a four-bit state machine that generates system timing signals. A description of these signals is given in Table 2-8 and their relationship is shown in Figure 2-16.

The reset input to U22 is only used for automatic testing, which requires that the signals start from a known state. The DBLSZ input causes the CDCLK output to toggle at half the rate of the DCLK output when the double-size mode is selected.

2-72. DISPLAY ACCESS

To display characters on the screen, a set of counters step through the addresses of the bytes that are sent to the monitor. The X-axis counters, U80 and U82, are incremented by the character clock 80 times as the monitor scans a single row. They are reset to their initial value at the beginning of each new scan row. U53 and U67 are clocked by HSYNC- when the monitor steps down to a new line. These Y-axis counters are reset by VSYNC- when the display cycle starts over. Because the refresh counters are clocked and reset by signals developed in the character display logic, the two images remain synchronized.

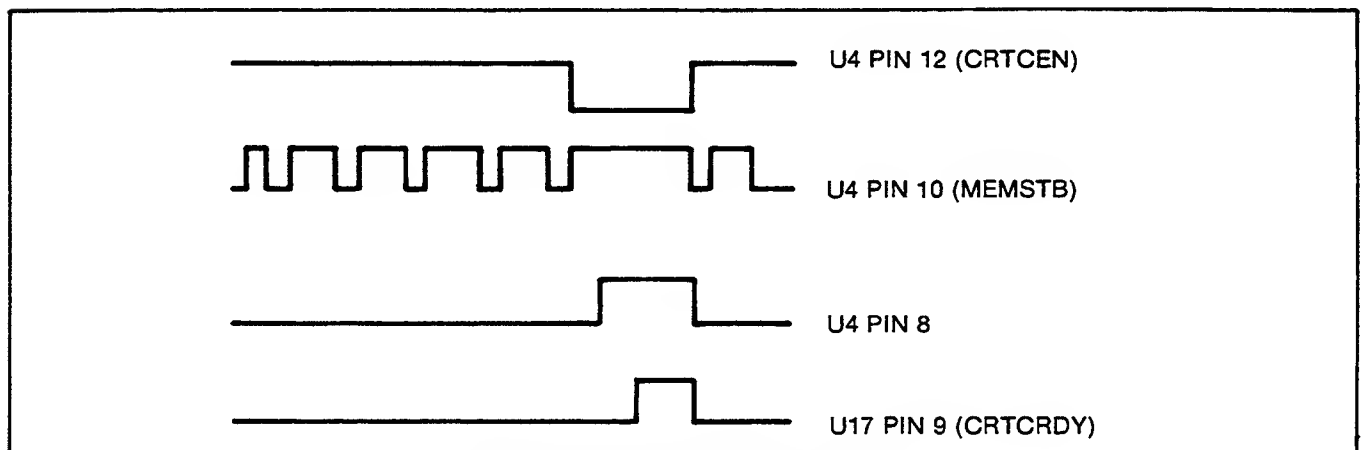


Figure 2-15. CRT Controller Timing

THEORY OF OPERATION

Table 2-8. System Clocks

SIGNAL	NAME	DESCRIPTION
DCLK	"Dot CLock"	50% duty cycle clock at the video frequency, used to clock the video shift registers, to modulate the video output for non-intensified character fields, and as the input frequency for the TMS-9995.
RAS	"Row Address Strobe"	Row Address Strobe for dynamic RAMs.
R/C-	"Ras select"	Used to multiplex the pixel address into the dynamic graphics memory. High when row address are selected and low when column addresses are selected.
VCLK	"Vector CLock"	Toggles at half the rate of R/C- to select between access by vector generator and the graphics display update counters. Also used to develop the load signals.
CAS	"Column Address Strobe"	Column Address Strobe for dynamic RAMs. Inactive edge marks the end of a RAM memory cycle for both character and graphics RAMs.
CCLK	"Character CLock"	Toggles at half the rate of CAS (slaved to VCLK) to select between access by the microprocessor and the character display update address. It is used to clock the vector generator and the graphics display horizontal counter.

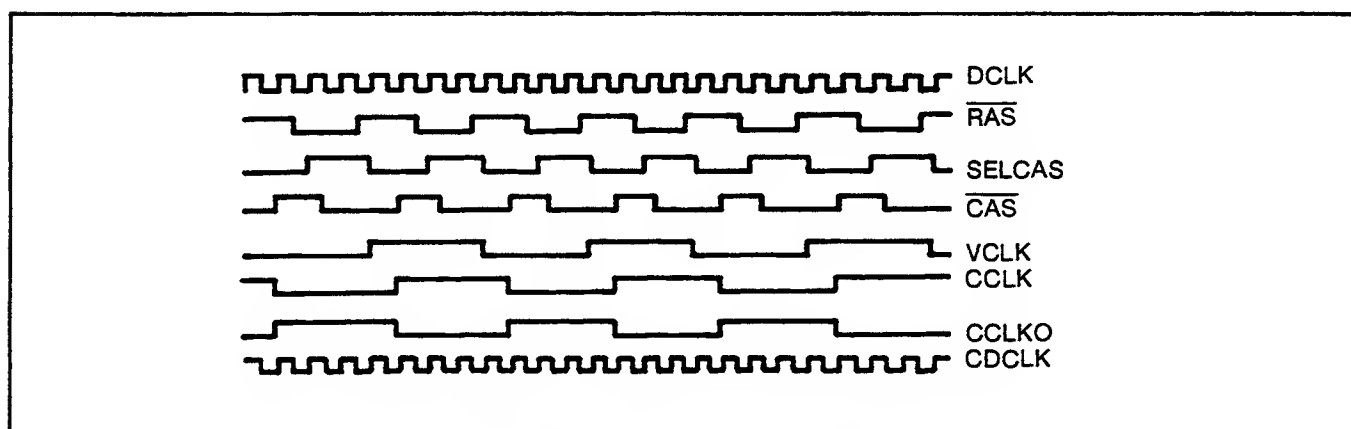


Figure 2-16. System Timing Outputs of Clock PAL (U22)

The graphics memory is about three times bigger than required to fill the screen with dots. The image on the display is a 224-by-640 bit window into a 256-by-2048 bit memory. The application software can move this window within the memory by sending a command to the VGK. The command establishes the initial values of the refresh counters. The initial values are stored in the PAN registers.

The value in the X-PAN register (U81) is copied into the X-axis refresh counters (U80 and U82) by HSYNC- at the beginning of every line. This eight-bit value determines the address of the column of bytes in the graphics memory that is to be displayed on the left edge of the screen. Increasing the value in the X-PAN register by one shifts the image on the display eight dots to the left. The value in

the Y-PAN register (U66) is loaded into the Y-axis refresh counters (U53, U67) by VSYNC- at the beginning the frame. This value determines the address of the row of bits that is displayed on the top edge of the screen. Adding one to the Y-PAN register moves the image up one scan row.

As with the character memory, the graphics memory has two sources. The first is the refresh counters. The second comes from the vector generator. Each address is applied to the memory chips for half of the character cycle. Four selector chips (U69, U79, U94, and U97) are used to choose one of the two addresses and to multiplex the row and column addresses into the DRAMs. Figure 2-17 shows that every other DRAM read is for display refresh.

The graphics memory consists of eight 64K-by-1 dynamic RAMs. The refresh requirements of the dynamic RAM

are satisfied by the display refresh counters. The arrangement of the inputs to the address multiplexer guarantees that all 256 internal rows will be accessed every 2 ms with any value in the pan registers.

2-73. VECTOR GENERATOR

Graphic dots are displayed on the CRT when the corresponding bits in the graphics memory are set to 1. The vector generator calculates the addresses of visually adjacent dots and writes to the graphics memory. It consists of address counters and logic to enable them, and logic to control the write enable and chip enable of the DRAMs.

To form a line on the screen, the VGK loads the starting horizontal position into the X counter (U52, U91, U93) and the vertical position into the Y counter (U84, U83). Next, a binary fraction representing the slope is loaded into the slope register (U72 and U92).

To start the process, the length of the line in dots is loaded into the count register (U85, U99). To prevent changes to the address inputs when they should be stable, all accesses the the vector generator registers are synchronized to the character clock, as with the character and attribute memories.

While the value of the count is non-zero, one dot is written onto the graphics memory during each complete memory cycle. Lines are drawn at the maximum memory speed of one dot every 627 ns (1.6 million dots per second).

With each dot, one or both of the X and Y counters is changed by 1, and the count register is decremented. When the count reaches zero, the carry out of the counter (U85, pin 15) becomes active, and the process stops. The carry-out line is called VBUSY and may be read by the microprocessor. The software is not allowed to change

the contents of the registers while the vector generator is busy.

The path traced by the line is determined by two bits, XUP and YUP, which program the X and Y counters to count up or down. The XYTRAN line selects which of X or Y will change with every clock pulse, leaving the other counter to change when it is enabled by the slope control logic. For example, if the X counter is programmed to count up and the Y counter is programmed to count down, then the resulting line will grow up and to the right. Note that the hardware places the 0,0 bit in the upper-left corner of the screen, although the software converts incoming data to place it in the lower-left corner.

If the X counter increments every cycle, and the Y counter never changes, the resulting line is horizontal. If both counters change, the line is diagonal. If the Y counter changes less often than the X counter, the line's horizontal component is greater than its vertical component. Lines of this type are called X-major lines and are enabled when XYTRAN = 0. When Y-major lines (XTRAN = 1) are drawn, the Y counter changes during every cycle and the X counter changes equally or less often.

The slope accumulator determines when the minor counter is enabled to change. While the vector generator is running, the rising edge of CCLK causes the value in the slope register (U72, U92) to be added (by U86, U88, U95) to the value in the slope accumulator (U87, U97). The slope register contains the fraction that represents the change in the minor counter divided by the change in the major counter. When adding the fractional slope to the accumulated value results in a carry (U86, pin 10), the minor counter is enabled to change. If, for example, the slope register contains the value 0.25, there will be a carry pulse every fourth clock cycle and the resulting line will take one step up for every four steps to the right (assuming XTRAN=0, XUP=1, YUP=0).

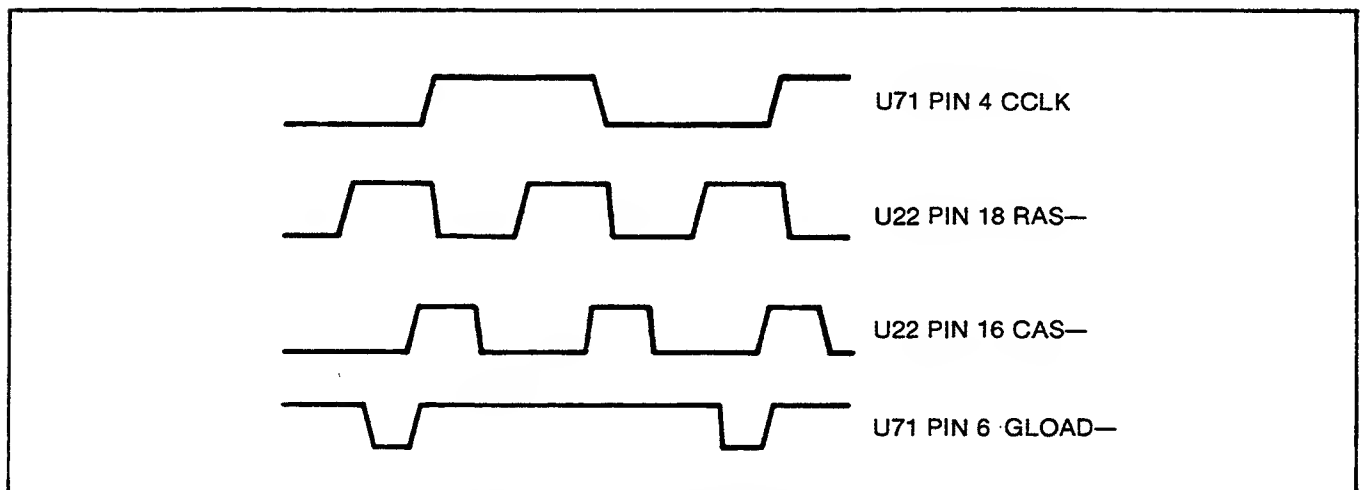


Figure 2-17. Graphics Refresh Timing

THEORY OF OPERATION

KEYBOARD

The address of each dot in the graphics memory is composed of eight bits from the Y counters and 11 bits from the X counter. The Y address and the upper eight bits of the X address are sent to each device through the row/column multiplexer (U69, U94, U94, U97). The lower three bits of the X address are used to select one of the eight memory devices. While writing to one of the memory chips, the data is presented to all eight but only one write-enable (WE) is activated by U77. All unselected memories perform a dummy read cycle.

2-74. UPDATE MODE

The graphics memory read/write logic allows the graphic image to be modified in several ways. Two shift registers are used to convert the bit-oriented graphics memory to a byte-oriented device seen by the VGK microprocessor. The output shift register (U90) collects one bit from the graphics memory during each vector access cycle. The microprocessor can read the contents of this register by enabling the associated bus buffer (U89). The data that modifies the contents of the graphics memory is loaded into the input shift register (U73). The contents is shifted following every write cycle. The shift output is connected to the shift input to allow patterns that repeat in eight cycles to be loaded only once.

Graphics memory modification modes are shown in Table 2-9. The affect of the vector generator on the graphics memory is determined by the update mode. The value written to the memory is affected by:

- the input shift register (U73, pin 9);
- the last bit read from the memory which is stored in the output shift register (U90, pin 3); and
- the current mode established by M1 and M2.

Table 2-9. Graphics Memory Modification Modes

M2	M1	MODE	PREVIOUS VALUE, INPUT BIT			
			0,0	0,1	1,1	1,0
0	0	NEW	0(w)	1(W)	1(w)	0(W)
0	1	OR	0	1(W)	1(w)	1
1	0	AND	0(w)	0	1	0(W)
1	1	XOR	0	1(W)	0(W)	1

KEY:

⟨W⟩ indicates that a new value was written.

(w) indicates that the existing value was rewritten.

When the contents of the input register are to be transferred directly to the graphics memory, a write operation is performed during every cycle. When the new

data is to be ORed with the present image, it is only necessary to write when the new data is high. Similarly, only 0 bits need be written to form the AND result. Finally, no write operation is required when a 0 bit is XORed with the existing value. Using this method, the only time that the present contents of the cell are needed is when it is toggled by XORing with a logic 1. In this case, updates to the screen are preceded by reading the existing bit at the calculated address. This read-before-write is controlled by a circuit (U50 and U47) which inhibits the vector generator from advancing on alternate cycles.

2-75. PROCESSOR ACCESS TO GRAPHICS MEMORY

All access to the graphics memory by the VGK microprocessor involves the vector generator. To write a byte to a specific location, the data is loaded into the input shift register (U73) and a horizontal line, eight dots long, is drawn from the appropriate starting point. A similar provision is made for reading the graphics memory.

Selector U76 collects the output bit from the currently addressed DRAM and directs it to the output shift register (U90). To read a specific byte from the graphics memory, the processor fills the input shift register with 1's and selects the AND mode so that no chips will be write-enabled. The vector generator is then programmed to "draw" a line, eight dots long, beginning at the desired address. Eight clock cycles later, the vector generator stops and the output shift register contains the desired datum. Note that the byte boundaries imposed by the hardware are irrelevant.

2-76. KEYBOARD THEORY OF OPERATION

2-77. Introduction

The 1722A serial keyboard (Model Y1700) uses the Intel 8048 Family Microcomputer. The hardware and firmware were designed to allow use of the same architecture on all 1722A keyboard options.

The keyboard communicates directly with the VGK. Characters received by the VGK are passed on to the SBC, which echoes printable characters back to the VGK for display on the CRT.

2-78. Operation

2-79. POWER-UP SEQUENCE

On power-up, and every 175 scans of the key matrix, the states of the left-shift and control keys are sampled and transmitted to the VGK. The natural state of these keys is open. A 1-second lamp test is executed along with a beep.

2-80. SCANNING

The Keyboard Microcomputer (U1) scans from column 15 to 0. The column address is sent to the decoder (U2),

which grounds one side of a column of keys. The Microcomputer then reads the data bus to find key closures as logic 0 and computes the row number. The key address is formed using the row and column number. If one key is closed for four scans, the UART routine is called to transmit the key address. If the key remains closed until the pause counter underflows, the key is re-transmitted once every sixteen scans until it is released.

If more than one key is pressed, the scanning process cycles until only one remains pressed.

2-81. COMMUNICATION PROTOCOL

The serial information is transmitted between a software-implemented UART in the Keyboard Microcomputer (U1) and a hardware UART (U36), on the VGK. When the VGK UART receives a key address from the keyboard, it generates an interrupt, informing the VGK Microprocessor (U30) that the data is available. Since the keyboard firmware does not use interrupts, it must check the TO KB line every pass through the main program loop to see if a break condition (logic 0) exists. If it does, the VGK has a command to send the keyboard. The keyboard waits in its UART routine for the break to clear and samples for data bits after detecting a start bit. If the break does not clear within a fixed time, the keyboard will start the next scan.

2-82. DATA TRANSMISSION FORMAT

The key addresses and commands use the following format:

- One start bit
- Eight data bits
- One stop bit
- 1200 baud
- Signal lines = FROM KB and TO KB
- Space = Logic 0 = 0V dc
- Mark = Logic 1 = 5V dc

2-83. LED CONTROL

The LEDs are driven by latch U3 as controlled by commands from the VGK.

2-84. TRANSDUCER (BEEPER) CONTROL

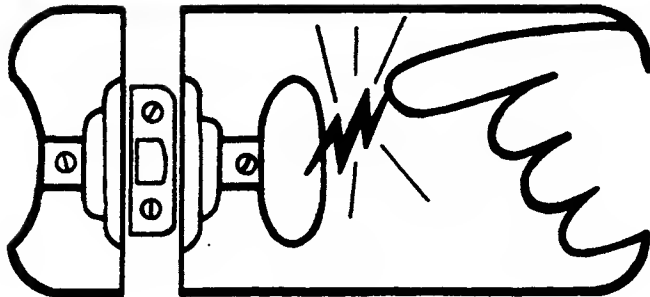
During the power-up lamp test, the audible transducer emits a 250 ms beep at 500 Hz. Tactile feedback for keystrokes is a 4 ms "click" at 1500 Hz. The VGK sends a command to disable the "click" when parts of the keyboard are "locked out" under user program control.



static awareness



A Message From
John Fluke Mfg. Co., Inc.



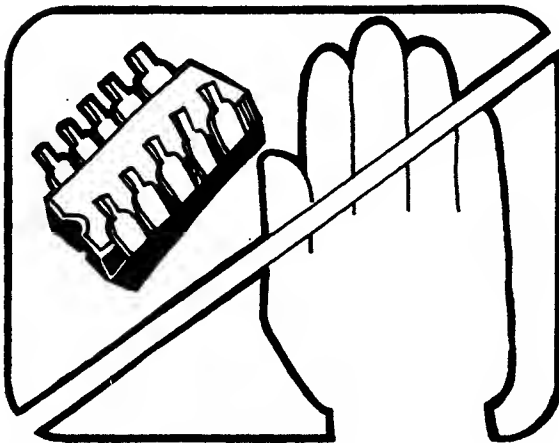
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

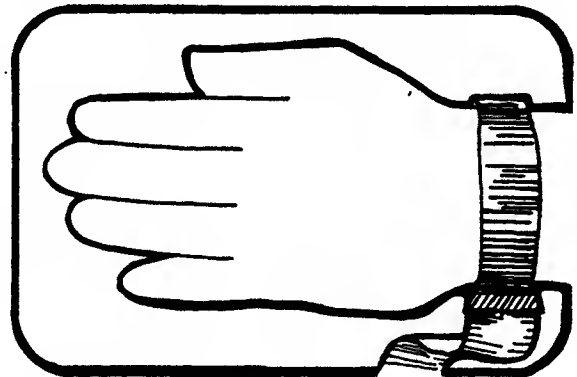
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol



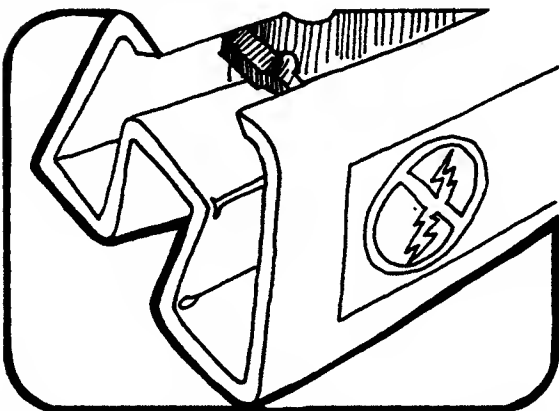
The following practices should be followed to minimize damage to S.S. devices.



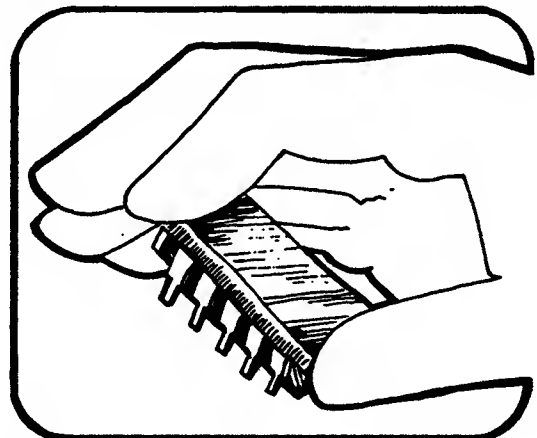
1. MINIMIZE HANDLING



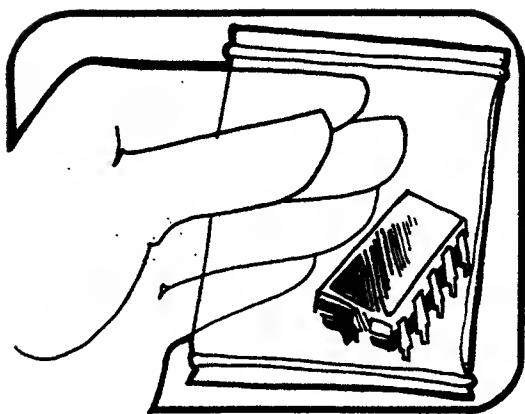
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



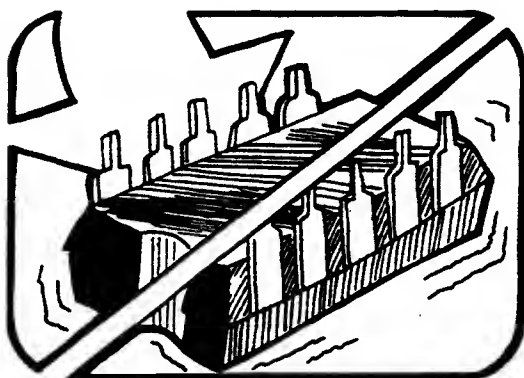
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



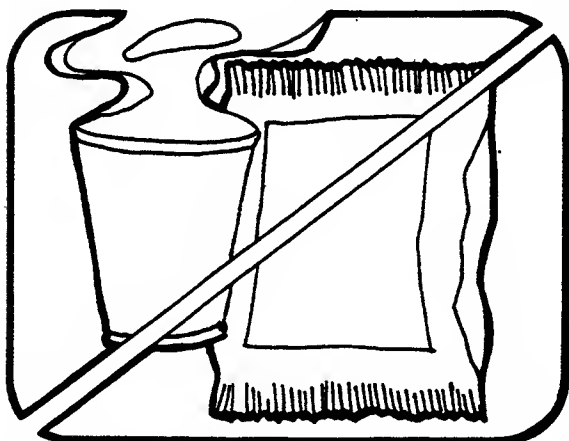
4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT

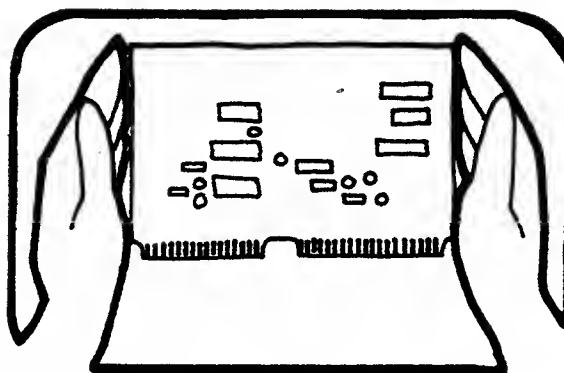


6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE

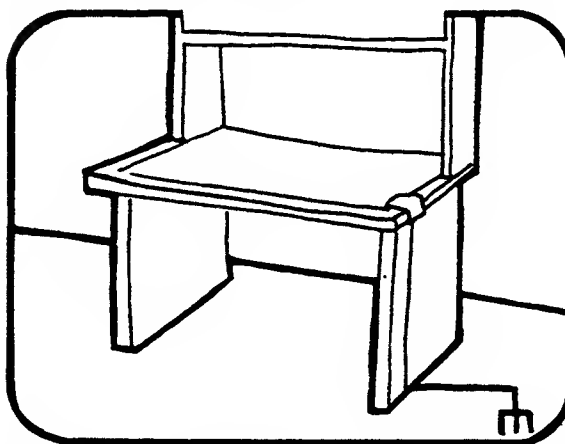


7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

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8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

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PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

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WARNING

THESE SERVICE INSTRUCTIONS ARE FOR USE BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

3-1. INTRODUCTION

The 1722A Controller has a modular design that minimizes down time by allowing the user to diagnose problems using System Diagnostic software. The diagnostics presented in this section have four parts: System Diagnostic Software, Dead Box Procedure, Board Isolation Procedure, and Fault Analysis. The Dead Box Procedure, Board Isolation Procedure, and Fault Analysis are contained under the heading Troubleshooting. Refer to Section 6 for Troubleshooting information for the 1722A and 1752A options.

The System Diagnostic software can usually narrow down the failure to one of the replaceable modules. The user can quickly determine whether the software or the hardware is at fault in any given problem by running the System Diagnostic software. If the system goes through the System Diagnostic without any failures, then the problem may be caused by other software. The Dead Box Procedure is a troubleshooting aid used when the System Diagnostic software will not run. The Board Isolation Procedure is used when neither System Diagnostic nor the Dead Box Procedure will isolate the faulty circuit board. The Fault Analysis discussion is used to isolate problems to a group of components. Component-level troubleshooting is recommended only when it is not possible to replace a defective module. The Access Procedures that follow the Fault Analysis describe how to remove and replace the faulty module. The Calibration and Alignment Procedures describe how to adjust the various subsystems for periodic maintenance or after repair. The final portion of this section is the Preventive Maintenance Program, which details the periodic actions necessary to maintain optimum performance.

For quick reference, the flow chart in Figure 3-1 presents an overview of the troubleshooting information in this section. A flow chart for the Dead Box Procedure is shown in Figure 3-2.

3-2. Required Tools and Equipment

Required equipment is listed in Table 3-1. If the recommended models are not available, equipment with equivalent specifications may be used.

3-3. SYSTEM DIAGNOSTIC SOFTWARE**3-4. Introduction**

The following paragraphs cover the operation of the System Diagnostic software and assist the user in diagnosing problems with the 1722A Instrument Controller.

The System Diagnostic (SD) software is provided on a floppy disk and is designed to be a customer, manufacturing, and field service tool. Successful completion of testing the 1722A using the System Diagnostic software gives the user confidence that the 1722A Instrument Controller is operating properly.

The 1722A and 1752A use a common diagnostic disk. Standard tests are selected automatically when you enter the System Diagnostic program. However, the -010 option test is not selected. Since the 1752A is supplied with a -010 assembly, the user must specifically select the -010 tests. There are additional performance tests for other 1752A-specific options (see Section 6.)

3-5. MAINTENANCE PHILOSOPHY

The maintenance philosophy for field-service repair is at the module level, including the SBC, VGK, video electronics, power supply, floppy disk drive, and the options. Faulty modules are identified by using the System Diagnostic software.

Replacement modules are available through your local Fluke Service Center. See Table 4-1 for a list of replacement modules. Contact your Service Center for details on in-warranty and out-of-warranty repairs.

3-6. DIAGNOSTIC DESIGN

The System Diagnostic software uses a menu system that presents the 1722A as a set of modules. A module is either a circuit board, an externally connected peripheral, or a major subsystem. There is a set of subtests for each module. Each subtest covers one specific function of a module. The test selections are presented on the 1722A display and use touch-sensitive command blocks for making choices.

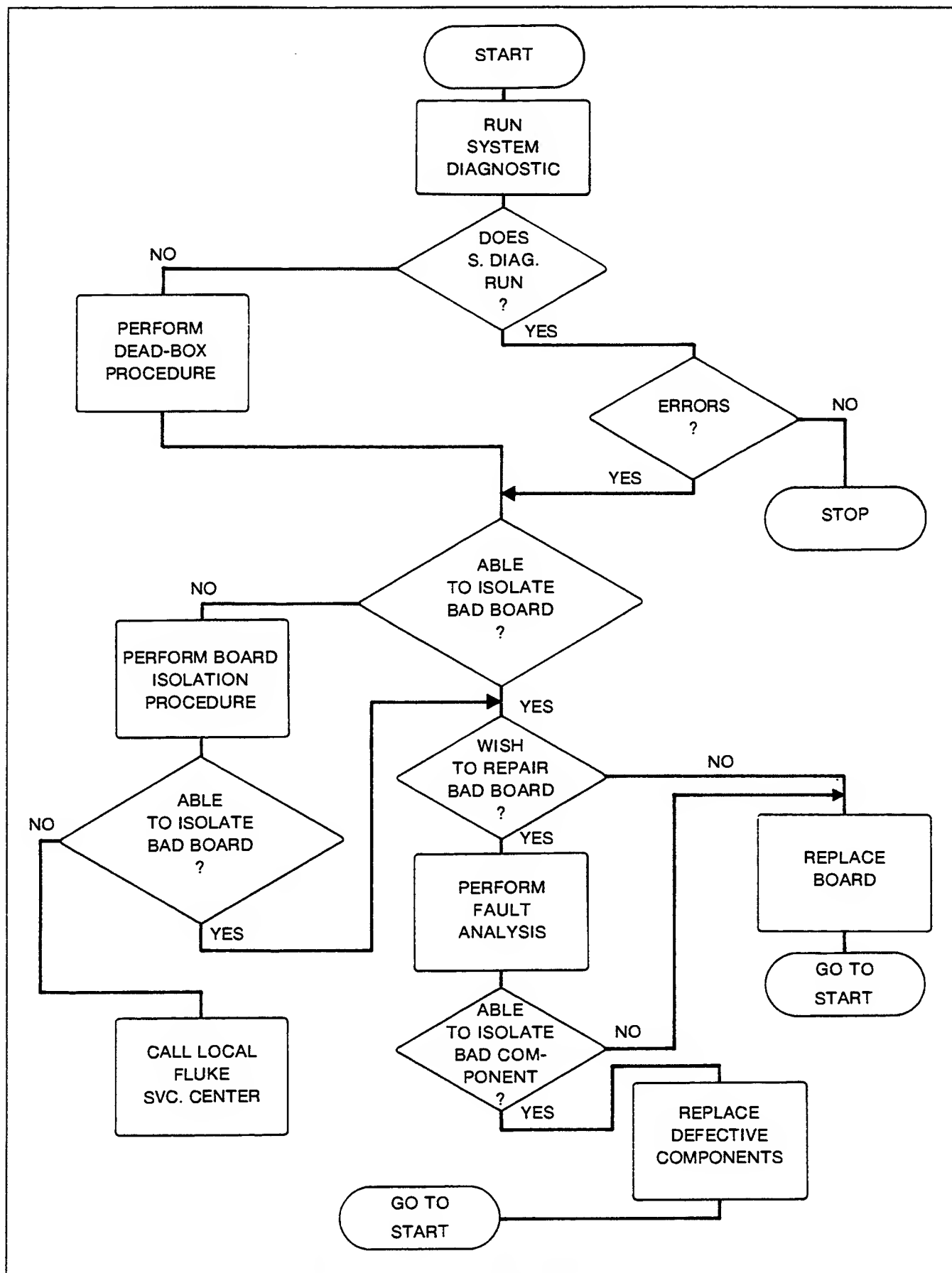
The menu system allows individual modules to be selected and tested. A particular combination of tests is called a test configuration. The Standard Test Configuration can be used to test a standard 1722A with no options installed. Other test configurations can be created, edited, stored, and recalled as Configurations A, B, and C.

Some module tests can cover up to five units (modules of the same type). For example, the test for the 512K byte Memory Expansion module (Option -007) can test from one to five modules.

3-7. MENU LEVELS

The diagnostic software has three menu levels:

- The Main Menu presents the test configurations, test modes, and a destination for the test results.
- The Test Menu presents the modules and options that can be selected for testing.
- The Subtest Menu presents the subtests that can be selected for each module and option.



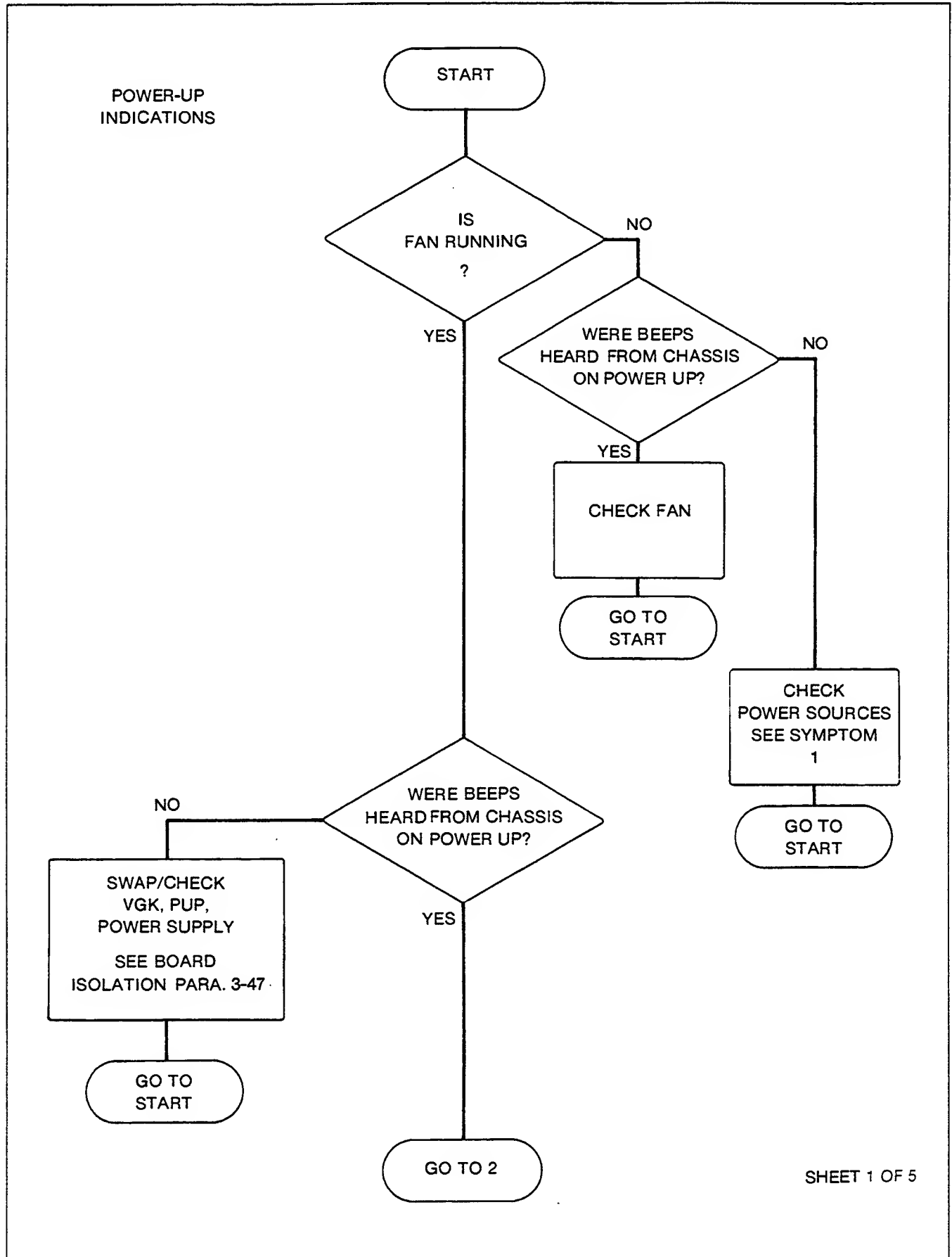
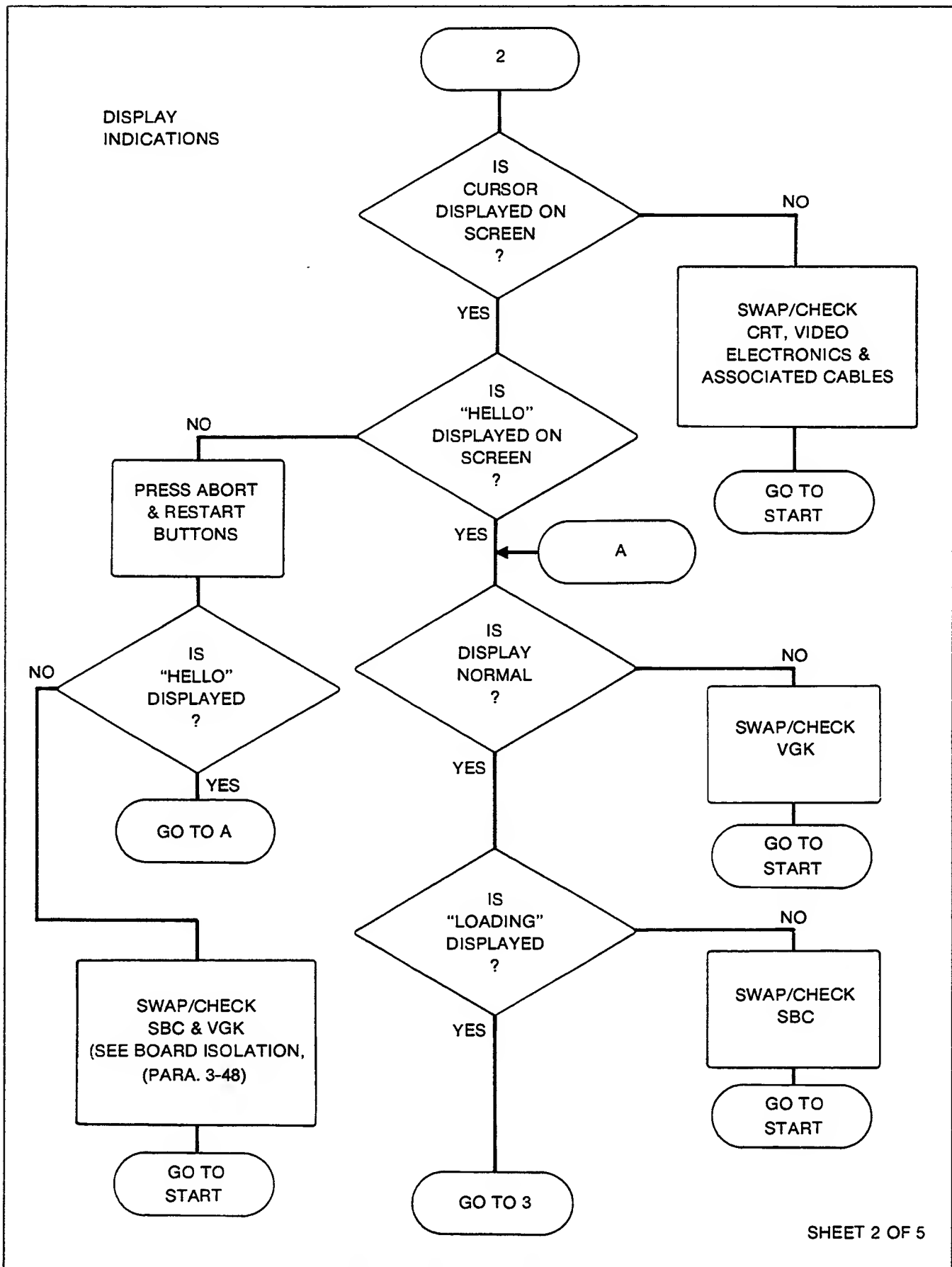
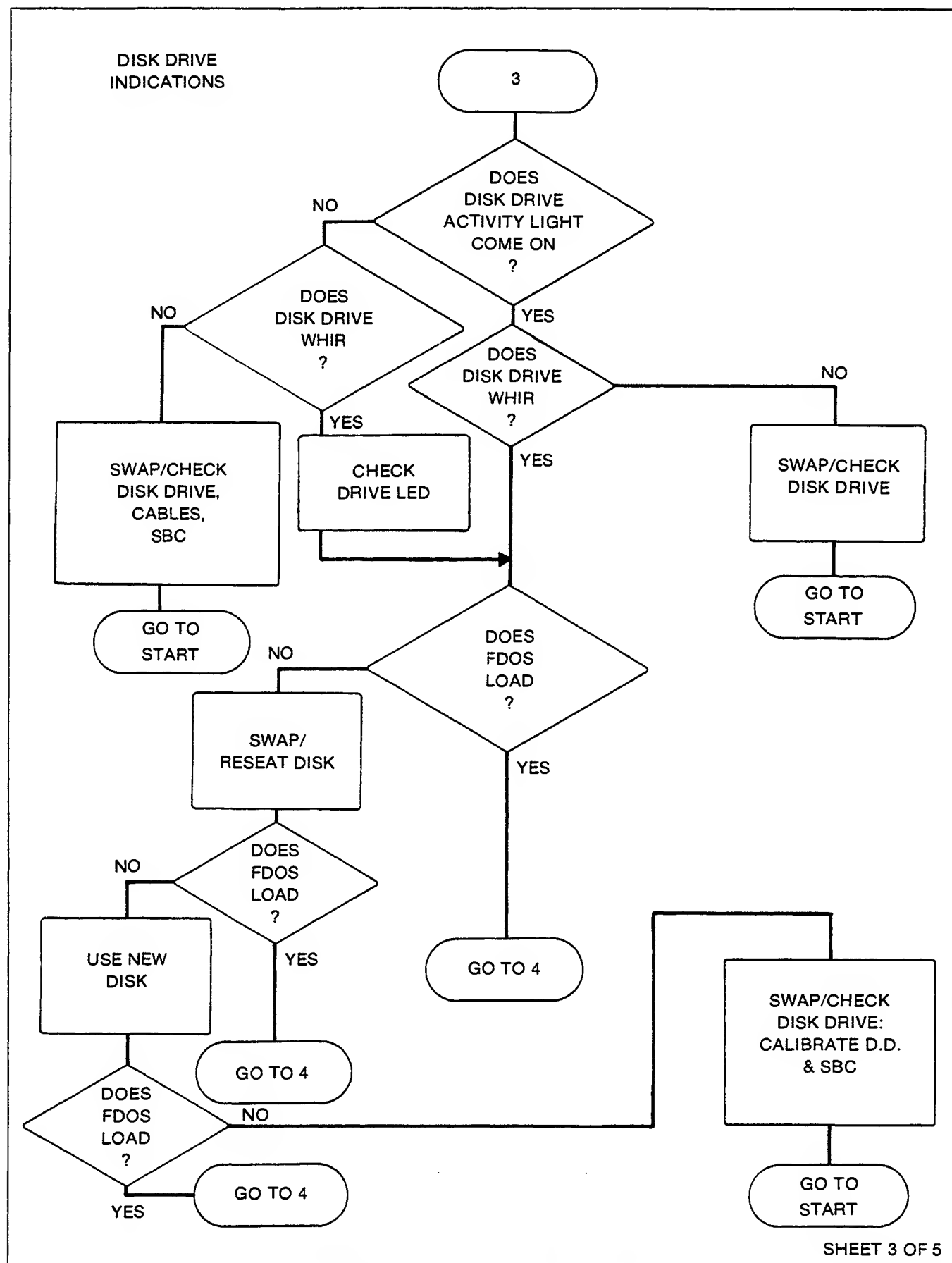


Figure 3-2. Dead Box Procedure

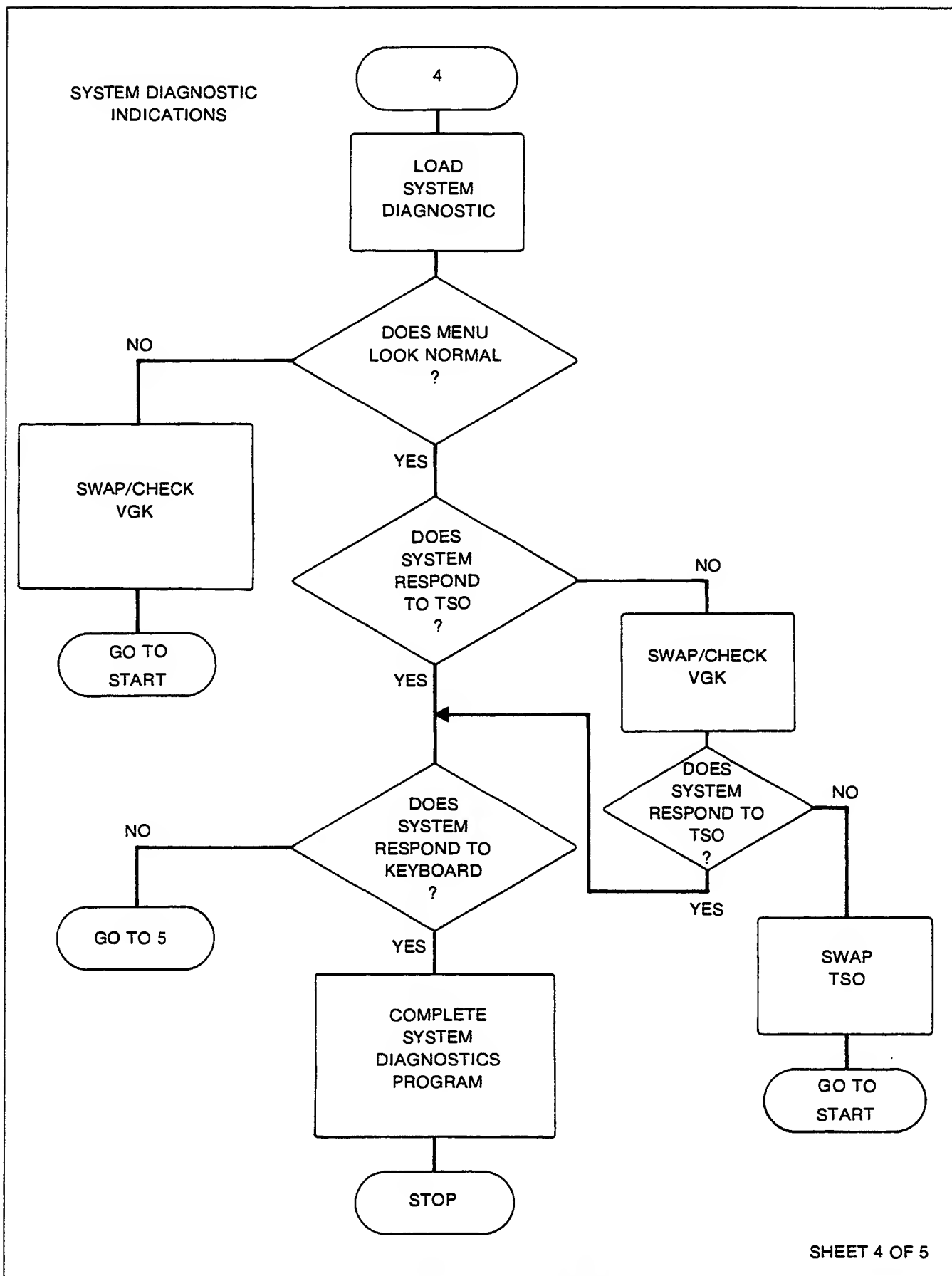


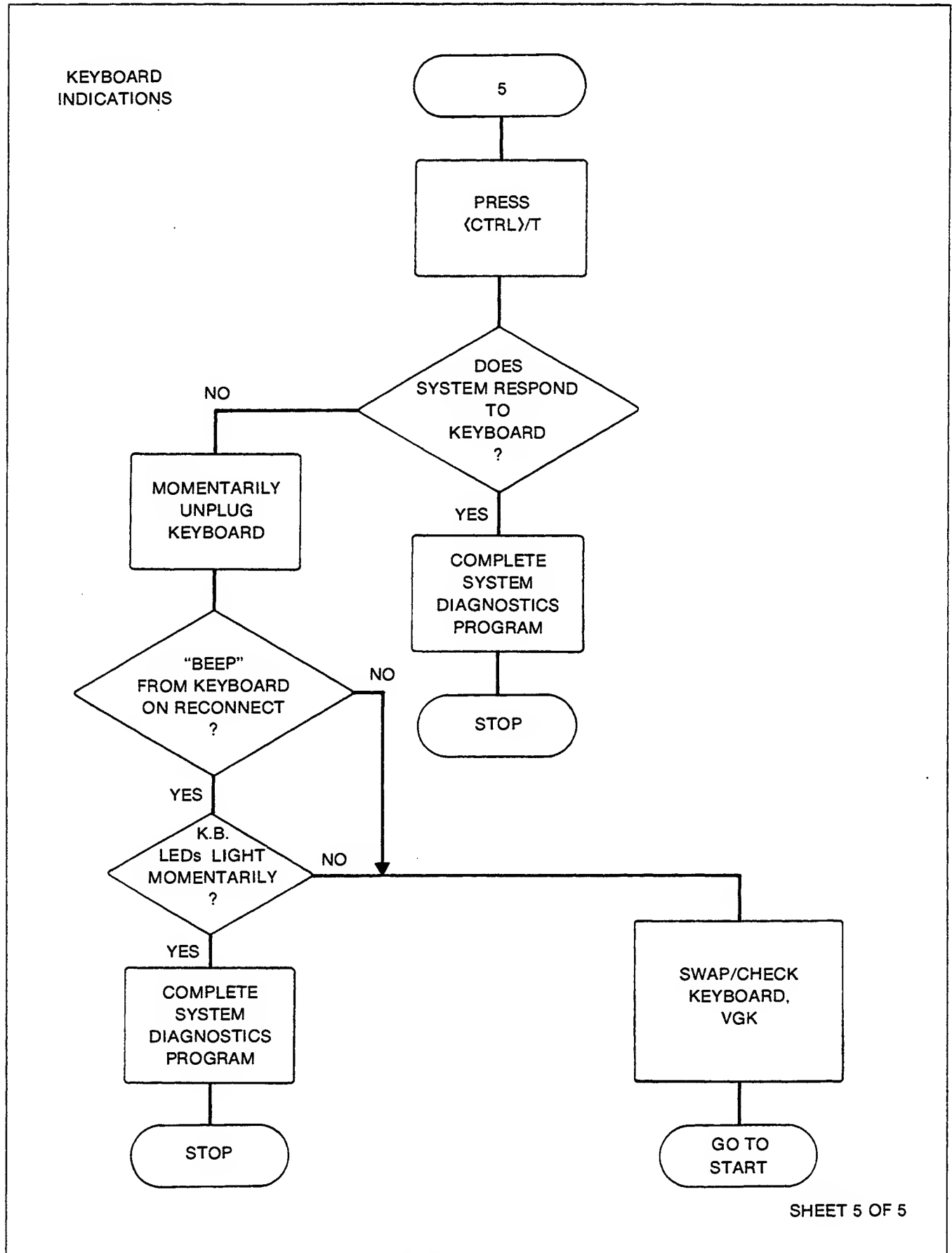
SHEET 2 OF 5



SHEET 3 OF 5

Figure 3-2. Dead Box Procedure (cont)





SHEET 5 OF 5

Figure 3-2. Dead Box Procedure (cont)

Table 3-1. Required Equipment

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
DC Calibrator	Fluke 343A	Used in 1752A subtests only.
Digital Multimeter	Fluke 77	
5 1/2 Digit Digital Multimeter	Fluke 8840	Used in 1752A subtests only.
Dual Trace Oscilloscope	Philips PM3065 100 MHz or equivalent	
IEEE-488 Interface Cable	Fluke Y8021	Connect IEEE-488 ports together.
RS-232-C Null-Modem	Fluke Y1705	Connect RS-232-C ports together.
RS-232 Loopback Connector	Fluke P/N 732107	Connector for RS-232-C External Loop Test.
DSI Test Cable	Fluke P/N 754648	Test Cable for Option 17XXA-009.
Solar Cell Board	Fluke P/N 765206	Used in 1752A-010 subtests only.
Line Sync Transformer	Fluke Y1752	Used in 1752A-010 subtests only.
Terminal Block with Cable	Fluke Y1750	Used in 1752A subtests only.
Screw Terminal Block	Fluke Option 2400A-110	Used in 1752A-011 subtests only.
1722A/1752A System Diagnostic Disk	Fluke P/N 718080	See "System Diagnostic Software" heading for instructions on ordering.
IEEE-488 Interface Cable	Fluke Y8021	Connect IEEE-488 ports together.
RS-232-C Null-Modem	Fluke Y1705	Connect RS-232-C ports together.
System Diagnostic Disk	Fluke P/N 718080	See "System Diagnostic Software" heading for instructions on ordering.
Alignment Tool	Fluke P/N 572321	
Gauge	Fluke P/N 535864	
Jumpers (2)		10-inch, alligator.
5-Inch #2 Phillips Screwdriver		
5-Inch Slot Screwdriver		
IC Pin Adapters		For connecting scope probes.
Logic Probe		
NOTE		
The following equipment is needed to replace the CRT Assembly or the Touch-Sensitive Overlay.		

The menu level diagram is shown in Figure 3-3.

NOTE

Copy any programs stored in the 1722A E-Disk onto a floppy disk before loading the System Diagnostic software. When the System Diagnostic software is loaded into the 1722A memory, portions of the E-Disk and program memory in the 1722A are erased.

3-8. OPERATION

Use the following procedure to run the System Diagnostic software:

1. Insert the System Diagnostic disk into the disk drive. Power up the 1722A, or press the RESTART and ABORT switches on the front panel simultaneously if the 1722A is already running.
2. After the System Diagnostic software is loaded from the floppy disk, the 1722A display reads as shown in Figure 3-4.

Table 3-1. Required Equipment (cont)

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
9-Inch Slot Screwdriver		1/4-inch blade, plastic handle at least 3 inches long.
Carbon Resistor		1 k Ω , 1/2 watt.
Two clip leads		Approximately 5 inches long, with alligator clips.
Safety gloves		
Full Face Shield (preferred) or Safety Goggles		
Long-Sleeved Jacket		
Work Bench or Table		Should be large enough to accommodate the 1722A when laid flat and still leave enough room on either side to allow work on the Front Panel assembly.
Soft Pad (foam or quilted)		Approximately 8 x 11 inches (to place the CRT on).
Plastic Screwdriver		At least 9-inches long, 1/4-inch tip approximate. Should be as rigid as possible to resist twisting during adjustment.

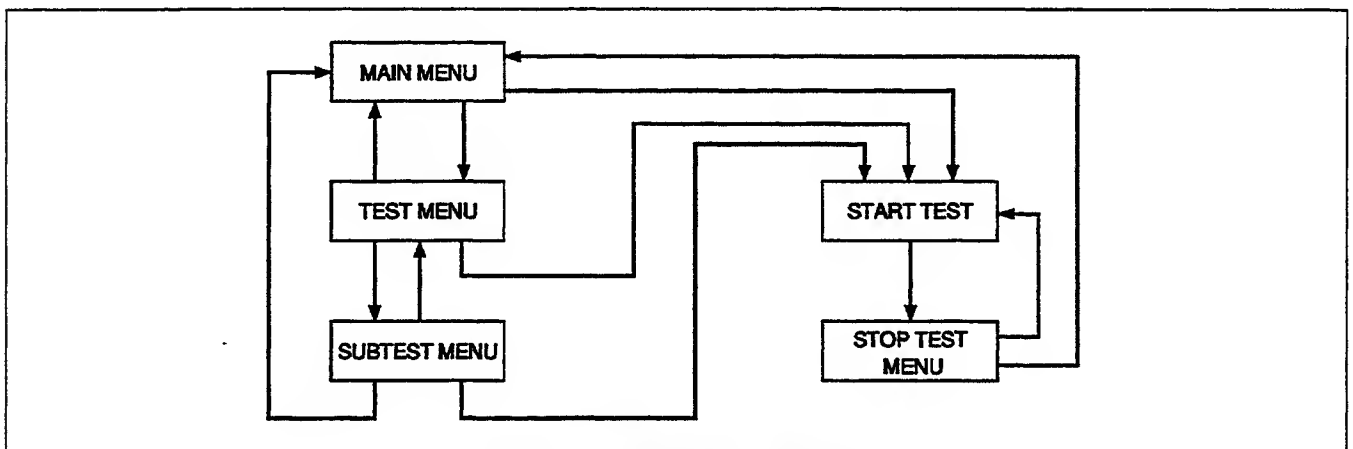


Figure 3-3. Menu Level Diagram

3. Touch the START TEST command block on the display to execute the Standard Test Configuration or select individual tests as described in the paragraphs below. Selecting an option that is not installed will result in the error message: Option faulty, missing, or improperly configured.
4. The test stops and displays a prompt at any point where a user response is required. At the end of the test, the results are displayed on the screen.

NOTE

If any problems are encountered while loading the System Diagnostic software or during the execution of a test, refer to the Dead Box Procedure.

3-9. Main Menu

The Main Menu has 11 command blocks:

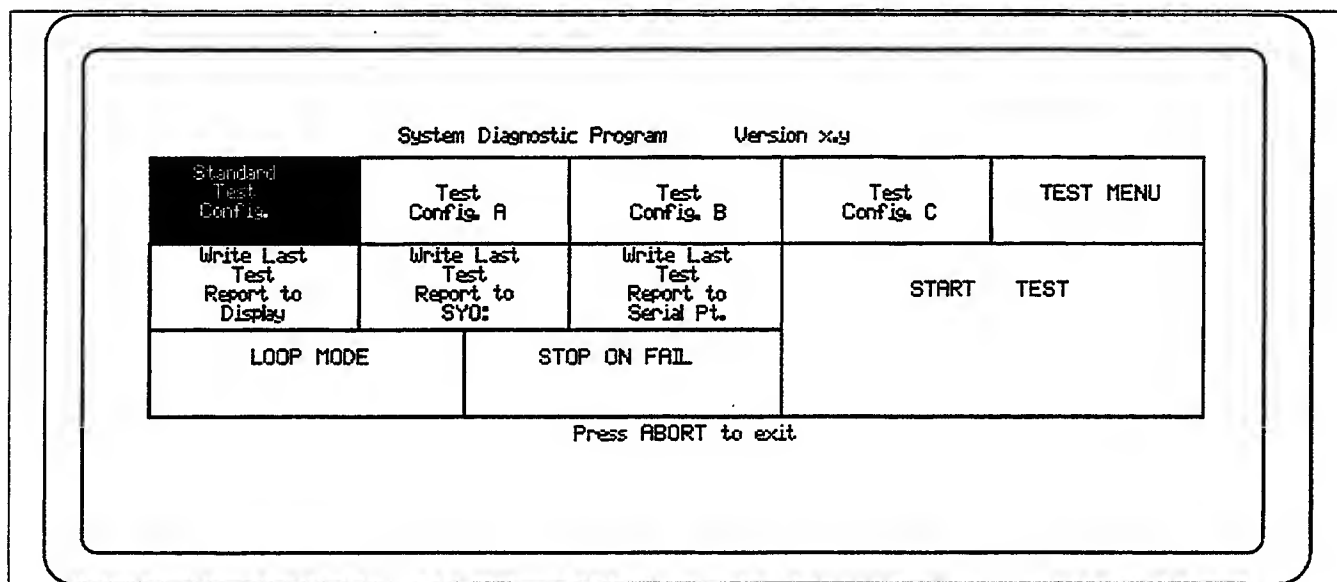


Figure 3-4. Main Menu

1. Standard Test Configuration.

The Standard Test Configuration is a set of tests that has been preselected to test the proper functioning of standard 1722A system modules. The tests allow untrained personnel to perform diagnostic testing. Additional hardware or test cables are not used with this test configuration. If the 1722A passes the Standard Test Configuration, the 1722A is fully functional up to the I/O drivers. The I/O drivers are tested with additional subtests and external hardware.

2. Test Config. A, Test Config. B, or Test Config. C.

The purpose of Test Configurations A, B, and C is to allow the creation of special test configurations. To create a configuration, select any combination of module tests and subtests, and store the special configuration if it will be needed again. Instructions on storing special configurations are given in the descriptions of the Test Menu selections.

3. Test Menu

By pressing the Test Menu command block, the Test Menu is displayed. From this menu, alternate test configurations can be defined and stored by the user.

4. Write Last Test Report to Display, SY0:, or Serial Pt. (Port)

After a test has stopped running, these three command blocks allow the user to redisplay the test results or send them to the system device or printer for future use.

If Write Last Test Report to SY0: is selected, the test results are stored in the file SY0:REPORT.DAT. If Write Last Test Report to Serial Pt. is selected, the test results are sent to serial port KB1: and can be output to a printer for a hard copy. The default baud rate set by the start-up command file when the System Diagnostic software is loaded is 1200 baud. Set your

printer to this baud rate. See Section 5 of the 1722A System Guide for more information about RS-232-C communications and the use of the SET Utility Program.

5. Loop Mode

The LOOP MODE command block performs like a toggle switch. When it is off (the power-up default), the test configuration executes one time and then stops. When LOOP MODE is on, the test configuration continues until the ABORT switch on the 1722A front panel is pressed.

6. Stop On Fail

The STOP ON FAIL command block performs like a toggle switch. When the System Diagnostic software is first loaded, STOP ON FAIL is selected. When STOP ON FAIL is off, the System Diagnostic software tests do not stop if a failure occurs.

When STOP ON FAIL is selected, the System Diagnostic software halts the test and gives a Stop Test Menu whenever a failure is encountered. An example of a Stop Test Menu is shown in Figure 3-5.

7. Start Test

The START TEST command block begins execution of the currently selected test configuration. The tests are executed and any failures are logged.

To begin any of the test configurations, press START TEST on the 1722A display. As the test runs, the 1722A display is updated at the completion of each subtest. To return to the Main Menu or to halt any test, press the ABORT switch on the 1722A front panel. If all the tests in the chosen configuration are successful, the display reads "No Failures". If any of the tests in the selected configuration are unsuccessful, three things happen:

- a. The 1722A display indicates the name of the test in progress at the time of the failure.
- b. The errors are stored on the "System Device".
- c. A Stop Test Menu is displayed with an error log and more operator choices.

CAUTION

Portions of the System Diagnostic software can write over areas of RAM used by FDOS. If <CTRL>/P is used to stop the System Diagnostic software, always reload the operating system by executing a cold start (press the RESTART and ABORT push buttons on the front panel simultaneously).

3-10. Test Menu

The Test Menu lets the user specify which modules are to be included in a particular test configuration. An example of a test configuration is the Standard Test Configuration which includes tests for the SBC, VGK, and floppy disk drive. If optional modules are installed in the 1722A, they can also be selected for testing from this menu.

The Test Menu consists of two screens of module/option selections. The initial screen contains the following module/option selections:

- Single Board Computer
- Floppy Disk Drive
- Video Graphics Keyboard
- RAM Options (-006, -007, -016, -017)
- NV RAM Options (-018, -019, -020)
- IEEE/RS232 Option (-008)
- Analog Measurement Processor (1752A-010) *

- Analog Output (1752A-011) *
- Counter Totalizer (1752A-012) *
- * Not for use with 1722A.

Figure 3-6 shows the initial selection screen.

To select a second screen, first press "Other Options (exit sd)", then "Subtest Menu" (appears in lower right of screen.) The second screen presents the following additional option selections:

- Parallel Interface (-002)
- Bubble Memory (-004, -005)
- Dual Serial Interface (-009)
- Dual Disk Drive (1760A, 1761A)
- Winchester Disk (1765A/AB)
- Winchester Disk (1765B)

To bring back the initial screen, press "Test Menu" at the bottom of the second screen.

With any of the module/option selections, the bottom row of menu selections is replaced with a new set of UNIT selections. Where multiple options of the same type are installed, these selections allow the user to select which option (UNIT) or set of options (UNITs) to test. Figure 3-7 shows the second selection screen with UNIT selections.

The command blocks for both screens of the Test Menu are described in the following paragraphs.

1. All Off

The All Off command block de-selects all the modules in the Test Menu that were previously selected for testing.

2. Store Configuration A, or B, or C

After a test configuration has been selected by lighting the appropriate display blocks in the Test Menu and

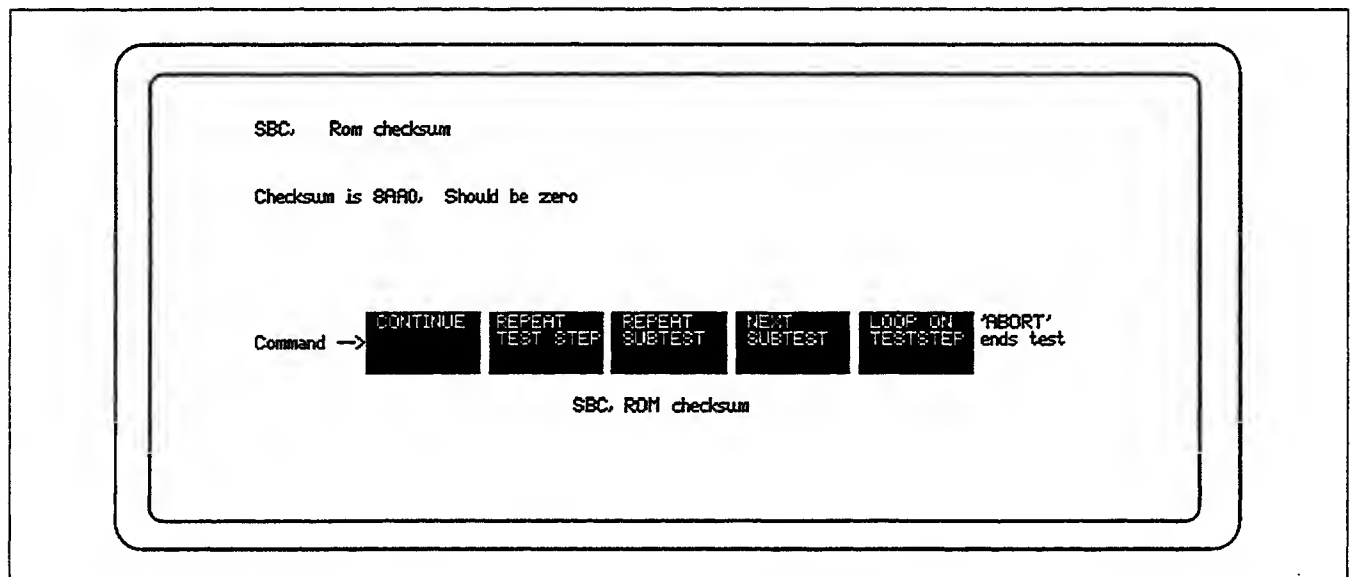


Figure 3-5. Stop on Fail Screen

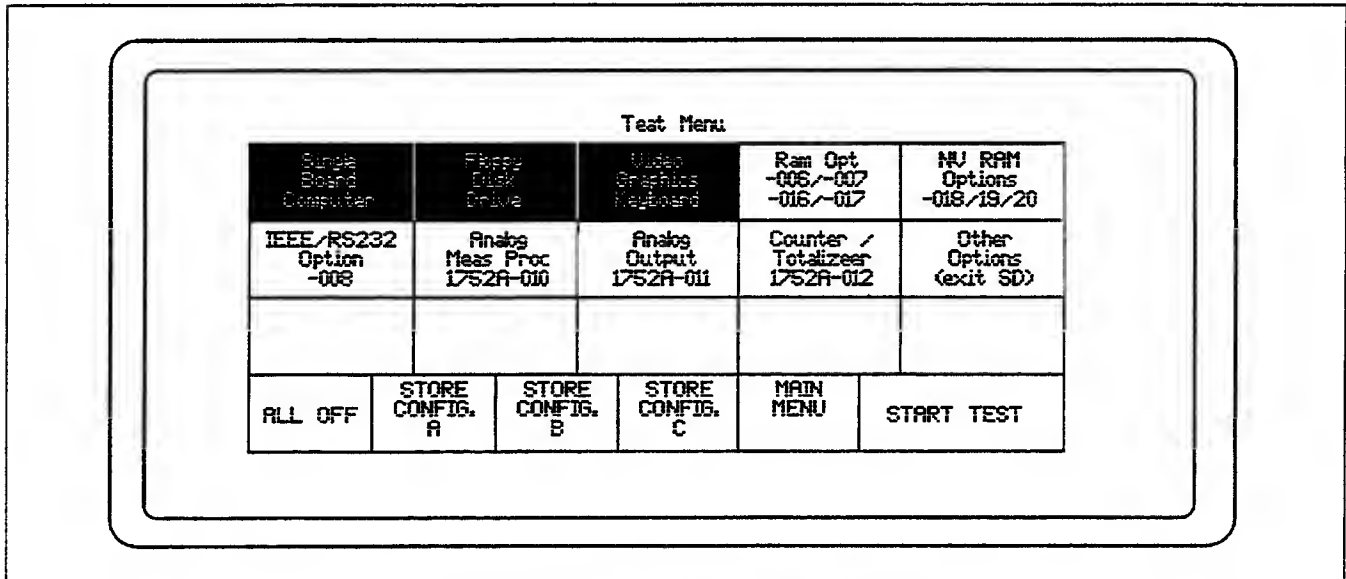


Figure 3-6. First Screen of Test Menu

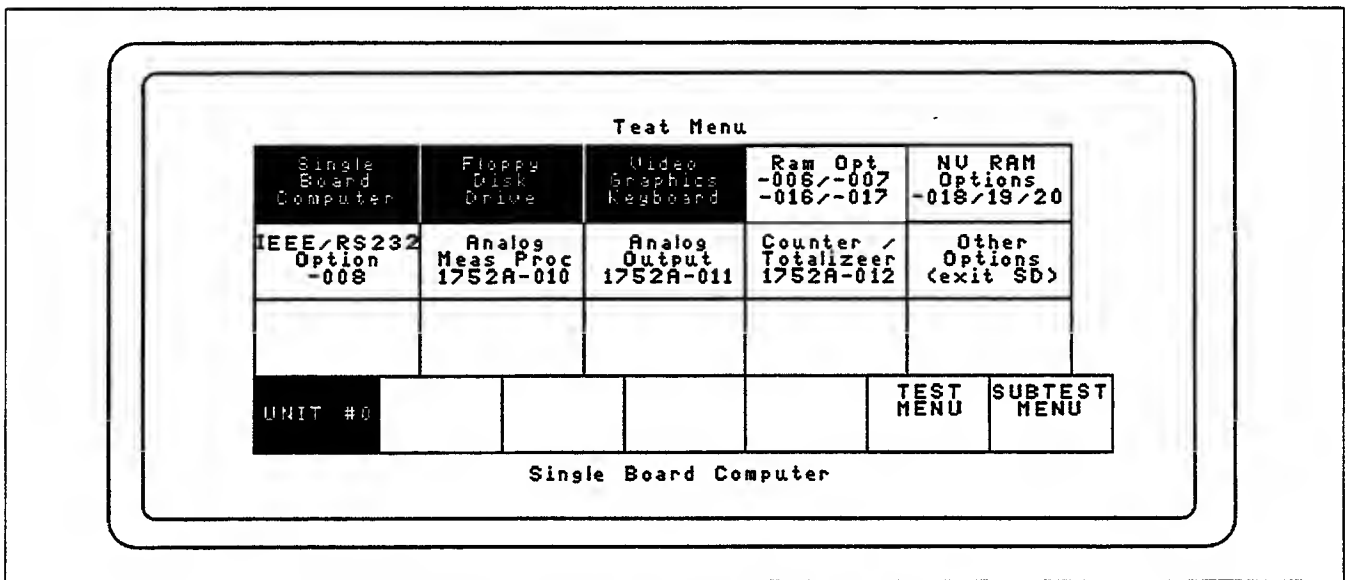


Figure 3-7. Second Screen of Test Menu

subtest Menus, the test configuration may be stored as Test Configuration A, B, or C by touching one of these command blocks. The special configuration is stored on the floppy disk and can be used again by selecting it from the Main Menu.

3. Main Menu

When the Main Menu command block is selected, the System Diagnostic software returns to the Main Menu.

4. Start Test

When the Start Test command block is touched, the currently selected test configuration begins to execute.

5. Unit #0, 1, 2, 3, 4

From the second screen of the Test Menu the user can select the number of units (modules of the same type) to be included in the testing.

6. Test Menu

Returns the user to the Test Menu screen.

7. Subtest Menu

When the Subtest Menu command block is selected, the Subtest Menu for the chosen module is displayed.

3-11. Subtest Menus

There is a Subtest Menu for each module listed in the Test Menu. From the Subtest Menu the user can select specific tests to be executed for the chosen module. This is useful

for obtaining more specific information about a module that has failed. For example, a failure at an RS-232-C port may be due to a problem on either side of the I/O buffers. To isolate the problem, there is an Internal Loopback Test, an External Loopback Test, and a Port-to-Port Loopback Test, any of which can be selected to exercise a particular portion of the module circuitry.

For each module subtest, there are 15 toggle-type subtest selection blocks and five command blocks. An example of the SBC Subtest Menu is shown in Figure 3-8.

The command blocks in the Subtest Menu operate identically to the command blocks described above for the Test Menu. The subtest selection blocks for each of the modules are described in the following paragraphs.

NOTE

The subtest selection blocks labeled "exit SD" are stand-alone programs that are loaded into memory, deleting the System Diagnostic software in the process. They cannot be run in LOOP MODE, because they do not return to SD after the test is completed. To reload the System Diagnostic software, press the RESTART and ABORT push buttons simultaneously.

3-12. SUBTEST DESCRIPTIONS

3-13. Single-Board Computer (SBC)

The SBC Subtest Menu includes the following tests:

1. Clock

Checks time rollover and storage of all stages of the real-time clock registers.

2. ROM Checksum

Generates a checksum for the contents of the BOOT ROM. The test fails if the checksum is not equal to zero.

NOTE

The ROM checksum test will not work properly with Version 1.0 of the 1722A BOOT ROM. The correct checksum for Version 1.0 is hex 8AA0.

3. Non-Destructive Macrostore

Performs a simple read/write test of the Macrostore memory. The contents of the Macrostore are left intact at the end of the test.

4. Non-Destructive RAM

This tests portions of the 1722A memory not presently being used by the System Diagnostic software.

5. Address Bus Test

This test uses the same algorithm as the Non-Destructive RAM test, but covers all of physical memory on the SBC and on any RAM options that are installed in the 1722A. Timeout errors are not reported, so if a RAM option fails to respond (missing or faulty) it will not be tested. When known good RAM options are installed in the 1722A, this test will check out the address and data buffers on the SBC.

6. Destructive Macrostore

This is a comprehensive memory test including pattern sensitivity. The System Diagnostic software loads another program from the disk to do this test, deleting the Operating System and the System Diagnostic software from the 1722A memory in the process. This

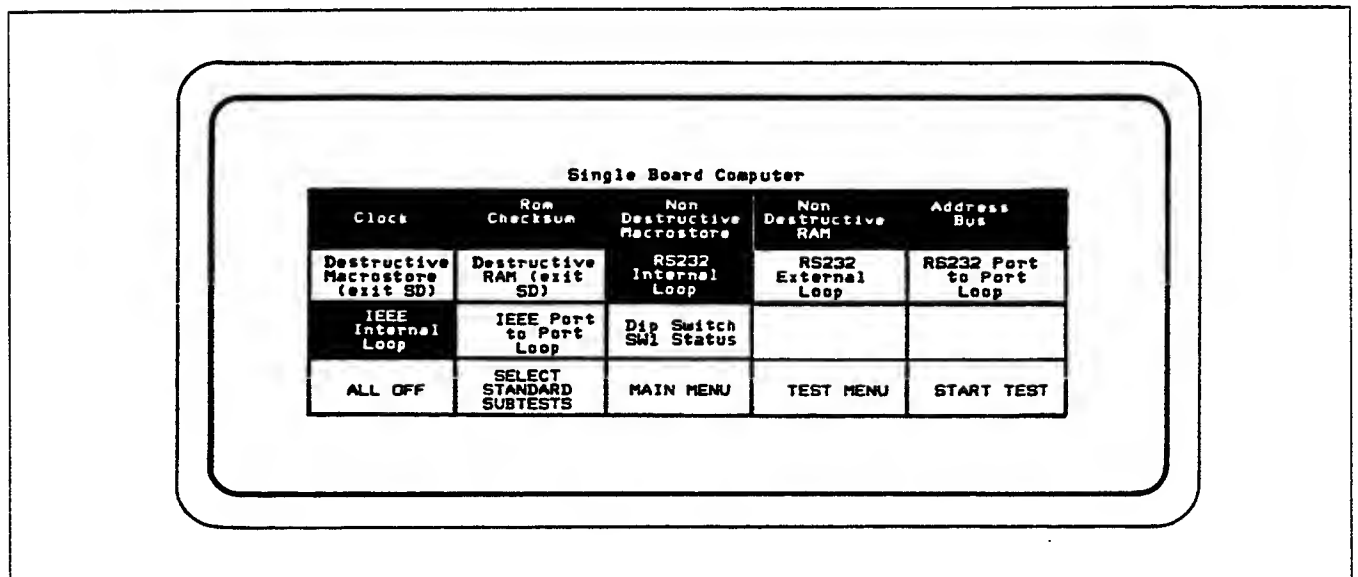


Figure 3-8. SBC Subtest Menu

test takes several minutes to complete. At the conclusion of the test, the Operating System and the System Diagnostic software must be reloaded.

7. Destructive RAM

This is an intensive memory test requiring approximately 30 minutes to execute. When the test is over, the System Diagnostic software must be reloaded because the test deletes the software from memory.

8. RS-232 Internal Loop

This test sets an internal loopback mode on the UART (universal asynchronous receiver transmitter) to allow the 1722A to send and receive data internally. The I/O buffers to off-board devices are not tested.

9. RS-232 External Loop

This test uses a special test connector (Fluke P/N 732107) to allow any port to talk to itself. The RS-232 External Loop test tests the buffers and registers of the RS-232-C port.

10. RS-232 Port-to-Port Loop

A Null Modem cable (Fluke Model Y1705) is required to permit two RS-232-C ports to communicate with each other and test the entire communications interface including the buffers. The Option 17XXA-008 IEEE-488/RS-232-C Interface module must be installed to run this test. The Null Modem cable connects the RS-232-C ports on the SBC and the Option -008 module.

11. IEEE Internal Loop

The IEEE-488 Internal Loop tests the operation of the IEEE-488 interface. The buffers to the IEEE-488 bus are not tested.

12. IEEE Port-to-Port Loop

The IEEE-488 Port-to-Port Loop Test verifies the port's ability to transmit or receive data and drive the IEEE-488 bus. Use any standard Fluke IEEE-488 cable (Y8021, Y8022, or Y8023). The Option 17XXA-008 IEEE-488/RS-232-C module must be installed to run this test. The IEEE-488 cable connects the IEEE-488 ports on the SBC and the Option -008 module. Switch positions 5 and 6 on the SBC must be in the OFF position and switch positions 5 and 6 on the Option -008 module must be in the ON position for the test to complete successfully.

NOTE

This test requires the user to remove the SBC or Option -008 module from the 1722A chassis in order to verify proper switch settings. It is not necessary to run this test unless there are IEEE-488 bus problems that cannot be identified using the Standard Test Configuration supplied with the System Diagnostic software. If it becomes necessary to run this test, refer to the Access Procedures later in this section.

This procedure explains how to remove the rear panel to gain access to the SBC and Option -008 module. Also, be sure to return the SBC and Option -008 to their initial switch configuration after running the test. For switch settings, see Figure 2-4 in Section 2.

13. Dip Switch SW1 Status Test

The Dip Switch SW1 Status Test reads the Single Board Computer switch settings and displays their status. Switch 5, which sets the System Controller function, is not tested by the SW1 Status test. Correct switch settings for the SBC may be found in Section 2 of this manual. For an option's switch settings, see the appropriate subsection in Section 6.

3-14. Floppy Disk Drive

The Floppy Disk Drive menu includes the following tests:

1. Write Protect Switch

This test displays the status of the Write Protect Switch. Removing or inserting a disk causes the switch to toggle. The System Diagnostic software tests to ensure that the switch does toggle. When testing is complete, touch the screen, and the System Diagnostic software reports its findings.

2. Track 0 Sw and Stepper Motor

The read/write head is moved from track 00 to track 39 and back again to test the operation of the track 00 indicator and the stepper motor.

3. Disk RPM Check/Adjust

A disk must be loaded to perform this subtest. Any disk will do, because nothing is written or read from the disk.

In this subtest the disk speed is measured and tested to ensure that it is within tolerance. The disk speed is displayed continuously if the System Diagnostic software is not in the LOOP MODE. When the System Diagnostic software is in the LOOP MODE, the disk speed is sampled and displayed for about 15 seconds, then the test continues to the next subtest. If the test results indicate that the disk speed needs to be adjusted, refer to the heading titled Alignment Procedures.

4. Format Disk

Formats a floppy disk in standard 1722A (double-sided) format. The operator will be asked for confirmation before proceeding.

5. Bad Block Scan

Each block on the disk is read and checked for errors. A total of 1600 blocks are read (two passes over the disk). The disk is never written on. Use this subtest to check a disk for bad blocks. If this subtest is used to check the disk drive itself, a disk with flawless format is required.

6. Soft Error Rate

This subtest does an extensive test of the disk drive's ability to read a worst case data pattern over many passes of the disk. A scratch disk with error free format is required. After writing the worst case data pattern (hex 6DB6DB...) over the entire disk surface, the disk is read for 306 passes (over 1 billion bits). This test takes approximately 3 hours to complete.

The display indicates the progress of the subtest while the disk is being read, showing the disk pass number, blocks read, bits read, and the current number of soft and hard errors. Refer to the heading titled Trouble-shooting for a description of soft and hard errors.

If the System Diagnostic software is in LOOP MODE, the total number of disk passes, blocks read, etc., for all the times the subtest was executed, are also shown in the display. The display is updated at the end of each disk pass.

7. Random Block I/O

This subtest tests the floppy disk drive's worst case ability to read, write, and seek. It is identical to the Soft Error Rate test except that the block number is chosen at random. A seek to the chosen block is followed by writing the worst case data pattern and reading it back. The total number of blocks tested is 800. The soft and hard errors are handled the same as in the Soft Error Rate Test.

3-15. Video/Graphics/Keyboard Interface (VGK)

The VGK menu includes the following subtests:

1. Alignment pattern

Displays the alignment pattern used for the initial factory setup of the CRT and permits later checking for shift of the display.

2. Keyboard

A picture of the keyboard is displayed on the screen. Each time a key is pressed on the 1722A keyboard, the corresponding key on the display toggles either on or off. Follow the instructions to light all the keys on the display and then touch the screen to continue. The diagnostic software records an error if a keystroke was not detected.

3. Touch-Sensitive Overlay

The Touch-Sensitive Overlay (TSO) grid is displayed. Each square covers exactly one TSO touch pad. Light each square by touching it. Press each one again to turn it off. The subtest passes if each touch pad responds at least twice. If a square does not work, exit the subtest by pressing the ABORT switch on the 1722A front panel.

NOTE

Graphics RAM, Vector Generator, and Character Attribute RAM tests will not work with versions of the VGK Firmware prior to Version 1.4.

4. Character RAM

Performs a read/write test of character and attribute memory and checks for stuck data bits and addressing errors. The display will be filled with a test pattern during this test.

5. Graphics RAM

Performs a read/write test of graphics memory and checks for stuck data bits and addressing errors. The display will be filled with a test pattern during this test.

6. Vector Generator

Performs a comprehensive test of the vector generator by drawing a series of vectors on the screen and reading back the contents of graphics memory.

7. Display Tests

Provide visual confirmation that the character generator, character graphics, and character attributes sections of the VGK are functional. Touching the screen cycles the test through several displays including double-size and single-size mode with attributes, standard and alternate character sets, and single-size and double-size character graphics. No error reporting is done, but information on the screen indicates what to look for.

8. Remote Control

Performs a functional test of the Handheld Remote Control Unit (RCU) supplied with the 1722A/AP Instrument Controller. Each LED on the RCU is turned on in sequence, and then the three push buttons are tested for continuity. Prompts indicate which RCU push buttons to use to proceed through the test steps. A failure is indicated any time an LED does not light at the appropriate time, or when the test fails to respond to a button press. Exit the subtest by pressing the ABORT button on the front panel.

3-16. Option -002, Parallel Interface

PIBTST is a program that tests up to three Parallel Interface Modules (Option 17XXA-002). The program performs three separate tests including writing to a port and reading back from the same port (Readback), writing to one port and reading back on the other port (Loopback), and an Interrupt test. When the program runs, the numbers of the modules under test are displayed across the top of the screen and the tests that are executing are displayed down the left side of the screen. In order to pass the Loopback test, a special test cable (Fluke P/N 632968) must be connected between the two ports on the module. If the user does not have a test connector, the Readback and Interrupt tests may be run individually by touching the PASS/FAIL block on the screen at the bottom of the column corresponding to the module under test. At this point a second menu is displayed. The user may run the tests individually on either port of the selected module by touching the screen at the appropriate point.

3-17. Option -004, -005, Bubble Memory

MBXTST is a program for testing up to three Bubble Memory Modules (Options 17XXA-004 and 17XXA-005). The program writes test patterns to the Bubble Memory to check for bubble collapse errors (a "1" bit turning into a "0") and pattern sensitivity problems with the Formatter/Sense Amplifier (FSA). Before executing the test, the program checks to see if there are any files on the bubble devices MB0: through MB3: and the user is asked to confirm whether he wants the files deleted. The bubble devices must be formatted in order for the test to execute properly. The bubble memories were formatted at the factory and should not need to be re-formatted unless there is a problem with the module. Any errors found during the test will be displayed on the screen and summarized at the end of the test. If the test will not execute properly try formatting the bubble memory using the File Utility Program (refer to Section 4 of the System Guide).

3-18. RAM Options (-006, -007, -016, -017)

RAM Options include the following:

- -006 (256k)
- -007 (512k)
- -016 (1M)
- -017 (2M)

Up to five of the smaller units can be tested at once by selecting the unit numbers from the Test Menu. Each unit number corresponds to a specific switch setting as described in the information supplied with the option and in Section 6 of this manual.

The menu for each RAM option includes the following tests:

1. Non-Destructive RAM Test

This subtest operates the same as the SBC Non-Destructive RAM test.

2. Destructive RAM Test

This subtest operates the same as the SBC Destructive RAM test. The test may take several hours to complete depending on how many memory option modules are installed.

3-19. Option -008, IEEE-488/RS-232-C

The subtests for the IEEE-488/RS-232-C option operate the same as the SBC Loop and Switch Status Tests. The cables described in the discussion of SBC subtests are also used for the IEEE-488 and RS-232-C port tests for Option -008. For the IEEE-488 Port-to-Port test, however, switch position 5 and 6 on the SBC are set to the ON position and switch positions 5 and 6 on the Option -008 module are set to the OFF position. Here is a list of the subtests for Option -008.

1. RS-232-C Internal Loop
2. RS-232-C External Loop
3. RS-232-C Port-to-Port Loop

4. IEEE-488 Internal Loop

5. IEEE-488 Port-to-Port Loop

NOTE

This test requires the user to remove the SBC or Option -008 module from the 1722A chassis in order to verify proper switch settings. It is not necessary to run this test unless there are IEEE-488 bus problems that cannot be identified using the Standard Test Configuration supplied with the System Diagnostic software. If it becomes necessary to run this test, refer to the Access Procedures in this section. That discussion explains how to remove the rear panel to gain access to the SBC and Option -008 module. Also, be sure to return the SBC and Option -008 to their initial switch configuration after running the test. For switch settings, see Figure 2-4 in Section 2.

6. Dip Switch SW1 Status

3-20. Option -009, Dual Serial Interface

Diagnostic program SPTEST performs a port-to-port loop-back test between the two ports on up to three -009 Options installed in the 1722A. 256 characters are transmitted and received on each port. An RS-232 Null Modem cable (Fluke Model Y1705) must be connected between the two ports on each -009 Option to test the RS-232 interface. A DSI Test Cable (P/N 754648) is required to test the RS-422 or 20 mA current loop interfaces. The port addresses must be set according to the information for the -009 Option in Section 6 of this manual.

3-21. Option -010, Analog Measurement Processor (1752A)

Option 1752A-010 is standard equipment with the 1752A. It is not present in the 1722A.

NOTE

Some of the Analog Measurement Processor subtests require the Solar Cell Board (P/N 765206) and Line Sync Transformer Accessory Y1752 (P/N 750687). The Solar Cell Board is supplied with the 1752A System. If another line sync transformer is used, its output should not exceed 5V ac, peak.

Up to four units can be tested at once by selecting the unit numbers from the Test Menu. Each unit number corresponds directly to a board address. (Unit 0 = board address 0, Unit 1 = address 1, etc.) To change a board's address, refer to Section 6 of this manual.

In the Analog Measurement Processor subtests, the lowest 16 channels of each board are referred to as channels 0-15, and the highest 16 channels are referred to as channels 16-31.

1. EEPROM Checksum Test

This test generates a checksum for the contents of the Analog Measurement Processor's firmware. The test fails if the checksum is non-zero.

2. RAM Test

This test performs a read/write check on the Analog Measurement Processor's RAM. The test verifies proper operation of the board's bus interface logic and identifies stuck data bits or board addressing errors.

3. Calibrate Routine

This routine allows you to calibrate the Analog Measurement Processor. The routine requires that the board's firmware be write-enabled. For calibration instructions, refer to the -010 Option subsection in Section 6 of this manual.

Note that the Calibrate Routine halts and waits for user input. The System Diagnostic Software cannot be run unattended while in the loop mode if this routine is chosen.

4. Phase-Locked Loop Test

This test verifies that the Analog Measurement Processor's phase-locked loop circuitry is operating properly. The test requires a reference signal from line sync transformer accessory Y1752 (P/N 750687). Connect the output of the line sync transformer to the external sync input (connector J3) on the Analog Measurement Processor when prompted.

The Phase-Locked Loop Test displays two sync frequencies: a 50/60 Hz Sync Frequency and a 400 Hz Sync Frequency. If the board is jumpered for 50/60 Hz operation, the 50/60 Hz Sync Frequency should be approximately 50/60 Hz. If the board is jumpered for 400 Hz operation, the 400 Hz Sync Frequency should be approximately 400 Hz.

Because you must connect and disconnect the external sync input during the test, the System Diagnostic Software cannot be run unattended while in the loop mode if this test is chosen.

5. Open Test (ch0-15)

This test scans channels 0-15 while their inputs are open-circuited. The test checks for channel inaccuracies caused by gross faults in the channel protection circuitry.

6. Grounded Test (ch0-15)

This test scans channels 0-15 while the respective inputs are shorted to the Analog Measurement Processor's common reference. The test checks the board's A/D circuitry for unusual channel leakage currents and for voltage offsets.

The Solar Cell Board is required for this test. Connect the cable from the Solar Cell Board to connector J1 (the right-hand connector) on the Analog Measurement Processor and set the switch on the Solar Cell Board to L.

7. Isolation Test (ch0-15)

This test scans the 15 legs of an external voltage divider to verify channel isolation between channels 0-15. The test verifies proper operation of the board's multiplexor circuitry.

This test requires the Solar Cell Board, which contains the 15-leg voltage divider, and a voltage input of 1-5 volts. Connect the cable from the Solar Cell Board to connector J1 on the Analog Measurement Processor (the right-hand connector), and set the switch on the Solar Cell Board to L.

Connect a voltage input of 1-5 volts between the INPUT and GND terminals on the Solar Cell Board. The voltage input can be provided by an external voltage source or by jumpering from the +5 and GND test points on the VGK. These test points are shown in Figure 3-9.

CAUTION

To avoid potential damage to the Analog Measurement Processor or the 1752A, the external voltage input must not exceed 30V.

8. Open Test (ch16-31)

This test performs the same checks on channels 16-31 as Open Test ch0-15 performs on channels 0-15.

9. Grounded Test (ch16-31)

This test performs the same checks on channels 16-31 as the Ground Test ch0-15 performs on channels 0-15. Before running this test, connect the cable from the Solar Cell Board to connector J2 (the left-hand con-

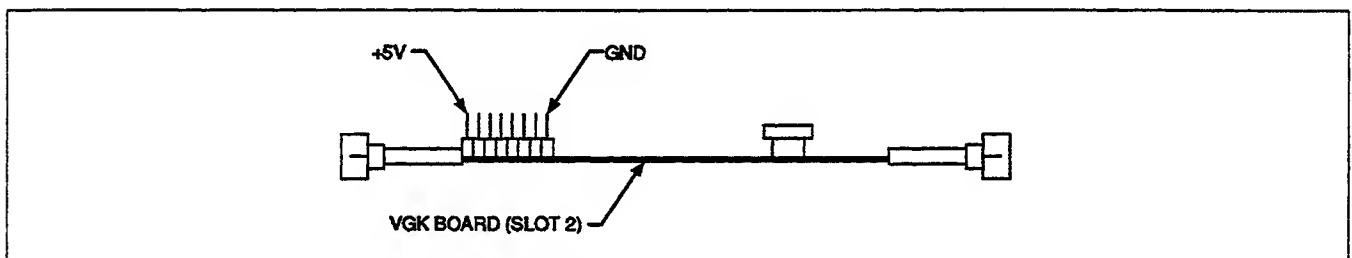


Figure 3-9. VGK Test Points

nector) on the Analog Measurement Processor and set the switch on the Solar Cell Board to L.

10. Isolation Test (ch16-31)

This test performs the same checks on channels 16-31 as Isolation Test ch0-15 performs on channels 0-15. Follow the instructions for that test, connecting the Solar Cell Board to connector J2 (the right-hand connector) instead of J1.

11. ADTST

ADTST allows the user to easily program and scan the input channels to the Analog Measurement Processor while applying an external input. (Refer to the 1752A Data Acquisition and Control Manual, Section 3, for programming information). This test is a menu-driven program that relies on the touch sensitive screen for input.

While ADTST is running, the program prints 4 menu buttons along the bottom of the screen. Each button represents a different function and pressing it will bring up a different screen. The functions associated with these buttons are listed below:

bd	allows the user to program board parameters (e.g. synchronization mode).
chan	allows the user to program input channel parameters for the selected board. The screen also has an input readout for the selected channel.
scan	prints the readings for all 32 input channels of the selected board. The readings are continuously updated.
exit	exits ADTST and reloads the System Diagnostic.

For an example using ADTST, refer to the performance test for the Analog Measurement Processor option in Section 6 of this manual.

3-22. Analog Output Option -011 (1752A)

Up to four units can be tested at once by selecting the unit numbers from the Test Menu. Each unit corresponds directly to a board address. (Unit 0 = board address 0, Unit 1 = board address 1, etc.) To change a board's address, refer to Section 6 of this manual.

Several of the Analog Output subtests require that you loop back (jumper) an output from the Analog Output board to an input on the Analog Measurement Processor. When making these connections, refer to Section 6 for connector pinouts. A screw terminal connector (Option 2400A-110) and terminal block with cable (Accessory Y1750) are recommended to facilitate these connections.

The loopback tests require that the Analog Measurement Processor be configured as board address 0.

The Analog Output subtest menu includes the following tests:

1. Register R/W Test

This test performs a read/write check on the board's registers. The test checks for stuck data bits and for proper operation of the board's bus interface logic.

Note that this test will output several voltages (or currents) from all channels on the Analog Output Option. You may want to disconnect the boards' outputs while running this test.

2. Channel 0 Voltage Loopback Test

This test verifies the accuracy of channel 0 when it is configured as a voltage output. The test requires that you loop back the + voltage and - voltage outputs from channel 0 to two input channels on the Analog Measurement Processor with board address 0. The test program tells you which channels to use.

3. Channel 1,2,3 Voltage Loopback Tests

These tests perform the same checks on channels 1 through 3 as Channel 0 Voltage Loopback Test performs on channel 0.

4. Channel 0 Current Loopback Test

This test verifies the accuracy of channel 0 when it is configured as a current output. The test requires that you loop back the + current and - current outputs from channel 0 to two input channels on the Analog Measurement Processor with board address 0. The test program tells you which channels to use.

5. Channel 1,2,3 Current Loopback Tests

These tests perform the same checks on channels 1 through 3 as Channel 0 Current Loopback Test performs on channel 0.

6. DATST

This test outputs a voltage or current on any channel selected by the user. DATST is a menu-driven program that relies on the Touch-Sensitive screen for input. For an example of DATST, refer to the performance test for the Analog Output option in Section 6 of this manual.

3-23. Option -012, Counter/Totalizer (1752A)

Up to five units can be tested at once by selecting unit numbers from the Test Menu. Each unit number corresponds directly to a board address. (Unit 0 = board address 0, Unit 1 = board address 1, etc.) To change a board's address, refer to Section 6 of this manual.

The Counter/Totalizer subtest menu includes the following tests:

1. Counter Chain R/W Test

This test performs a read/write check on the board's counter chain while the board is configured as a Totalizer. The test checks for stuck data bits in the counter chain and measurement storage registers, as well as proper operation of the board's bus interface logic (e.g. bus buffers, interface timing logic, etc.)

2. Timebase Selfcheck Test

The Timebase Selfcheck Test verifies that all types of time measurements can be made by the -012 option. This test internally loops back the signals comprising gate times 0-3. It then configures the board to take the following time measurements on these signals:

- Rising edge to rising edge
- Falling edge to rising edge using the fast rate clock
- Falling edge to rising edge using the slow rate clock

3-24. NVRAM Options (-018, -019, -020)

NVRAM Options include the following:

- -018 (256K)
- -019 (512K)
- -020 (1M)

Up to five NVRAM units can be tested at once by selecting the proper unit numbers from the unit selection screen. Each unit number corresponds directly to a board address (unit 0 = board address 0, unit 1 = board address 1, etc.) Refer to Section 6 of this manual for instructions on changing a board address.

The NVRAM subtest menu includes the following tests:

1. -018 (256K) Test (Destructive)
2. -019 (512K) Test (Destructive)
3. -020 (1M) Test (Destructive)

These tests allow you to perform a READ/WRITE test on a selected size of NVRAM option. Each of these tests checks the addressing, decoding, and integrity of the NVRAM ICs. Any data present on the NVRAM is erased during the test.

If an error is detected in one of the RAM ICs, the software attempts to report to the user which IC has failed. Such errors are reported by address, with indications of both the data written and the data read. For example, an error response could appear as follows:

— wrote 97FF, read 7FFF — check memory chip U103

4. Test All NV RAM (Destructive)

This test performs the same checks (as described above for individual types of NVRAM) - but on all types of installed NVRAM options that are detected. If there are multiple NVRAM units installed, this test eliminates any need to select each NVRAM option individually. The unit must be formatted after you perform this test.

5. Test Low Battery Circuitry

This test verifies the ability of the Low Battery Check circuitry to detect a discharged memory retention battery. (The battery is not checked.)

You must have access to the option board to perform this test. Refer to Section 6 of this manual for access instructions.

6. Write Protect Switch

This test ensures that the write protect switch and associated circuitry operates correctly. Refer to Section 6 of this manual for the required access procedures to the option.

7. Format

This selection formats the selected NVRAM option. Any prior data on the NVRAM is erased without warning.

3-25. Dual Disk Drive 1760/61A

MFXTST tests up to two 1760A or 1761A Disk Drive Systems. Refer to the Options section in the 1722A System Guide or the information supplied with the 1760A or 1761A for instructions on switch settings and connecting the unit to the 1722A. The program will check the disk drive speed and disk detection logic, then seek, format, write and readback data from a disk installed in each drive. The program will erase any files on the disk. Refer to the 1760A/1761A Manual for more information.

3-26. Winchester Disk Drives 1765A/AB

WDXSTST tests the 1765A/AB Winchester Disk Drive. The test selections are displayed on the screen and are selected by touching the desired menu item.

The tests include a self test of the 1765A/AB Winchester controller board and a verification of all of the blocks on the disk. If a bad block is found on the disk, that block is no longer used for storing data and an alternate block is automatically assigned.

These selections test the external IEEE Winchester Disk Drives. The 1765A/AB will test either the Zebec Inc. disk drive or the MSC disk drive. The 1765B test is intended for use only with the Bering Inc. disk drive unit.

When executed, both of these tests will present the user with a small text submenu with the following choices:

- Self test
“Self test” checks the interface and control system of the disk drive without any tests of the media.
- Verify
“Verify” does a quick read/write test of the media. A percentage done display indicates how far along the test is.
- Self test & verify
“Self test & verify” automatically runs both of the first two tests.
- Quit
“Quit” causes the program to exit. To continue further testing, you must invoke the SD program again.

3-27. SCSI Interface and Option -440 Hard Disk Test

The SCSI Interface Test verifies the SCSI interface circuitry inside the 1722A/1752A option bay. This test repeatedly checks the SCSI control and interface circuitry. A

PASS FAIL status is displayed as the test program continually loops through the various test segments. The test sequence continues until the TSO screen is pressed.

The SCSI Hard Disk Test differs in that the same set of tests are performed only once. The SCSI Hard Disk Test then continues on to a quick read test of a sampling of data blocks on the drive unit. If any error is detected, the program stops and displays the error. The 1722A/1752A must then be rebooted to resume additional testing. If no error is detected, the test program finishes and automatically restarts the SD program for additional testing.

3-28. System Diagnostic Error Messages

When the System Diagnostic software encounters an error during the execution of a test, an entry is made in an error log. If STOP ON FAIL has been selected from the Main Menu, an error message is displayed on the screen. This message includes the name of the module under test and the particular subtest being executed when the error occurred.

Generally, the module under test is at fault whenever an error occurs. If an error is reported, check that the switch settings are correct on the module in question (if applicable), then run the test again. If the error condition persists, replace the module after verifying that it is faulty. (See Board Isolation Procedure.)

3-29. TROUBLESHOOTING

3-30. Introduction

The following information is intended to aid in troubleshooting a standard 1722A or 1752A in the event that the System Diagnostic software will not load and run, or when it is necessary to troubleshoot to the component level. Troubleshooting information for 1722A and 1752A options may be found in Section 6. The information is presented in three parts: the Dead Box Procedure, the Board Isolation Procedure, and the Fault Analysis Procedure. The Dead Box Procedure is an aid for troubleshooting a dead controller at the module level when the system will not run the System Diagnostic program. The Board Isolation and Fault Analysis Procedures require some dismantling of the 1722A and considerably more skill than does the Dead Box Procedure. The Board Isolation Procedure should be used when the fault cannot be isolated by the Dead Box Procedure. The Fault Analysis Procedure is intended to lead the technician to the component or group of components at fault.

Because of the large number of possible combinations of failure modes and effects, this manual cannot hope to address all possibilities. However, it does address the most common problems encountered by factory technicians and the most common problems associated with high failure component types.

It is possible to isolate troubles to sections of a faulty board by using a logical thought process and by checking signal levels and scope patterns. However, isolating troubles

to the component level can be a demanding and time-consuming task, particularly on the VGK module. It is therefore recommended that any defective modules be returned to the factory and replaced with functional modules if at all possible.

If a module cannot be replaced for some reason, and you wish to attempt to repair it you will need, at a minimum, a multi-trace O-scope, a digital multimeter, a logic probe and a quantity of replacement ICs to swap for suspect ICs. Although some chips are installed in sockets, most are soldered into the circuit board, so be prepared to unsolder DIP ICs in order to swap them.

CAUTION

Remember that all the modules manufactured by Fluke used in this unit are multilayer printed circuit boards (pcbs). Irreparable damage may be done to the pcbs' feed-through plating, and consequently to internal layers, unless extreme care is used when removing and replacing components.

3-31. General Troubleshooting Tips

3-32. LOGIC TECHNIQUES

Successful troubleshooting of any microcomputer depends on the ability to watch what the unit is doing and use deductive reasoning to arrive at a set of probable causes. This process requires that one carefully analyze how the hardware and software interact, and how the interaction differs from the expected sequence.

For example: If the system proceeds only part way through the self-test process before crashing, one can reason that something is amiss in the SBC dynamic RAM. Here is a logical process that leads to this conclusion.

The self-test procedure is part of the boot sequence, which prints HELLO to the screen as it begins, followed by SELF TEST IN PROGRESS. When the boot and self-test routine is finished, it prints LOADING to the screen.

EXAMPLE SYMPTOM:

The SBC Microprocessor starts to boot but does not finish self-test.

To start booting and print HELLO we know that:

- The Microprocessor fetches the boot and self-test program from ROM.
- The Microprocessor is a TMS 99105, which requires DRAM as short term workspace memory.
- The Microprocessor must read/write data and address memory.

To complete the self-test and print LOADING we know that:

- The Microprocessor must have read reliable data from DRAM as long-term memory.
- DRAM must be refreshed periodically or it quickly forgets and data become unreliable, although it sometimes can hold data for several seconds.

THEREFORE:

Since the Microprocessor is able to read short-term data, stored in DRAM as workspace data, but long-term data is unreliable or has been lost, we may conclude that the Microprocessor and support logic, clock, ROM, DRAM, and read/write hardware are functional but that the refresh hardware is suspect.

There may be other considerations for this particular example, but this represents a process that will lead one to a suspected group of components. Although it is beyond the scope of this manual to provide logical processes leading to all subsystems of the 1722A, background information is provided detailing what should be expected and how the hardware and software interact so that a technician can use this method.

This logic technique is useful for troubleshooting the SBC, but it is less suited for troubleshooting the VGK because most VGK operation is transparent except to a technician with access to equipment usually found only at the factory. Accordingly, this manual presents a more symptomatic approach with respect to the VGK.

Because of the complexity of this unit it is doubtful that random replacement of high-failure components will be a successful technique, at least initially. However, if one keeps accurate records of which component failures are associated with various symptoms, a more intuitive approach may become successful.

3-33. CIRCUIT ACTIVITY OBSERVATION

Circuit activity can be observed by using a logic probe and watching the activity on various suspected lines when the unit is rebooted using the ABORT and RESTART push buttons. In particular, look for logic levels that you know to be wrong, such as DCOK being low after power supply voltages have come up. Most important, look for a floating logic level at an input or output pin of a suspected component.

3-34. POOR CONNECTIONS

Poor electrical connections in the plugs and card-edge connectors are a common source of trouble, and can produce a wide variety of symptoms. When checking for signals, check at both the source and destination of the signal to logically eliminate connectors and cables as sources of trouble. Card-edge pins and traces should be cleaned with a non-abrasive device such as a cotton swab and alcohol.

CAUTION

Do not use a red pencil eraser or other abrasive devices on gold-plated edge connectors.

When using card extenders or extension cables, be sure that the edge-connector fingers line up with the contacts. Some card extenders allow the contacts to shift, thus breaking contact.

3-35. Dead Box Procedure

3-36. INTRODUCTION

In order to run the System Diagnostic software, the 1722A must be able to load and run the operating system and the System Diagnostic software. The Dead Box Procedure should be used whenever the 1722A will not load the operating system or the System Diagnostic. The following paragraphs provide an analysis for diagnosing problems at the module level up to the point at which the System Diagnostic can be run.

The symptoms in the Dead Box Procedure are arranged in the chronological order that they would appear after power-up or operator-controlled reset. It is important to read the entire sequence of indications to arrive at a probable cause at the module level. Simply searching for a symptom that matches yours will lead you astray, since it isn't possible to list all the symptoms that might occur.

3-37. POWER-UP INDICATIONS

3-38. Normal Operation

When the 1722A is first powered up, the fan on the rear panel starts up, and two beeps can be heard, one from the 1722A chassis and one from the keyboard, if it is plugged in.

3-39. Fault Indication

SYMPTOM 1:

No beeps are heard and the fan does not come on.

POSSIBLE CAUSES:

- The cord is not properly installed.
- The line voltage, indicated on the rear panel, does not match your line power source.
- The line fuse on the back panel is blown.
- The fuse on the power-supply board is blown. (See Access Procedures later in this section.)

CONCLUSION:

If the above items are in order, the power supply is faulty.

SYMPTOM 2:

The fan is running, but there is no beep from the chassis.

POSSIBLE CAUSES:

- The VGK is faulty.
- The PUP (Power-Up Assembly) is faulty.
- The power supply is faulty.

NOTE

To isolate the VGK, the power supply or the PUP as the source of trouble the see Board Isolation Procedure in this section.

3-40. DISPLAY INDICATIONS

3-41. Normal Operation

After the 1722A warms up (less than one minute), the Bootstrap Loader should print HELLO to the screen, and a beep from the chassis should be heard. The beep can be considered an indication that the VGK is functional. The screen should then display SELF-TEST IN PROGRESS. During the power-up and self-test sequence the 1722A will display error messages describing defective component groups, if any. While this is not normal, it does indicate that the SBC is at least partially functional.

After the 1722A has executed the power-up and self-test sequence, it attempts to load the operating system (FDOS2.SYS) from the floppy disk. The message LOADING should be displayed on the screen, and the disk-drive-activity light on the front panel should come on.

The word LOADING on the CRT is an indication that the boot sequence has arrived at the point at which it attempts to load the operating system from the disk into memory. The print-to-screen instruction for LOADING is embedded in the boot ROM, so the appearance of LOADING does not mean that loading is actually taking place. LOADING means only that the boot ROM has attempted to access the floppy drive if FDOS is to be loaded from the disk. If the disk is bad, FDOS can't be loaded.

3-42. Fault Indication

SYMPTOM 3:

There is a beep but no display at all after a power-up or cold start.

POSSIBLE CAUSES:

- The CRT is faulty.
- The video electronics board is faulty.
- The associated cables are faulty.

SYMPTOM 4:

The CRT display shows a blinking cursor, but HELLO is not displayed.

CONCLUSION:

The CRT and video electronics are functional.

ACTION:

Perform a cold start. (Press the RESTART and ABORT switches on the 1722A front panel simultaneously.)

CONCLUSION:

If the problem persists, possible causes are:

- The SBC is probably faulty. (See Board Isolation procedure.)
- The ARGUS Interface on the VGK may be faulty. (See Board Isolation procedure.)

SYMPTOM 4A:

HELLO is displayed, but LOADING is not.

POSSIBLE CAUSE:

The SBC is faulty.

3-43. DISK DRIVE INDICATIONS

3-44. Normal Operation

Following the display of LOADING on the screen, the disk-drive-activity light should come on and the disk drive should whirl momentarily and then shut off. When the disk drive shuts off, the light should go out. At this time the disk should have finished loading and the System Diagnostic Menu should be displayed on the screen if you loaded the System Diagnostic disk.

3-45. Fault Indications

SYMPTOM 5:

The disk-drive-activity light comes on, and the drive whirs, but the operating system does not load.

One of the disk-error messages should be displayed on the screen. Causes of error at this point usually result from hard or soft media errors. A soft error is any single failure to read a block correctly. It can be caused by improper seating of the disk or by a dust particle momentarily passing under the read/write head. An occasional soft error is of no concern. Ten successive soft errors are considered a hard error and indicate a problem either with the disk or the disk drive.

In general, whenever a disk error occurs:

- Reseat the disk by opening and reclosing the disk drive door.
- If the problem persists, try another disk. If this solves the problem, the original disk was faulty.

Disk error messages can occur at any time during the operation of the 1722A Controller. They are always preceded by a question mark indicating that they are non-recoverable. The Controller continues to return the same error message until you take some corrective action.

? Disk Not Ready

Insert or reinsert the System disk. Either there is no disk in the drive, or it has been inserted incorrectly. Make sure the disk drive door is latched.

? Illegal Directory

The disk is faulty and must be reformatted before the Controller will operate properly. Try another system disk.

? Device Error

The system is having difficulty reading the floppy disk. Check to be sure it is a System disk, and that it is inserted properly. If so, RESTART and try again. If the failure continues, try another System disk.

? No System On Device

The Controller does not recognize the disk in the drive as a System disk. Try another System disk. The wrong disk may be inserted or it may be inserted incorrectly.

3-46. Disk Drive Fault Indications

Some disk drive problems are indicated by the fact that the disk drive simply does not run. Others are indicated when the drive runs, but the disk will not load. Disk drive problems can be isolated from disk problems by using the process of elimination.

SYMPTOM 6:

The disk drive runs, but the disk won't load. The problem cannot be solved by using another disk.

POSSIBLE CAUSES:

- The disk drive is faulty.
- The disk drive is out of calibration.
- The disk controller on the SBC is out of calibration.

SYMPTOM 7:

The disk-drive-activity light does not come on, and the disk drive motor does not come on.

POSSIBLE CAUSES:

- The disk drive is faulty.
- The associated cables are faulty.
- The SBC is faulty.

NOTE

If the disk drive motor comes on but the light does not, check the LED. (See Access Procedures, later in this section.)

3-47. SYSTEM DIAGNOSTIC INDICATIONS

3-48. Normal Operation

The software makes extensive use of block graphics and video attributes. (See the heading titled System Diagnostic Software for proper appearance of menus.) The system should respond when the TSO is touched. There is a TSO test in the System Diagnostic program that verifies the operation of the TSO. Operator interaction is required for this test.

3-49. Fault Indications

SYMPTOM 8:

Some of the reverse video blocks or highlighted characters do not appear to be correct.

POSSIBLE CAUSE:

The VGK may be faulty.

SYMPTOM 9:

The System Diagnostic software has been loaded, but there are problems with the appearance of the menus.

POSSIBLE CAUSE:

The VGK may be faulty.

SYMPTOM 10:

The display does not respond when a menu block is touched.

ACTION:

Try other menu blocks. Keep in mind the possibility of parallax error as discussed in Section 2 of the 1722A System Guide/1752A System Guide.

CONCLUSION:

If the problem persists, the Touch-Sensitive Display is faulty.

3-50. KEYBOARD INDICATIONS

3-51. Normal Operation

During a power-up or cold start, the keyboard should emit a beep, and both the CAPS LOCK and PAGE MODE indicators should light momentarily.

3-52. Fault Indication

SYMPTOM 11:

The keyboard does not respond when a key is pressed, but the characters and System Diagnostic menus are correctly displayed.

ACTION:

1. Press <CTRL>/T to reset the keyboard and display.
2. Perform a power-up reset on the keyboard. (Momentarily unplug the keyboard.)

CONCLUSION:

If the problem persists, one of the following is faulty:

- The keyboard.
- The VGK.

To isolate the problem to one or the other, substitute a good keyboard or a good VGK.

3-53. Board Isolation Procedure

3-54. INTRODUCTION

Since the Dead Box Procedure may not discriminate between problems that could be caused by either the SBC or the VGK and problems that could be caused by either

the VGK or the PUP, the following paragraphs provide an analysis that will aid in isolating the trouble to one board.

3-55. ISOLATING DEFECTIVE PUP OR VGK

The PUP resets the system on power-down by using the DCOK signal. The PUP also monitors power supply voltages and controls the ABORT and WBOOT lines, which are activated when the ABORT and/or RESTART push buttons are pressed.

The PUP holds the System Reset line (DCOK) low until power supply voltages have come up. If, for this or some other reason, the DCOK line is held low, the system will not come up.

SYMPTOM 12:

No beep is heard from the VGK on power-up.

POSSIBLE CAUSES:

- The VGK is faulty.
- The power supply is faulty.
- The PUP is faulty.

ACTION:

Take the cover off the PUP. (See Access Procedures.)

- Check the reference voltages on the PUP at TP1, TP2, and TP3.
- Check the power supply voltages at J102 pins 2 and 3.
- Check the DCOK line. It should be high if the power supply voltages are correct.
- Check the ABORT and WBOOT lines. These should be inactive unless the ABORT or RESTART push buttons are depressed.

CONCLUSION:

- If the power supply and reference voltages are correct and the DCOK line is high, the PUP and power supply are OK, and the problem is the VGK.
- If all voltages are correct and the DCOK line is low, the problem is the PUP.
- If the power supply voltages are correct and the Reference voltages are incorrect, the problem is probably the power supply, but could be the PUP.
- If the power supply voltages are incorrect, the problem is the power supply.

NOTE

If you suspect the VGK is faulty and want to double check, follow the instructions in the next paragraph.

3-56. ISOLATING DEFECTIVE SBC OR VGK

As discussed in the Dead Box Procedures, a symptom that is common to both the VGK and the SBC is when only the

cursor is displayed on the CRT. To determine which of the two modules is at fault, an ASCII terminal can be substituted for the VGK.

SYMPTOM 13:

Only the cursor appears on the screen.

ACTION:

1. Unplug the VGK. (See Access Procedures for removal instructions.)
2. Plug an ASCII terminal, set to match the baud rate of the SBC, into the RS-232-C connector on the SBC. A Y1702 cable should be used with the terminal.

NOTE

The baud rate of the SBC can be changed if necessary. For switch settings, see Figure 2-4 in Section 2.

3. Perform a cold boot by pressing the ABORT and RESTART push buttons simultaneously.
4. The SBC should now execute the complete power-up and self-test sequence, beginning with the word HELLO and ending with the word LOADING displayed on the ASCII terminal.

CONCLUSION:

- If LOADING is not displayed, it is highly probable that the SBC Microprocessor, support logic, or memory is faulty; however, it is possible, although not likely, that the VGK and the RS-232-C interface are faulty.
- If LOADING is now displayed on the ASCII terminal screen, it is highly probable that the VGK is faulty; however, it is possible that the ARGUS/AGGIE interface on the SBC is faulty. Since the SBC talks to the VGK over the CRU subset of the ARGUS/AGGIE bus, the fault probably lies in the bus interface devices on either the SBC or the VGK.

ACTION:

To determine if the problem lies in the SBC/VGK interface:

1. Unplug the ASCII terminal at the RS-232-C connector.
2. Install the VGK on a card extender, making sure that the contacts are aligned.
3. Execute a cold boot by simultaneously pressing the ABORT and RESTART push buttons.
4. Check for CRUIN at pin 39 of the VGK card-edge connector and CROUT at pin 40. Also check CRCLK-. Note: these signals are active ONLY when the VGK and SBC are communicating.

CONCLUSION:

- If CRUIN and CROUT are present, the ARGUS/AGGIE interface on the SBC is functioning.
- If these signals are not present, the problem is on the SBC.

3-57. Fault Analysis Procedure

Many problems can be isolated by observing how far through the boot procedure the 1722A gets before a failure is observed. Other problems occur while the unit is operating and may be isolated by observing the display on the CRT. Refer to the example in the Troubleshooting introduction for a method of analyzing symptoms.

3-58. SBC FAULT ANALYSIS

3-59. Introduction

Once trouble has been isolated to the SBC module, faults can be further isolated by observing how far the power-up and self-test sequence proceeds before failing or hanging up. If the SBC will run the self-test routine, isolating the fault will, of course, be much easier. On the other hand, if the SBC will not run the boot-strap program at all, the trouble cannot be isolated without checking scope patterns and signal levels. These guidelines are arranged chronologically, beginning at the start of the boot-strap routine

and ending with an analysis of disk access problems.

For reference, interrupt assignments are shown in Table 3-2.

3-60. Symptoms

A message displayed on the screen saying HELLO followed by SELF TEST IN PROGRESS is an indication that the SBC is booting from ROM.

SYMPTOM 14:

Only the cursor is displayed on the screen. No HELLO message appears.

This is an indication that the boot-strap program is not executing. Any components associated with the "core" of the computer on the SBC could be faulty. Below is a list of the more common failures.

POSSIBLE CAUSES:

- Clock (U74)
- Microprocessor (U75)
- Boot ROM (U68, U81)
- Data Buffers (U76, U85, U44, U60, U7, U8)
- Address Latches (U78, U84)

Table 3-2. Interrupt Assignments

LEVEL	DESCRIPTION	COMMENT
NMI	Warm Boot (WBOOT-)	Non-Maskable Interrupt
0	Data Bus Bit 0 (DI00)	Unused
1	1797DRQ- (Floppy on SBC)	
2	Exception Conditions:	
	Timeout	Timeout
	MERR	Map Error
	ACOK/ABORT	Abort
	WERR	Write Error
	HALT-	Halt
3	Data Bus Bit 3 (DI03)	Bubble Option
4	1797INT- (Floppy on SBC)	
5	Data Bus Bit 5 (DI05)	Parallel I/F
6	Data Bus Bit 6 (DI06)	IEEE-488/RS-232-C
7	9902INT- (UART on SBC)	
8	Data Bus Bit (DI08)	VGK
9	9914INT- (IEEE on SBC)	
10	Data Bus Bit 10 (DI10)	IEEE-488/RS-232-C
11	Data Bus Bit 11 (DI11)	Memory Expansion
12	Data Bus Bit 12 (DI12)	Unused
13	Data Bus Bit 13 (DI13)	Bubble Option
14	Data Bus Bit 14 (DI14)	Unused
15	Data Bus Bit 15 (DI15)	Unused

NOTE: Unused interrupts are available for future options.

- Microprocessor's workspace in DRAM (U52-U59, U36-U43)
- DRAM address and control logic (U46, U47, U33)
- RAS and CAS Generator (U19, U51, U62, U65, U66,)
- Wait Generator (U31)

CONCLUSION:

These elements make up the "core" of the SBC. Signal levels and activity must be checked individually to determine the fault.

SYMPTOM 15:

Error message displayed for all devices.

POSSIBLE CAUSE:

DRAM is faulty (U52-U59 and U36-U43).

CONCLUSION:

If part of DRAM not used as workspace fails, the self-test may display an error message for every device on the SBC. During the self-test, the Microprocessor writes to write/readable registers and stores the value written in memory. It then reads the register to which it wrote, comparing what it reads with what it stored in memory. If the data does not match, the Microprocessor writes an error message to the screen. Thus, if the DRAM memory cells that the self-test uses for memory are faulty, the Microprocessor will report an error, having assumed the DRAM to be functioning.

If there is a fault in the DRAM, the self-test software is unlikely to reliably report which bits are bad. In fact, the self-test software is unlikely to run at all. There is a chance, however, that the SBC RAM tests will return an error message that is meaningful. In this case, Table 3-3 may be used to help isolate the failure to a specific DRAM chip. Another possibility is that the buffer chips U44 and U60 are at fault and the DRAM chips are OK.

SYMPTOM 16:

The screen displays HELLO and SELF-TEST IN PROGRESS, or only HELLO, but does not display LOADING (fails part way through test).

POSSIBLE CAUSE:

The DRAM Refresh Logic is faulty (U33, U35, U48, and U49).

CONCLUSION:

If the self-test fails or hangs up part way through the test sequence, it may indicate that the DRAM refresh logic is at fault. The DRAM can store data for a time without being refreshed. Since the DRAM can sometimes hold data for several seconds without being refreshed, there may be enough time for the boot and self-test to partially complete its sequence before the DRAM begins to suffer from lost data. Check to see that RFR- has a period of 15.6 μ s.

SYMPTOM 17:

Self-Test error message displayed.

The following are error messages that may be printed during self-testing. The error messages may be displayed even though the System Diagnostic will not run. If an error occurs during the self test, a message will be displayed that takes the form:

FAILED: - xxx Test.

The xxx will be replaced by the failing component name, and may be any of the following:

- ROM Test
- RS-232 Port Test
- Memory Mapper Test
- Macrostore Memory Test
- On-Board Memory Test
- IEEE Controller Test
- Floppy Disk Controller Test

ACTION:

Try resetting the Controller first, but if the error continues, make a note of the test that failed.

CONCLUSION:

All of these messages indicate a non-recoverable hardware failure.

NOTE

Table 3-3 can help isolate faulty Macrostore RAM chips.

SYMPTOM 18:

The LOADING message is printed to the screen but the disk drive light does not come on.

NOTE

This symptom can be caused by a faulty disk drive unit or associated cables; however, it is assumed at this point that the fault has been isolated to the SBC.

POSSIBLE CAUSES:

- No output from Floppy Motor Controller chip (U1).
- The Data Buffer (U2) is faulty.
- The floppy-calibration jumper is in the CAL position.

CONCLUSION:

Component faults other than those mentioned as possible causes would have been found during self-test, and the screen would have displayed an error message.

SYMPTOM 20:

The screen displays LOADING; the disk drive comes on, then shuts off without displaying an error message or loading FDOS.

Table 3-3. DRAM and Macrostore Fault Isolation

DRAM FAULT ISOLATION			MACROSTORE FAULT ISOLATION	
Bit Position Where XOR = 1	DRAM Chip at Fault	Buffer Chip at Fault	Bit Position Where XOR=1	Macrostore Chip at Fault
LSB 0	U52	U60	LSB 0	U69
1	U53	U60	1	
2	U54	U60	2	
3	U55	U60	3	
4	U56	U60	4	U70
5	U57	U60	5	
6	U58	U60	6	
7	U59	U60	7	
8	U43	U44	8	U71
9	U42	U44	9	
10	U41	U44	10	
11	U40	U44	11	
12	U39	U44	12	U72
13	U38	U44	13	
14	U37	U44	14	
MSB 15	U36	U44	MSB 15	

EXAMPLE:

The unit failed the Macrostore Memory Test at memory location 20000. The Microprocessor wrote 7FFF, but read back FFFF, and displayed this error on the screen. To find the position of the bit in error and thus the chip at fault, first convert the hexadecimal numbers displayed on the screen to binary. Next, XOR the two binary numbers. The position of the resulting ones (1) correspond to the location of the bit in error.

MSB LSB

7FFF = 0111111111111111

FFFF = 1111111111111111

XOR: 1000000000000000

Note that the 1 in the MSB position represents the error bit. Look at the table and find bit 15, the MSB. Note that this bit is the MSB of U72. Thus, U72 is the faulty bit.

POSSIBLE CAUSES:

- Interrupt request is stuck on, either as a result of defective interrupt logic or as a result of the interrupt line on some device being stuck on. This symptom can be associated with the interrupt logic (U5, U6, U15, U16, and U86) or some device that requests an interrupt.
- Check inputs to interrupt priority encoders (pins 1, 2, 3, 4, 10, 11, 12, 13) of U15 and U16. None should be stuck low (active).
- Check interrupts 1797DRQ- and 1797INT-.

NOTE

1797DRQ- interrupt is the data request interrupt from the Floppy Disk Controller. It should be active during data transfers to the disk.

1797INT- interrupt signals the end of a data transfer or a fault condition during a data transfer to the disk.

CONCLUSION:

While FDOS is being loaded, all interrupts are disabled. One of the first things FDOS does is turn the interrupts on.

If the interrupt logic is faulty, the Microprocessor continually sees an interrupt request and enters the appropriate interrupt service routine. Upon completion of the service routine, it immediately sees another request and reenters the service routine.

SYMPTOM 21:

Part of the FDOS start-up message is printed to the screen, then the disk drive shuts off.

POSSIBLE CAUSE:

See previous SYMPTOM.

SYMPTOM 22:

SBC loads FDOS but will not run System Diagnostic or other programs.

POSSIBLE CAUSES:

- Interrupts generated by Floppy Controller. (Check.)
- DRAM refresh. (Check.)

CONCLUSION:

- FDOS is loaded with interrupts disabled, but from then on it requires the Floppy Disk Controller to generate interrupt requests, since FDOS turns the interrupts on right after it is loaded. So, if the Floppy Disk Controller cannot generate interrupts, FDOS can be loaded, but from then on the disk cannot be accessed.
- DRAM refresh may be partially functional. The area of DRAM occupied by FDOS is refreshed but other areas are not, so programs occupying these areas die gradually.

SYMPTOM 23:

The IEEE-488 port does not communicate with parallel devices.

NOTE

The software reads the DIP switch (S1) to set the IEEE-488 address and RS-232-C baud rate. Switch S1 controls this function directly.

POSSIBLE CAUSES:

- The switch setting is wrong. (See Figure 2-4 in Section 2.)
- The IEEE-488 Controller (U67) is faulty.
- The Data Buffer is faulty.
- The Control Buffer is faulty.
- The connector is faulty.

ACTION:

Run the RS-232-C Port-to-Port Loopback Test in the System Diagnostic software. (See the heading Subtest Descriptions, earlier in this section.)

SYMPTOM 24:

The system will not communicate with devices over the RS-232-C port.

POSSIBLE CAUSES:

- The systems' baud rates don't match.
- Handshaking is incompatible.
- The interface UART (U61) is faulty.
- The buffer (U77, U83) is faulty.
- The connector or cable is faulty.

SYMPTOM 25:

The SBC will not communicate over the ARGUS/AGGIE bus.

POSSIBLE CAUSES:

- The Address Buffer (U9, U10, U11) is faulty.
- The interface Logic (U20, U22, U23, U63, U64,) is faulty.
- The WAITGEN logic (U31) is faulty. If something is loading down the READY line or one of the chip select lines, WAITGEN may generate the wrong number of wait states.

ACTION:

Connect a terminal to the RS-232-C port and use it instead of a VGK for troubleshooting. Alternatively, run the RS-232-C Port-to-Port test in the System Diagnostic software. (See the heading Subtest Descriptions, earlier in this section.)

SYMPTOM 26:

Clock time incorrect after boot.

POSSIBLE CAUSES:

- One or more outputs of U25 are shorted.
- U24 is faulty.
- Battery is bad.

3-61. VGK FAULT ANALYSIS

3-62. Introduction

Once the problem has been isolated to the VGK module, the fault can be further isolated to a group of components by observing what appears on the CRT and by checking signals at critical points.

Although the VGK is a single-board computer, the approach to troubleshooting is different than that used to troubleshoot the SBC. Since VGK processes are not visible, except with very sophisticated equipment not normally found in the field, the following paragraphs use a symptom approach to problems rather than the process approach used on the SBC.

For troubleshooting purposes, the VGK can be thought of as a collection of subsystems. These subsystems are grouped into inputs, outputs, and processors. The inputs include: keyboard inputs, inputs from the SBC, and TSO inputs. The outputs include: keyboard outputs, video outputs, and outputs to the SBC. The processors are: the Character Generator, the Graphics Generator, and the CPU.

Failures can usually be isolated to one of the subsections of the VGK by watching the interaction of I/O and processors. For example: if none of the I/O is functioning, the most obvious cause would be something associated with the Microprocessor, since it is common to all I/O. Once the trouble has been isolated to a subsection, it will be necessary to check signal levels and line activity to further isolate the trouble. For example, in the case of the suspected bad processor, one should start at the point that is common to all other activity: the clock PAL (U22).

NOTE

Two programs on the Getting Started disk, "Lace" and "Wow," produce fairly complicated graphics displays. These programs may be useful in diagnosing problems with the VGK. Also, running the System Diagnostic's Character RAM or Vector Generator subtests in Loop Mode will exercise the VGK continually for troubleshooting purposes.

3-63. Symptoms

SYMPTOM 27:

The cursor is displayed, but the 1722A does not respond to keyboard. Characters are displayed during self-test and boot.

ACTION:

Boot up the System Diagnostic disk and touch the screen to see if the unit responds to the TSO input.

CONCLUSION:

If the unit responds to the TSO, but not the keyboard, and you know the keyboard to be good, the problem must be in the Keyboard Interface UART (U36).

SYMPTOM 28:

Characters or parts of characters are missing. Character message is garbled.

ACTION:

Check the Attribute PAL (U54). This symptom is often associated with overheating. Try cooling the chip to see if normal operation is restored. If so, check to see that all covers are properly installed with the vent holes on the cover matching those on the chassis (CRT side). Check GVID and CVID inputs for proper waveform and level. If only characters are to be displayed then GVID should be inactive. If only graphics should be displayed then CVID should be inactive. If the inputs are incorrect, replace the chip.

SYMPTOM 29:

Graphics displays appear as disjointed "fireworks", or graphics are displayed when no graphics should be present. Character display is otherwise normal.

ACTION:

Check Attribute PAL (U54) for proper input at TP12. The signal should be at a logic low if at that time no graphics should be displayed. If there is signal at this point, there are problems in the graphics section. If signals are correct, suspect the PAL (U54).

Assuming that PAL (U54) is OK, then suspect that its input signal from the Graphics Video Shift Register (U75) is faulty. At this point trouble becomes difficult to isolate because on power-up the DRAM is completely erased, and if there is a bad chip anywhere in the graphics system, garbage will be loaded into the DRAM and will be displayed continuously.

Look for particular types of erroneous graphics displays. For example, if it looks like a proper graphic form is trying to be loaded but is being repeated in the wrong position, suspect a bad Y-PAN, or vertical register chip (U83,U84), or a bad X-PAN, or horizontal register chip (U52,U91,U93).

SYMPTOM 30:

Characters are displayed at inappropriate times.

ACTION:

Check Attribute PAL (U54) for proper input at TP10. The signal should be logic low when no characters should be displayed. If the signal is high, suspect problems in the character generator section. If there are proper signals on both CVID and GVID (TP10 and TP12) inputs to the PAL, suspect the PAL (U54).

Assuming that the PAL (U54) is OK, try swapping Character Generator PAL (U32), Attribute Memory (U33), and Character Memory (U34), all of which are socketed.

SYMPTOM 31:

Garbled character display; characters are unrecognizable.

ACTION:

Check data I/O for Character RAM (U34). These are Output Latch (U27) and Input Buffer (U13). A catastrophic failure in one of these would probably cause no display at all. The most common failure is U13, the Data Input Buffer.

Another less common failure that will produce this symptom is the character address multiplexer (U21, U39, U44).

SYMPTOM 32:

Screen blooms up with sparkly display, odd or no characters are displayed. Both characters and graphics are distorted.

ACTION:

Check Clock PAL (U22) pins 12-19. Check for proper square wave output. Should be fixed period pulse train, not random.

SYMPTOM 33:

Unit doesn't respond to TSO.

ACTION:

Check the TSO, an item more likely to fail. Check U3 pins 2, 5, 7, 10 for output. Check U6 pins 2, 4, 6, 10, 12, 14 for input as you touch each TSO square going diagonally.

NOTE

There is a certain amount of protection against static, but static discharge can destroy U5.

SYMPTOM 34:

The screen starts out blank, then to inverse video, then looks like a snow storm, and finally ends up as a few dots and a cursor. The beeper makes strange noises.

ACTION:

Check Clock PAL (U22). This unit is temperature-sensitive, and when cooled may alleviate the problem. The problem will return, however, as soon as the temperature comes up again. Check that all covers are properly installed with the vent holes on the covers matching those on the chassis (CRT side). Replace the chip if the problem persists.

SYMPTOM 35:

Display shows extra dots in a vertical pattern on either side of the display when the Lace program is run. There are also extra dots with the Wow program.

ACTION:

Check DRAM chips (U58-U65). Cool chips one-by-one to see if normal operation is restored. If so, replace chip that is heat-sensitive.

SYMPTOM 36:

The Lace and Wow programs produce distorted display. Most diagonal lines steeper than 45 degrees are incomplete, consisting of only a few dots.

ACTION:

Check the output of the Graphics Video Shift Register (U75 pin 2). If it is high or floating, replace the chip. Sometimes the signal at pin 2 will look normal even though the chip is bad. If U75 is OK, the display will be all vertical lines when any DRAM chip is removed and Lace or Wow is run.

SYMPTOM 37:

Inverse video fills the screen. Varying degrees of distortion.

ACTION:

Check inputs to Attribute PAL (U54). If they are normal, U54 is suspect.

SYMPTOM 38:

Distorted characters, and a wide variety of other display distortion problems are displayed.

ACTION:

Check Doublesize PAL (U40). Incorrect outputs at any of the pins can cause problems associated with those outputs, which are implemented by Attribute PAL (U54).

SYMPTOM 39:

Wrong characters are displayed; the display is filled with exclamation points or asterisks or other characters. The message LOADING and other messages are misspelled or consist of random characters. All words are misspelled, but the disk will boot and programs can be run.

ACTION:

Check Character RAM Input Buffer (U13).

SYMPTOM 40:

Horizontal bars appear across the screen (graphics problem). The screen is filled with narrow horizontal bars that will not erase. The Lace program will not erase the screen. However, the Wow program will erase.

ACTION:

Check X-Pan Registers (U52, U91, U93). This problem may be hard to find because there may be signals of proper amplitude but wrong frequency. For example, there may be no output from U52 pins 12, 13, or 14, but this chip may be good. Check to see that the pulse frequency at U52 pin 10 is high enough as compared to a normal board, if not, check outputs at U93 pins 11, 12, 13, and 14. Here again, if too few pulses are seen at U93 pin 10, check for pulse train at pin 10 of U91. Pins 10 and 15 pass the PCLK signal through, so the chip that fails to pass PCLK through is faulty. If PCLK is not seen at U91 pin 10, check inputs and outputs at U47.

SYMPTOM 41:

Vertical bars appear across screen. (See Symptom 40.)

ACTION:

Check Y-Pan registers (U83 and U84). (See action for Symptom 40.)

SYMPTOM 42:

When the Lace program is running, the graphics pattern has double image and is not complete and displays only segments of lines.

ACTION:

Check Address Multiplexer chips (U69, U94, U79, U97). Waveforms may prove to be normal even though one of these chips is bad. Shorting out PA address lines may produce similar results. Swap chips one-by-one until the problem is isolated.

SYMPTOM 43:

Screen is completely in inverse video and is blinking.

ACTION:

Check Data bus lines for correct signals. This particular symptom is caused by an open D07 (U15 pin 11).

SYMPTOM 44:

Display is all inverse, except that the highlighted message FLUKE 1722A/1752A shows up at power-up. All other normal-intensity characters are masked out.

ACTION:

Check the Chip Select Logic (U74, U77), and Input Shift Register (U73). The following lines, which should not be high, may be high: U74 pins 9 and 10; U73 pin 9. If these conditions exist, Input Shift Register (U73) is suspect.

3-64. KEYBOARD FAULT ANALYSIS

SYMPTOM 45:

Keyboard LEDs do not light and a beep is not heard on power-up.

POSSIBLE CAUSES:

- No power to circuitry.
 1. Bad connection in cabling between Motherboard and Keyboard.
- Microcomputer (U2).
 1. Bad crystal.
 2. Bad level on Reset pin.
- U3 is nonfunctional.

SYMPTOM 46:

Some keys work and others do not.

POSSIBLE CAUSES:

- Key contacts are dirty.
- Row driver in U1 is bad. (All keys in one row of the keyboard map will malfunction.)

SYMPTOM 47:

The keyboard beeps and LEDs come on, but no keys on the keyboard work.

POSSIBLE CAUSES:

- Two or more key contacts are stuck closed.
- A row or column is shorted.

3-65. PUP FAULT ANALYSIS

SYMPTOM 48:

DCOK remains low after the unit is powered up.

POSSIBLE CAUSES:

- Power supply voltages are below minimum limits.

ACTION:

- Check TP1, TP2, and TP3 for proper operating voltages.

3-66. Troubleshooting OEM Modules

For troubleshooting information regarding modules not of Fluke manufacture (the power supply, CRT, and floppy disk drive), see the respective OEM manuals included in this service manual.

3-67. ACCESS PROCEDURES

3-68. Introduction

The following procedures allow the user to remove and replace any of the modules or assemblies mentioned in either of the diagnostic procedures found at the beginning of this section. The term module refers to one of the pcbs within the card cage. The term assembly denotes other replaceable portions of the 1722A. Each procedure has its own heading and appears in the table of contents.

WARNING

UNPLUG THE AC LINE CORD BEFORE PERFORMING ANY ACCESS PROCEDURES.

WARNING

HIGH VOLTAGE IS PRESENT WITHIN THE CRT AREA. TO AVOID ELECTRIC SHOCK, DO NOT PUT YOUR HANDS OR METALLIC IMPLEMENTS INTO THIS AREA.

3-69. External Line Fuse Replacement

1. Referring to Figure 3-10 for the 1722A or Figure 3-11 for the 1752A, locate the fuse on the back panel below the POWER ON-OFF switch.
2. Insert a coin or other suitable tool in the slot in the fuse holder.
3. Turn counterclockwise 1/8-turn.
4. Withdraw the fuse holder.
5. Install an identical new fuse in the fuse holder. For 120V ac operation, install a 3A slow-blow fuse; for 230V ac operation, install a 2A slow-blow fuse.

3-70. Top and Bottom Chassis Cover Removal

1. Refer to Figure 3-12. The top and bottom covers are retained by six countersunk screws. It is not necessary to remove the feet.
2. Remove the six retaining screws (A) from the top cover and set the cover aside.

3. Remove the six retaining screws (B) from the bottom cover and set the cover aside.

3-71. Power Supply Fuse Replacement

1. Remove the top chassis cover as described in the previous procedure.

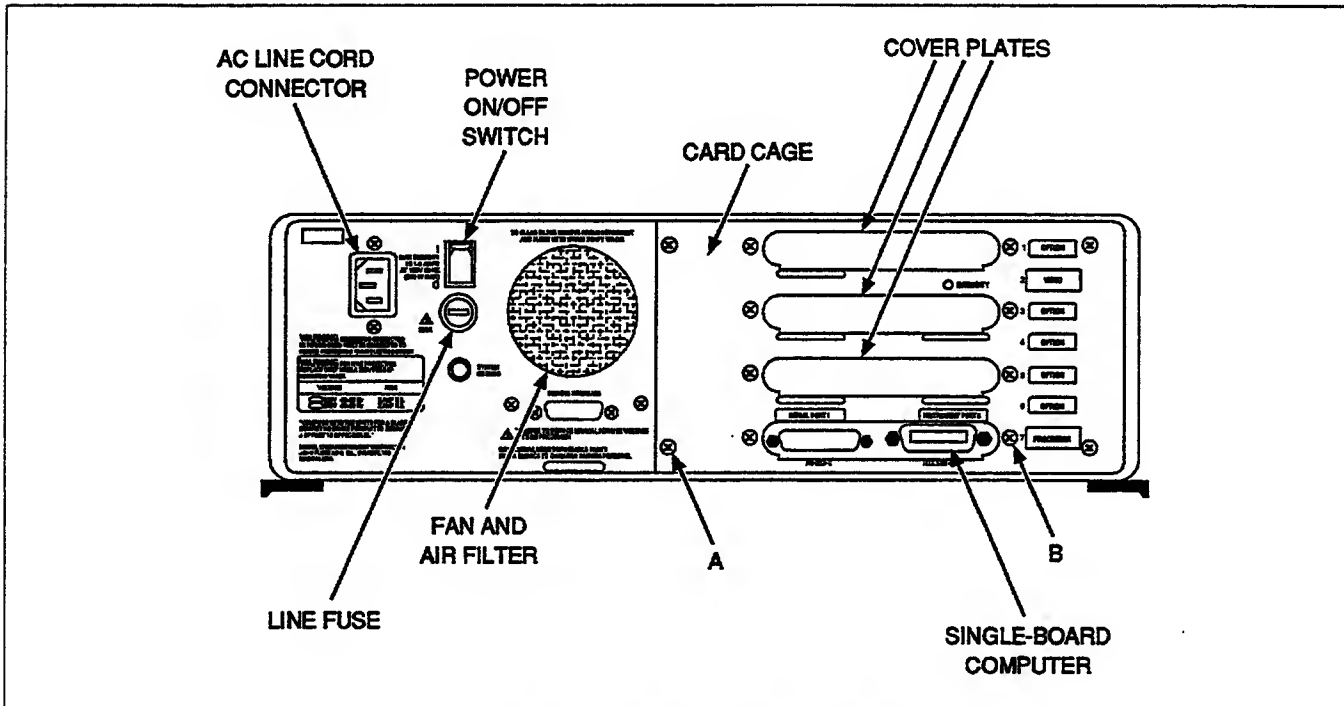


Figure 3-10. The 1722A Rear Panel

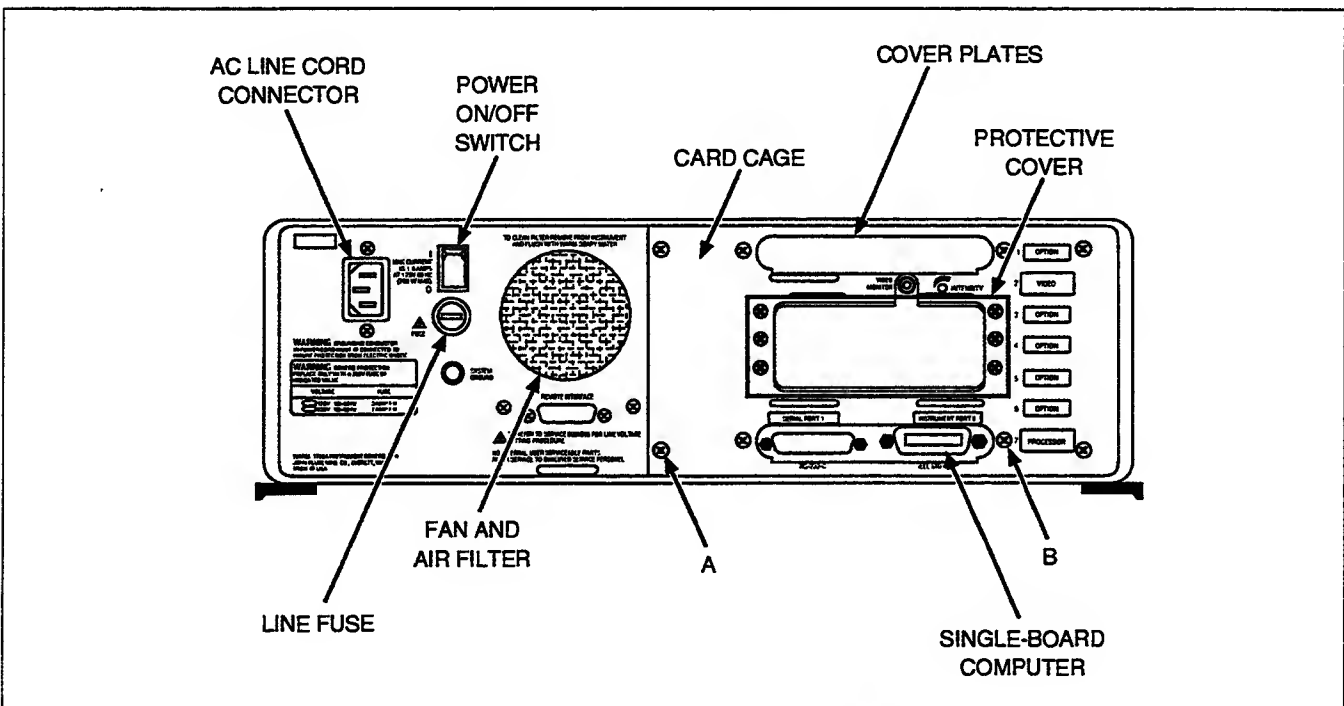


Figure 3-11. The 1752A Rear Panel

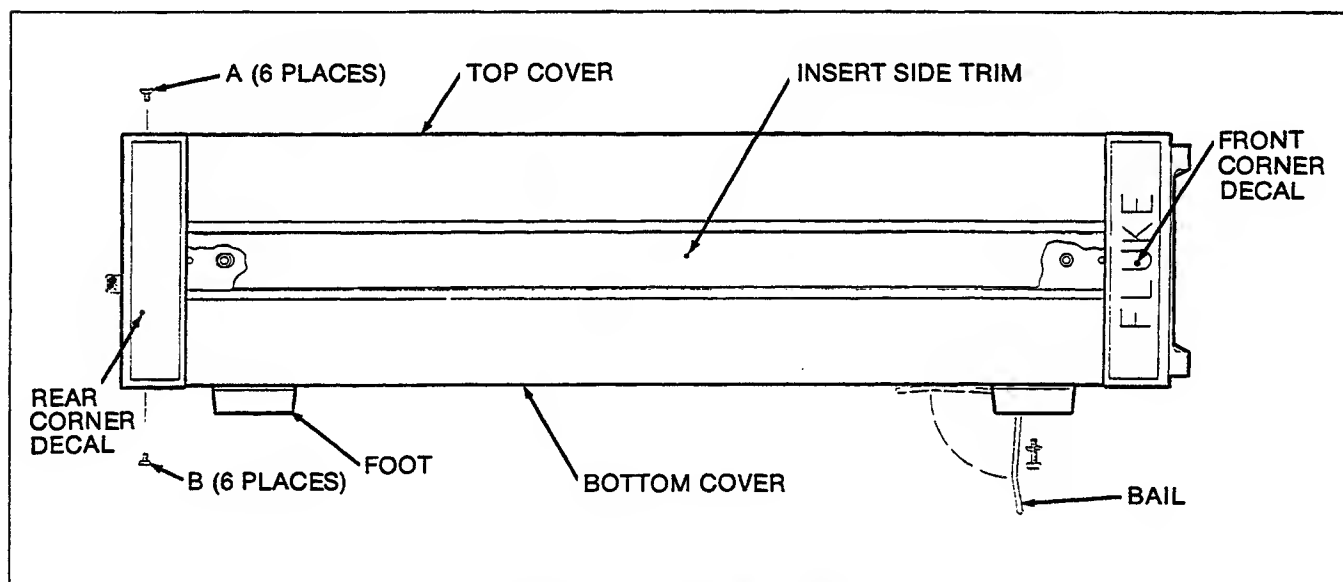


Figure 3-12. Left Side of Case

WARNING

HIGH-VOLTAGE CAPACITORS IN THE POWER SUPPLY RETAIN A CHARGE EVEN AFTER THE UNIT HAS BEEN POWERED DOWN. DISCHARGE CAPACITORS AS SOON AS THEY ARE ACCESSIBLE TO AVOID DANGEROUS ELECTRICAL SHOCK.

2. Remove the power supply top cover by removing the four retaining screws.
3. Locate the fuse mounted on the circuit card, immediately adjacent to the fan.
4. Grasp the fuse with an insulated fuse puller and pull the fuse from the retaining clips.
5. As appropriate per the power supply model, install an identical new fast acting fuse in the fuse clip as follows:
 - NPT Model NQ130: one (4A)
 - Boschert/CP Model XL160: two (2A and 5A)
 - CP Model XL200: two (5A and 10A)

3-72. Line Voltage and Frequency Selection

The unit comes from the factory set for either 115V ac (60 Hz) or 230V ac (50 Hz) unless specified further by the customer.

1. To set the line voltage, proceed as follows:
 - a. If not already performed, change the rear panel fuse as described above under "External Line Fuse Replacement."

- b. Remove the top chassis cover as described under "Top and Bottom Chassis Cover Removal."
- c. Remove the four retaining screws securing the top cover of the power supply, then remove this cover.
- d. Perform the appropriate voltage selection procedure based on power supply manufacturer and model number, as follows:

- CP model XL200

Voltage selection is made automatically. No changes are required on the power supply.

- CP or Boschert model XL160

Voltage is selected on the power supply by placing the slip-on jumper JP1 onto either E1 for 110V operation or E2 for 220V operation.

- NPT or IPT model NQ130

To set the unit for 230V ac operation, cut or unsolder one end of the select link labeled TEST JMPR. Secure any loose ends to prevent contact with any other conductor.

To set the unit for 115V ac operation, replace the cut link (if applicable) with a new one or resolder the loose end into the board, taking care to make a good solder joint.

- e. Replace the top cover of the power supply area and the instrument cover.
2. To set the line frequency, proceed as follows:
 - a. Remove the rear card cage cover as described in "Card-Cage Cover Removal".

- b. Remove the VGK from the unit and locate the 50 Hz jumper block by referring to the component layout diagram in the schematics section.
- c. To set the unit for 60 Hz operation, remove the jumper from the 50 Hz position (if applicable). This jumper is not used for 60 Hz operation.

To set the unit for 50 Hz operation, place a jumper (JF/PN 530253) over the two posts labeled "50".
- d. Reinstall the VGK in the chassis and replace the rear card cage cover.
- e. Power up the unit. If necessary, readjust the vertical hold on the video monitor and center the display as described in "Video Alignment".

3-73. Card-Cage Cover Removal

1. Referring to Figure 3-10 for the 1722A or Figure 3-11 for the 1752A, remove the four screws (A) that hold the card-cage cover to the back panel.
2. Remove the two screws (B) that hold the Single-Board Computer onto the card-cage cover.

NOTE

If options are installed which are screwed onto the cover, remove the screws holding them to the cover.

3. Remove the cover.

3-74. Disk Drive Access (Old Chassis, Figure 3-13)

1. Remove the top and bottom chassis covers as described under "Top and Bottom Chassis Cover Removal".
2. Refer to Figure 3-13. Unplug the disk drive power connector (C) at the motherboard.
3. Remove the four retaining screws (A) from the top cover of the disk drive and remove the cover to gain access to the card edge connector.
4. Unplug the ribbon cable (B) at the card edge connector.
5. Refer to Figure 3-14. Turn the 1722A on its side. Working from the bottom of the disk drive, remove the four retaining screws (A) from the bottom of the disk drive support chassis. Hold the disk drive during removal to avoid dropping it.
6. Remove the four screws on the disk drive cage and separate the cage from the disk drive.
7. Unplug the power connector from the disk drive.
8. To reassemble the disk drive, reverse steps 1 through 7.

NOTE

When reinstalling the ribbon cable, line up the red stripe on the cable with the keyed notch on the card edge connector (pin 1). Be sure to dress the ribbon cable carefully, so that it is remains below the edge of the chassis when the chassis cover is replaced.

3-75. Disk Drive Access (New Chassis, Figure 3-15)

1. Remove the top and bottom chassis covers as described under "Top and Bottom Chassis Cover Removal".
2. Refer to Figure 3-15.
3. Unplug the disk drive power connector (A) at the motherboard.
4. Push the disk drive backward with your thumbs until the cage is free of the slots in the disk drive support.

NOTE

If the disk drive does not glide smoothly, turn the 1722A on its side. Working from the bottom of the disk drive, hold on to the drive and loosen it by tapping firmly on the lip of the disk drive support with a screw driver handle.

5. Lift the disk drive and cage assembly out of the chassis and rest it on the video monitor cover.
6. Remove the four retaining screws on the side of the disk drive cover. Remove the cover.
7. Remove the ribbon cable (C) at the disk drive.
8. Remove the four screws on the side of the disk drive cage and separate the cage from the disk drive.
9. Unplug the power connector (A) from the disk drive.
10. To reassemble the disk drive, reverse steps 1 through 9.

NOTE

When reinstalling the disk drive, check the alignment of the disk drive and bezel. Pressing the disk drive too firmly forward will inhibit the operation of the disk drive door.

When reinstalling the ribbon cable, line up the red stripe on the cable with the keyed notch on the card cage connector (pin 1). The TEAC cable will require a 180 degree rotation of the cable for proper insertion.

3-76. Back Panel Removal

1. Remove the top and bottom chassis covers as described earlier.

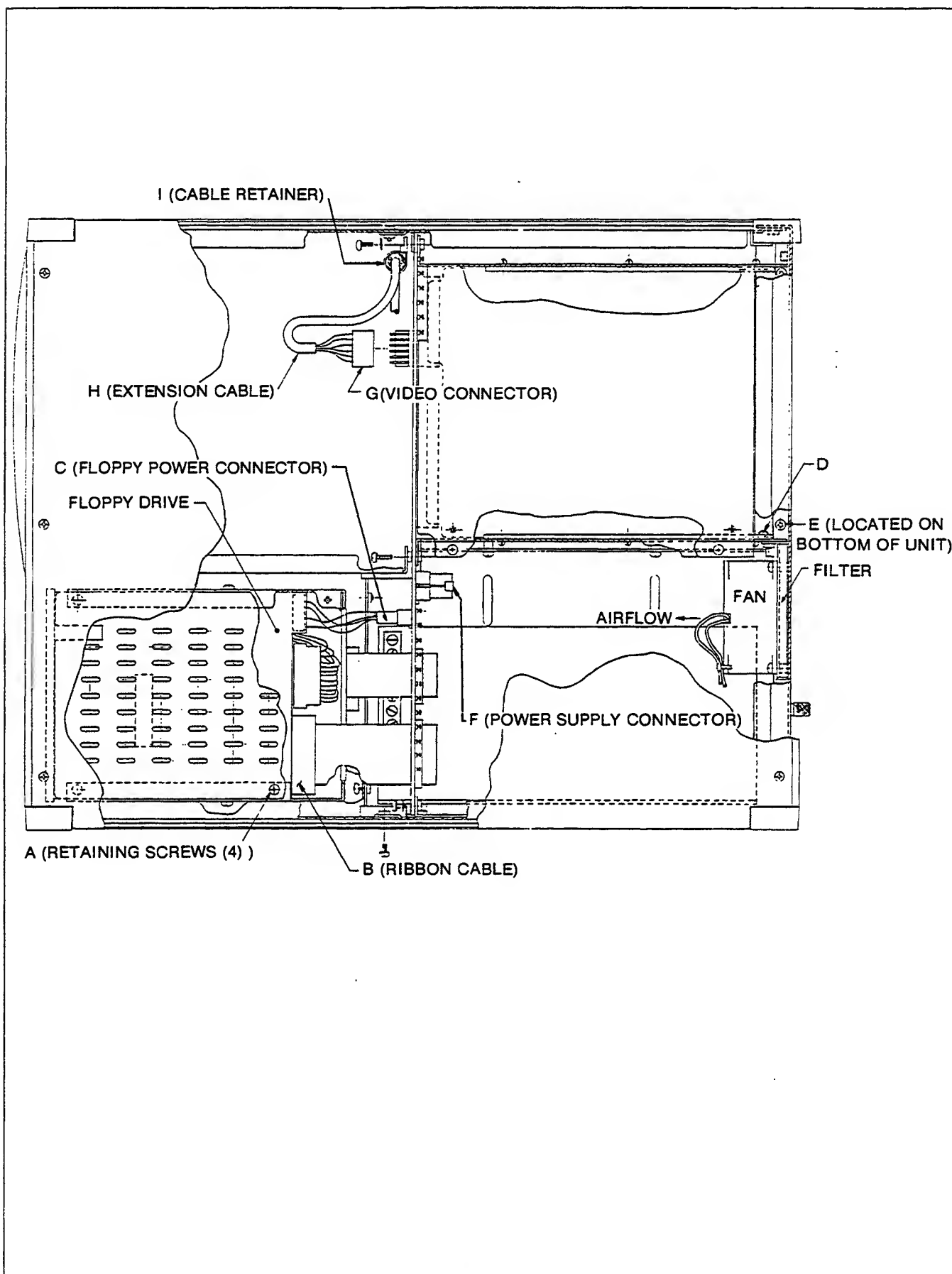


Figure 3-13. Top View of 1722A (Old Chassis)

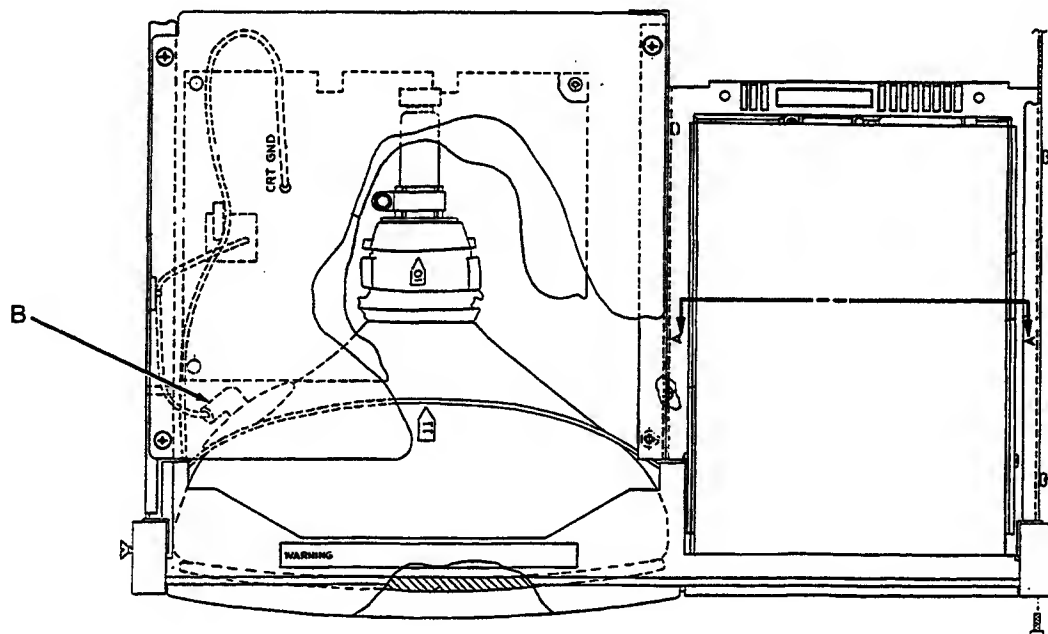
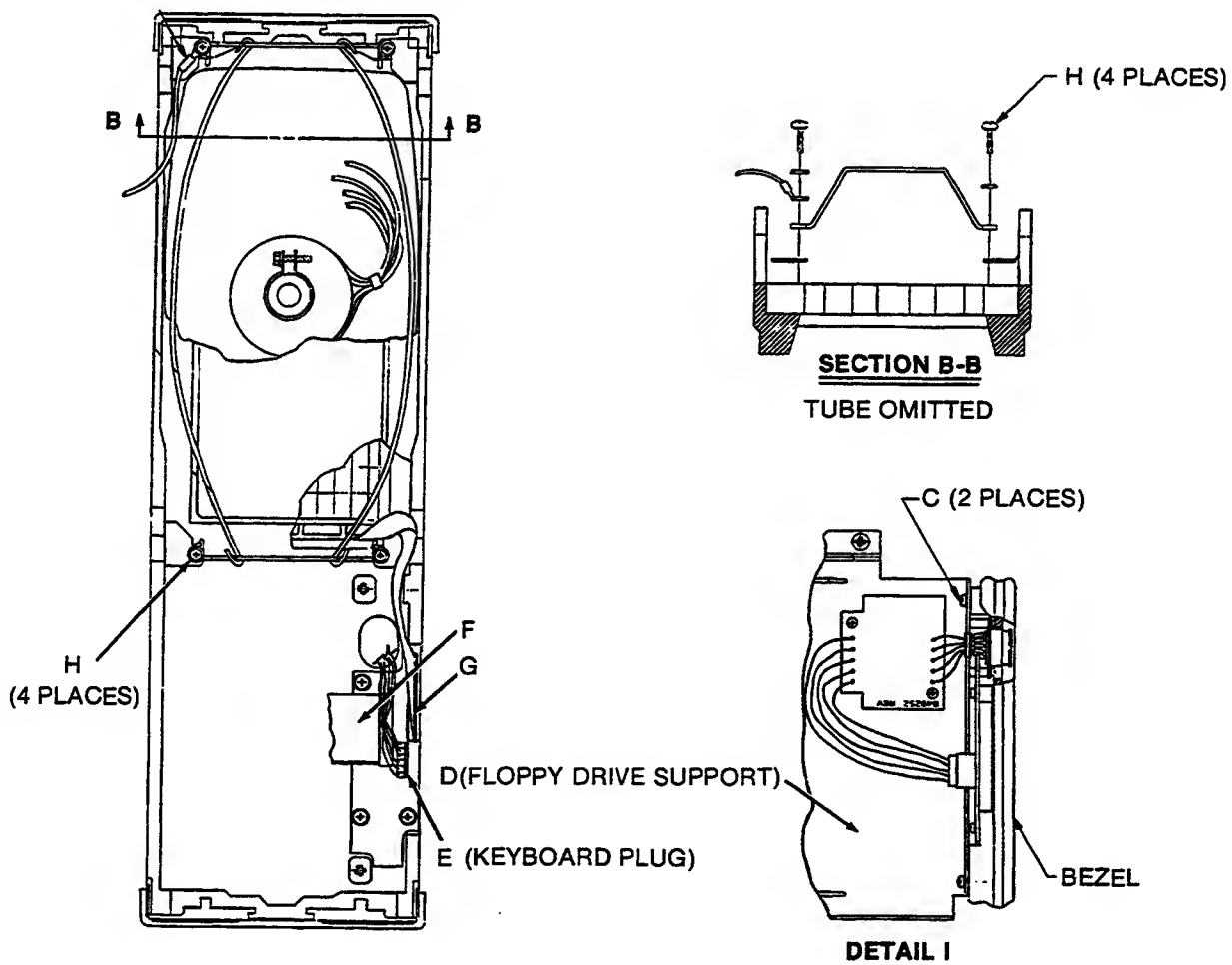


Figure 3-14. Front Panel Details

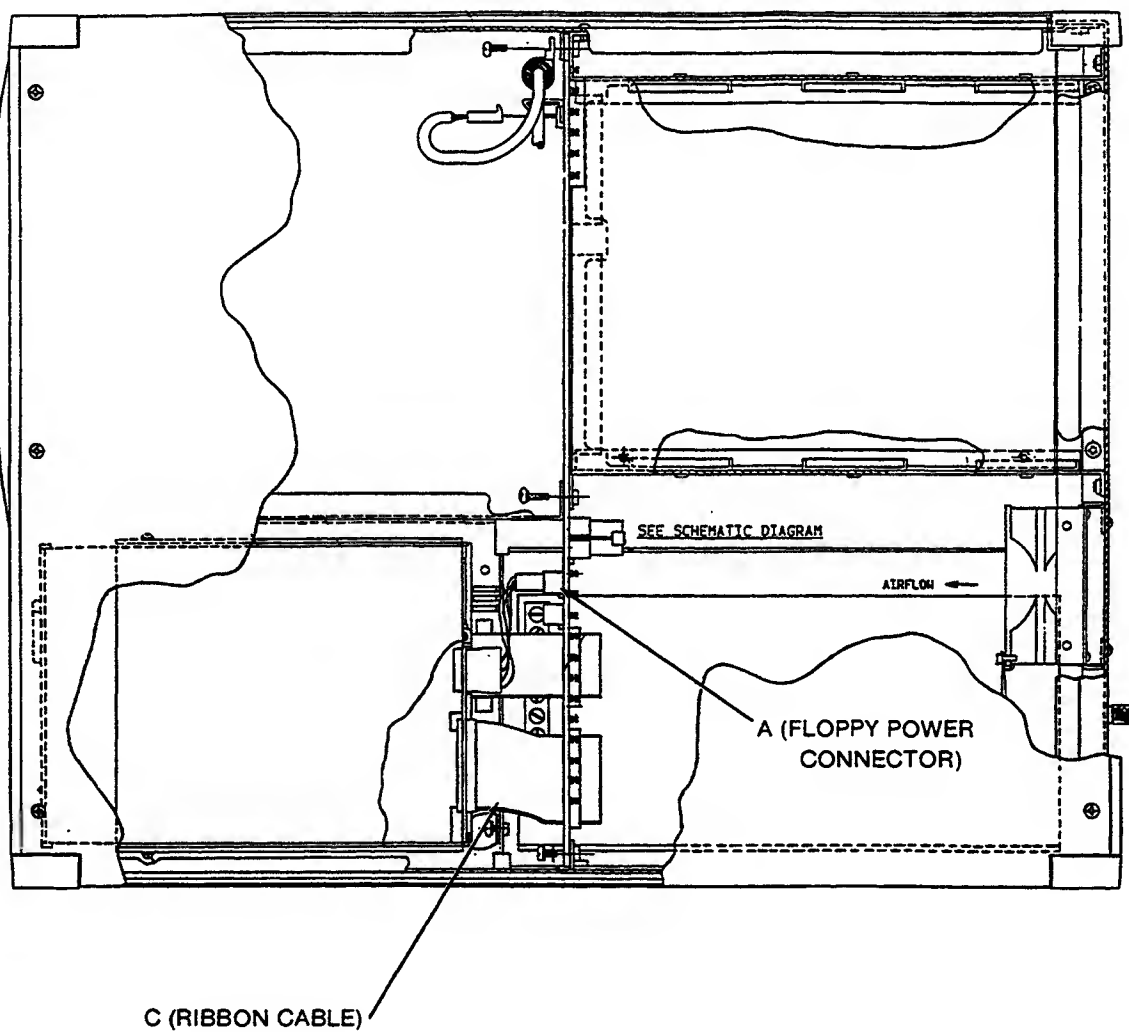


Figure 3-15. Top View of 1722A/1752A (New Chassis)

2. Referring to Figure 3-16, expose the power supply by removing the four screws (A) that retain the right rear module cover and remove the cover.
3. Unplug the fan wires from the PUP.
4. Remove the card cage cover as described in an earlier paragraph.
5. Remove the cards from the card cage, noting their positions in the cage.
6. Referring to Figure 3-17, remove the three screws (A) hidden behind each plastic facing on each of the two rear-corner lugs (B).
7. Referring to Figure 3-13, remove the two screws (D) from the left card-cage wall. The screws are immediately inside the opening.
8. Remove the single screw (E) from the bottom flange of the rear panel.
9. Work the back panel loose from the chassis and tilt it face down on the bench. Be careful not to unduly stress the ac wires attached to the power supply.
10. Remove the three ac wires from the power supply. The connectors are spade lugs. Note the position of each wire.

3-77. Fan Removal

1. Remove the top and bottom chassis covers as described earlier.
2. Remove the back panel as described earlier.
3. Referring to Figure 3-18, remove the four fan retaining screws (A).

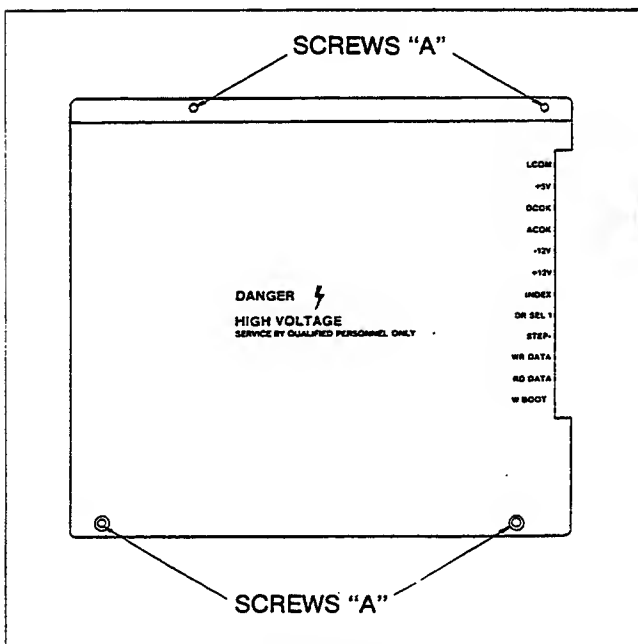


Figure 3-16. Power Supply Cover

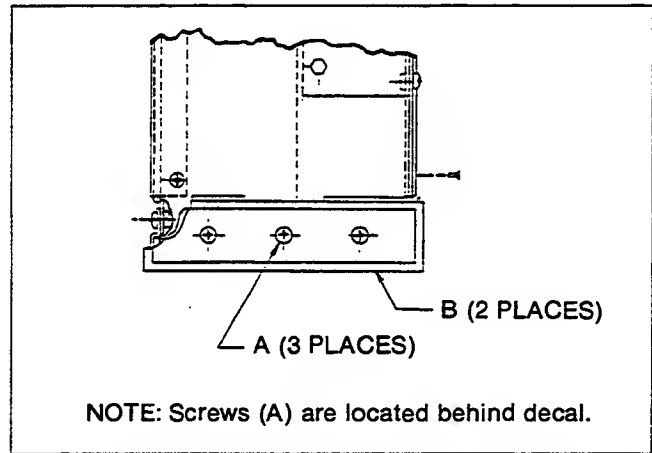


Figure 3-17. Detail of Rear Corner Lug

4. Cut the plastic tie wrap holding the fan wires.
5. Remove the fan.
6. After reassembling, install a new tie wrap on the fan and ac wires.

3-78. Power Supply Removal

WARNING

THERE IS A DANGER OF ELECTRICAL SHOCK FROM HIGH VOLTAGE STORED IN CAPACITORS. USE EXTREME CAUTION WHEN REMOVING THIS UNIT. DISCHARGE ALL CAPACITORS AS SOON AS THEY ARE ACCESSIBLE.

1. Remove the top and bottom chassis covers as described earlier.
2. Remove the back panel as described earlier.
3. Remove the four screws that hold the power supply to the chassis. The screws are accessible from the bottom.
4. Referring to Figure 3-13, unplug the connector (F) labeled POWER SUPPLY from the motherboard.
5. Slide the power supply back and lift it out.

3-79. Power-Up Assembly (PUP) Removal

1. Remove the top chassis cover as described earlier in Top and Bottom Chassis Removal.
2. Referring to Figure 3-16, remove the retaining screws (A) from the power supply cover, and remove the cover, exposing the power supply.
3. Unplug the fan wires from the PUP.
4. Remove the three retaining screws from the PUP circuit board.

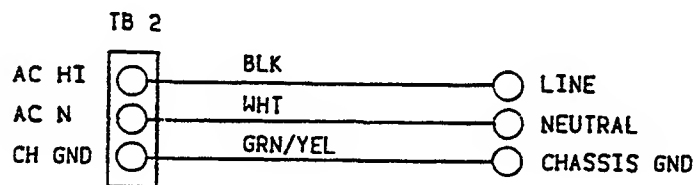
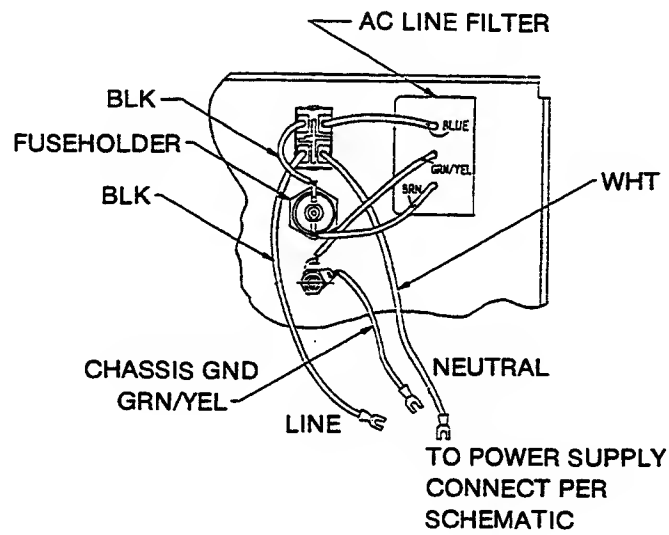
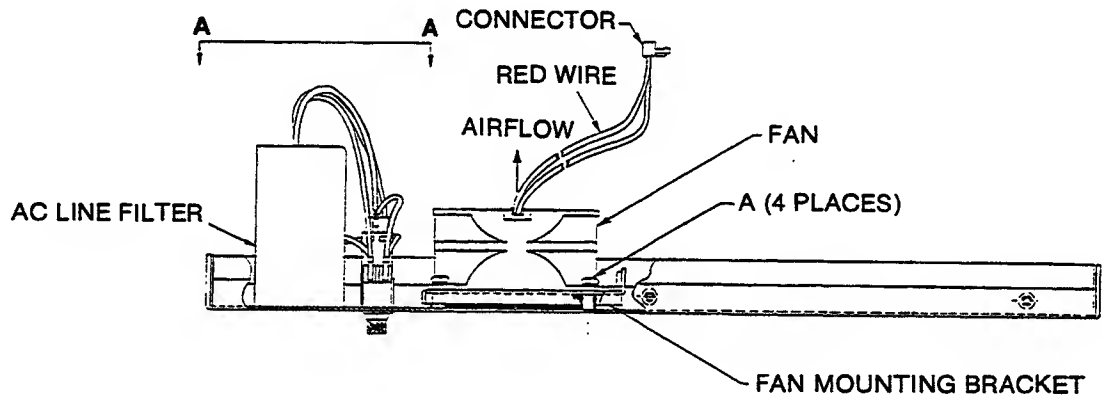


Figure 3-18. Rear Panel Details

5. Slide the PUP back out of its card-edge connector, and remove it from the chassis.

3-80. Video Monitor Circuit Card Removal

1. Remove the top and bottom chassis covers as described earlier.

NOTE

Two video assemblies have been used on the 1722A/1752A. On earlier models, a Ball or Dotronix assembly was used. These earlier assemblies require that you perform the following discharge procedure. On newer models, a Data Ray assembly is used. The Data Ray assembly incorporates a bleeder resistor: no discharge procedure is required (you can proceed directly to step 3.) In all cases, use the discharge procedure if the video assembly manufacturer cannot be determined.

2. Referring to Figure 3-14, discharge the CRT as follows:

WARNING

BOTH THE CRT ANODE AND THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. IN THE CASE OF THE CRT ANODE, THIS CHARGE CAN BUILD BACK UP EVEN AFTER BEING DISCHARGED BY THE PROCEDURE THAT FOLLOWS. ALTHOUGH IT DOES NOT CONTAIN ENOUGH ENERGY TO BE HARMFUL, THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

WARNING

MAKE SURE THE POWER IS OFF! DISCONNECT THE LINE CORD BEFORE STARTING.

- a. Connect one end of a 1 k Ω resistor to the chassis with one clip lead.
- b. Connect the other end of the resistor to the shaft of the 9-inch screwdriver with the 1/4-inch tip, using the other clip lead.
- c. Hold the screwdriver by its plastic handle and gently slip it under the edge of the plastic nipple (B) on the CRT end of the high voltage lead; keep the blade flat against the glass envelope.
- d. Slide the blade forward until the screwdriver blade touches the metallic clip at the end of the

high voltage lead. Be careful not to scratch the surface of the CRT.

3. Squeeze the high-voltage anode wire connector and detach it from the side of the CRT.

NOTE

Notice how the high voltage cable is routed. It is important to copy this routing when reconnecting the high voltage lead because it minimizes corona losses by staying as far as possible from all grounded surfaces.

4. Turn the unit so that it is right side up.
5. Remove the four screws that retain the top of the monitor module.
6. With the front of the instrument facing you, lift the right edge of the cover, noting that the Video Monitor Circuit Card is screwed to the bottom.
 - a. Unplug the plugs that are connected to the circuit board.
 - b. Unplug the green ground wire from the circuit board, straighten it, and pull it from underneath the circuit board.
 - c. Pull the video cable (H) through its retainer (I) to gain enough slack cable to set the cover and circuit board upside down on the card cage.
7. Unplug the cable from the card-edge connector or post header, depending on the version of the circuit board installed.
8. Remove the Video Monitor Circuit Card from the cover by removing the four retaining screws.

3-81. Front Panel Removal

WARNING

BOTH THE CRT ANODE AND THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. IN THE CASE OF THE CRT ANODE, THIS CHARGE CAN BUILD BACK UP EVEN AFTER BEING DISCHARGED. ALTHOUGH IT DOES NOT CONTAIN ENOUGH ENERGY TO BE HARMFUL, THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

NOTE

The front panel and the CRT are most easily removed as an assembly.

1. Remove the top and bottom chassis covers as described earlier.
2. Remove the Video Monitor Circuit Card as described earlier.
3. Referring to Figure 3-14, remove the two screws (C) that secure the front panel to the floppy drive support (D).
4. Unplug the keyboard plug (E) from the front panel.
5. Unplug the two ribbon cables (F and G) from the front panel.
6. Referring to Figure 3-12, remove the two front corner plastic decals (imprinted with the Fluke logo) from the front corner lugs.

NOTE

The decals must be replaced with new ones when reassembling the instrument.

7. Remove the two screws that were hidden behind the front corner decals on each of the front corner lugs.

WARNING

BE CAREFUL WHEN YOU HANDLE THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMplode.

8. Carefully pull the front panel and CRT, as a single assembly, away from the chassis and set the assembly aside in a safe place.

3-82. CRT Removal

WARNING

BE CAREFUL WHEN YOU HANDLE THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMplode.

1. Remove the front panel as described in the previous procedure.

NOTE

The CRT is positioned with the anode towards the floppy drive and must be reinstalled in the same way, or the display will be upside down.

2. Referring to Figure 3-14, remove two of the four screws (H) that hold the wire CRT retainer to the front panel. The screws are under tension, so hold the retainer down with one hand while loosening the screws.
3. Remove the retainer.
4. Work the CRT loose from its foam seat.
5. Carefully remove the CRT from the front panel and set it aside in a safe place, face down on a soft surface.

3-83. Touch Sensitive Overlay (TSO) Removal

1. Remove the CRT as described in the previous heading.
2. Referring to Figure 3-14, make sure the TSO ribbon cable (G) is unplugged from the front panel.
3. Carefully work the TSO loose from its foam mounting and set it aside. The TSO can be easily scratched, so put it in a safe place.

3-84. CALIBRATION AND ALIGNMENT

3-85. Required Equipment

The following special equipment is required for this procedure:

- Alignment Gauge (P/N 884739)
- Alignment Tool Set (P/N 572321)

3-86. Preparation

1. Remove the instrument's top and bottom chassis covers.
2. Turn power ON and allow a 30-minute warm-up period before making any adjustments or measurements.
3. Referring to Figure 3-19, modify the Alignment Gauge using the following procedure:
 - a. Trim the excess mylar to not less than 1/16-inch of the outside, solid double-line border of the gauge.
 - b. Using a hole punch, punch holes in two of the empty areas of the gauge (away from any lines.)
 - c. Place clear tape over these holes. When pressed against the 1722A/1752A screen, this tape will hold the gauge securely in place.
 - d. As shown in Figure 3-19, place a third piece of tape on an empty part of the gauge. Use this tape as a handle when removing the gauge.

4. Place the Alignment Gauge inside the outer face of the 1722A/1752A bezel. Center the gauge in the bezel by hiding the outer solid line just beneath the bezel (all four sides.) Press on the tape-covered holes to adhere the gauge to the screen.
5. Load the System Diagnostic Disk and display the alignment pattern (subtest menu of the Video Graphics Keyboard - VGK).
6. Adjust the EXTERNAL INTENSITY control on the VGK clockwise to maximum.
7. On the Video Monitor Assembly:
 - Adjust the CONTRAST and SUB BRIGHT controls counterclockwise to maximum.
 - Then adjust the MAIN BRIGHT control until the raster is barely visible on the CRT.
 - Now readjust SUB BRIGHT until the raster disappears.
 - Finally, turn the CONTRAST down until the test pattern is comfortably readable.

3-87. Video Alignment Procedure

Vertical lines on the gauge should coincide with the vertical bars of dollar signs (\$) and the brackets ([]) of the alignment pattern. Horizontal lines of the gauge should coincide with the center crossbars of the eights (8's) of the pattern. Figure 3-20 identifies alignment ideal and limit points.

The outer lines of the alignment gauge denote how far the alignment pattern can vary and still be within specification. Alignment is within specification until the character touches an outer line of the gauge.

NOTE

To obtain consistent readings, view the CRT and gauge straight-on. You can ensure the correct viewing angle by looking for your eye's reflection in the intended area. Making observations with one eye closed also aids in proper viewing alignment.

On the Video Monitor Assembly, adjust the video alignment as necessary using the following adjustments. Refer to Figure 3-21 (for Ball/Dottronix video boards) or Figure 3-22 (for Data Ray video boards) to identify adjustment locations. Verify that all text of the alignment screen falls inside the limits of the gauge.

3-88. CENTERING 1 (LEFT & RIGHT)

Use HORIZONTAL PHASE to align the center columns of the video test pattern to the Alignment Gauge. In this step, do not center the video left-to-right by adjusting CENTERING RINGS.

3-89. CENTERING 2 (UP AND DOWN)

Use CENTERING RINGS (on the neck of the CRT) to align the center rows of the video test pattern to the Alignment Gauge.

3-90. VERIFY ROTATION

Verify that the display is not rotated by comparing the center vertical columns and the horizontal rows of the video test pattern to the Alignment Gauge. If rotation is apparent, loosen and rotate the yoke.

CAUTION

Use care when tightening the yoke. The securing bolt should be torqued to 6 inch-pounds; over-tightening can cause damage to the CRT neck.

NOTE

Use only slight adjustments for the following pincushion/barrel, horizontal, and vertical alignment procedures.

3-91. PINCUSHION/BARREL CORRECTION

Correct the display geometry for pincushion and barrel distortion (in vertical and horizontal axes.) Adjust the yoke magnets or add yoke magnets to make these corrections.

3-92. HORIZONTAL ALIGNMENT 1

Using HORIZONTAL PHASE, align the center columns of the video test pattern to the Alignment Gauge.

3-93. HORIZONTAL ALIGNMENT 2

Adjust display width with the WIDTH coil (located on the yoke.) Adjust this coil until the right column of the video test pattern falls between the right lines of the Alignment Gauge.

3-94. HORIZONTAL ALIGNMENT 3

Working from under the video board, adjust the HORIZONTAL LINEARITY coil. Adjust this coil until the left column of the test pattern coincides with the appropriate line on the Alignment Gauge.

3-95. HORIZONTAL ALIGNMENT 4

In order, repeat Horizontal Alignments 1, 2, and 3 until center, right, and left columns are all in alignment.

3-96. VERTICAL ALIGNMENT 1

Adjust the CENTERING RINGS until the top row (8's) of the test pattern falls between the appropriate lines on the Alignment Gauge.

3-97. VERTICAL ALIGNMENT 2

Adjust the VERTICAL SIZE control to position the bottom row (8's) of the test pattern halfway between its current position and the appropriate center line on the Alignment Gauge.

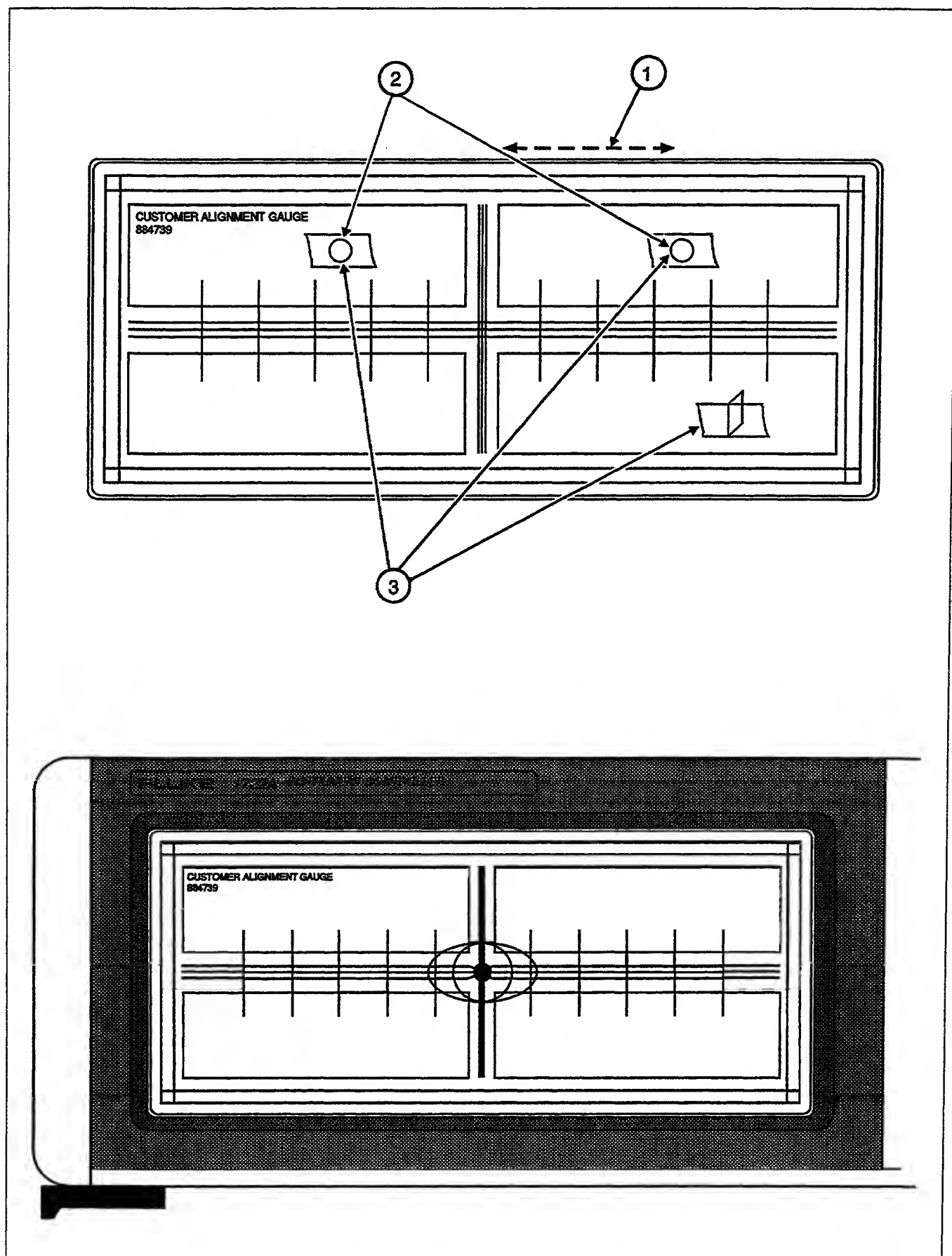
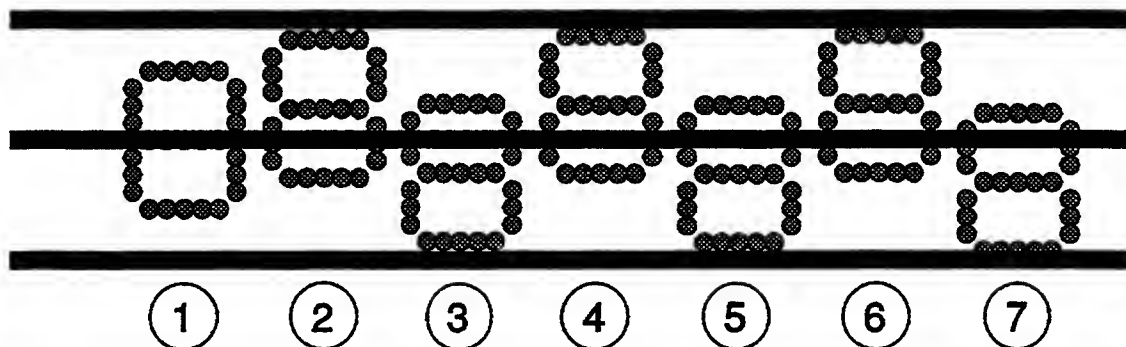
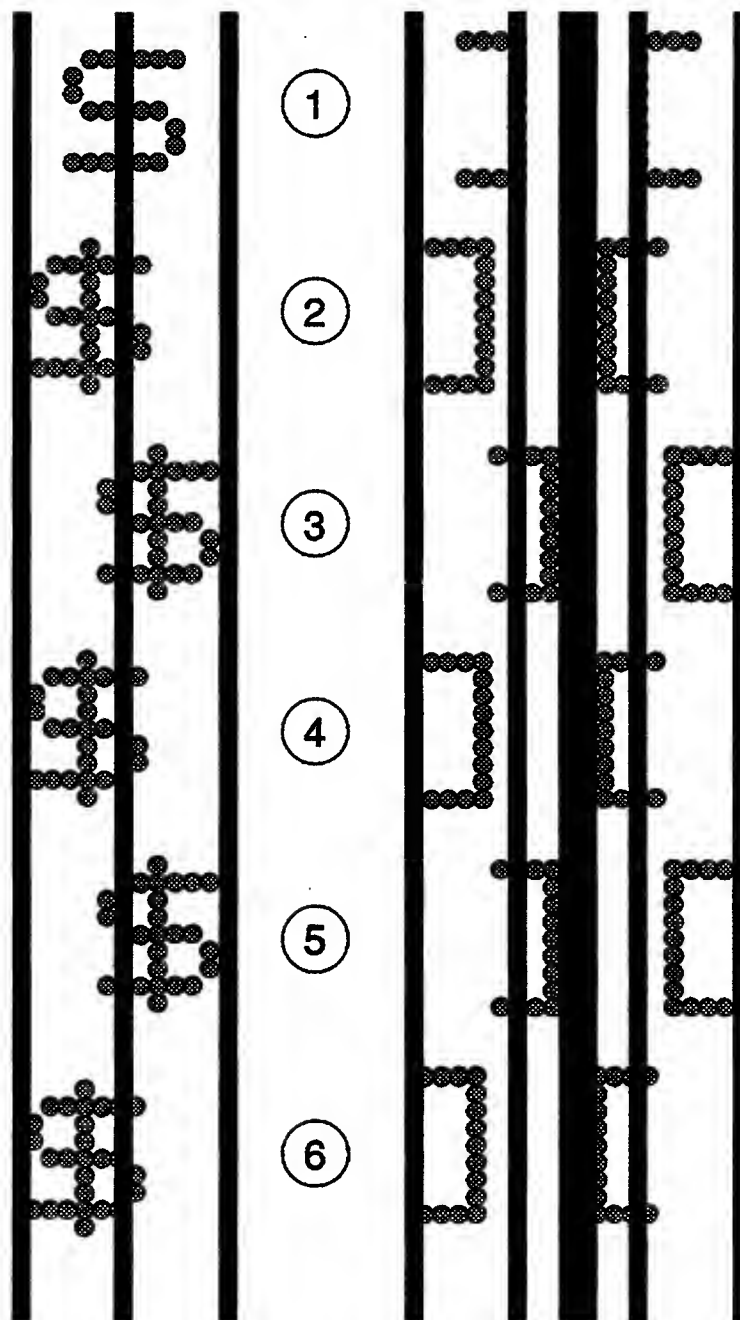


Figure 3-19. Alignment Gauge



KEY:

- 1) In alignment; centered
- 2, 3) In alignment; at extreme of tolerance. No shadowing, no decrease in character size.
- 4, 5) Out of alignment slight shadowing of character, decrease in apparent size.
- 6, 7) Out of alignment; increased shadowing of character.



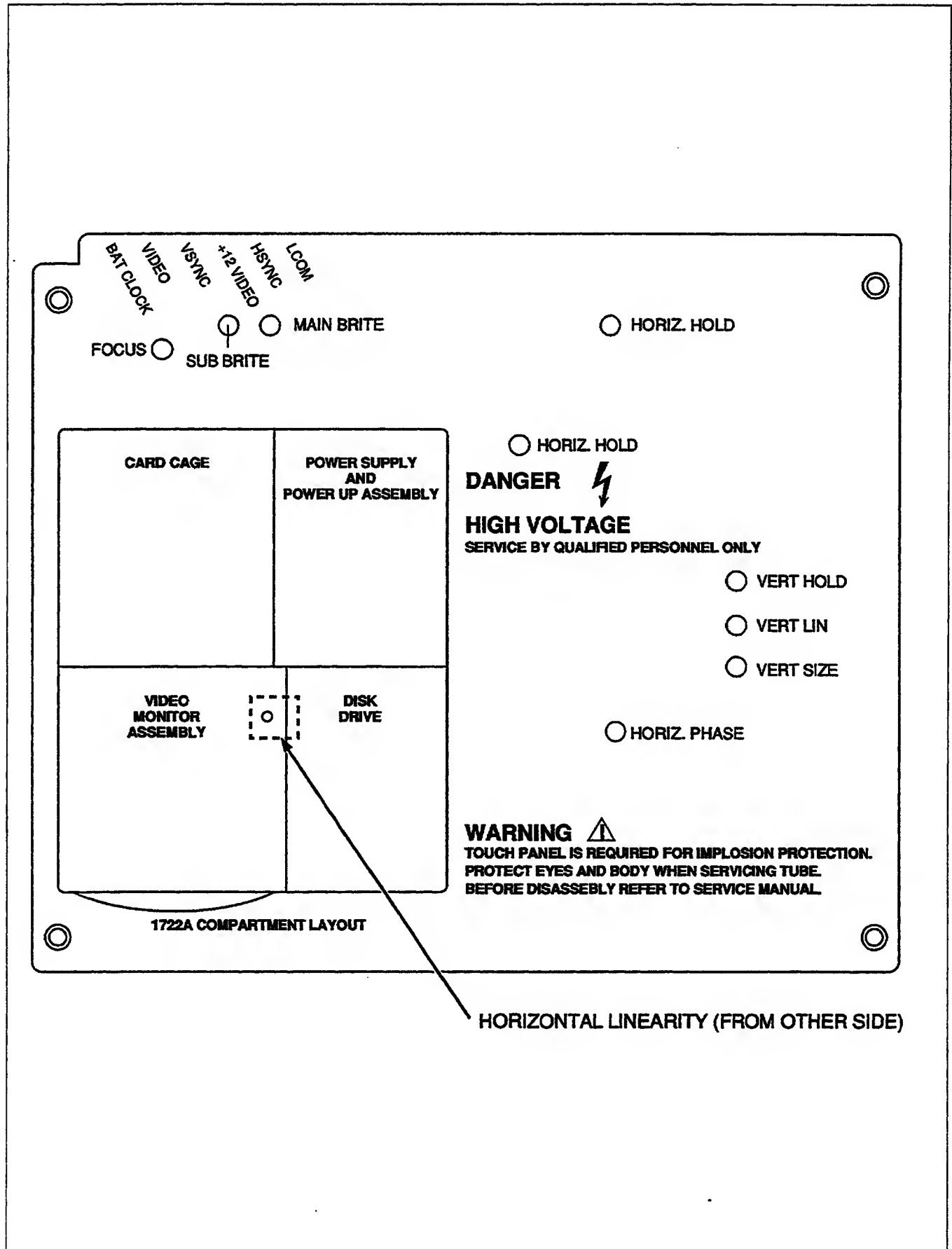
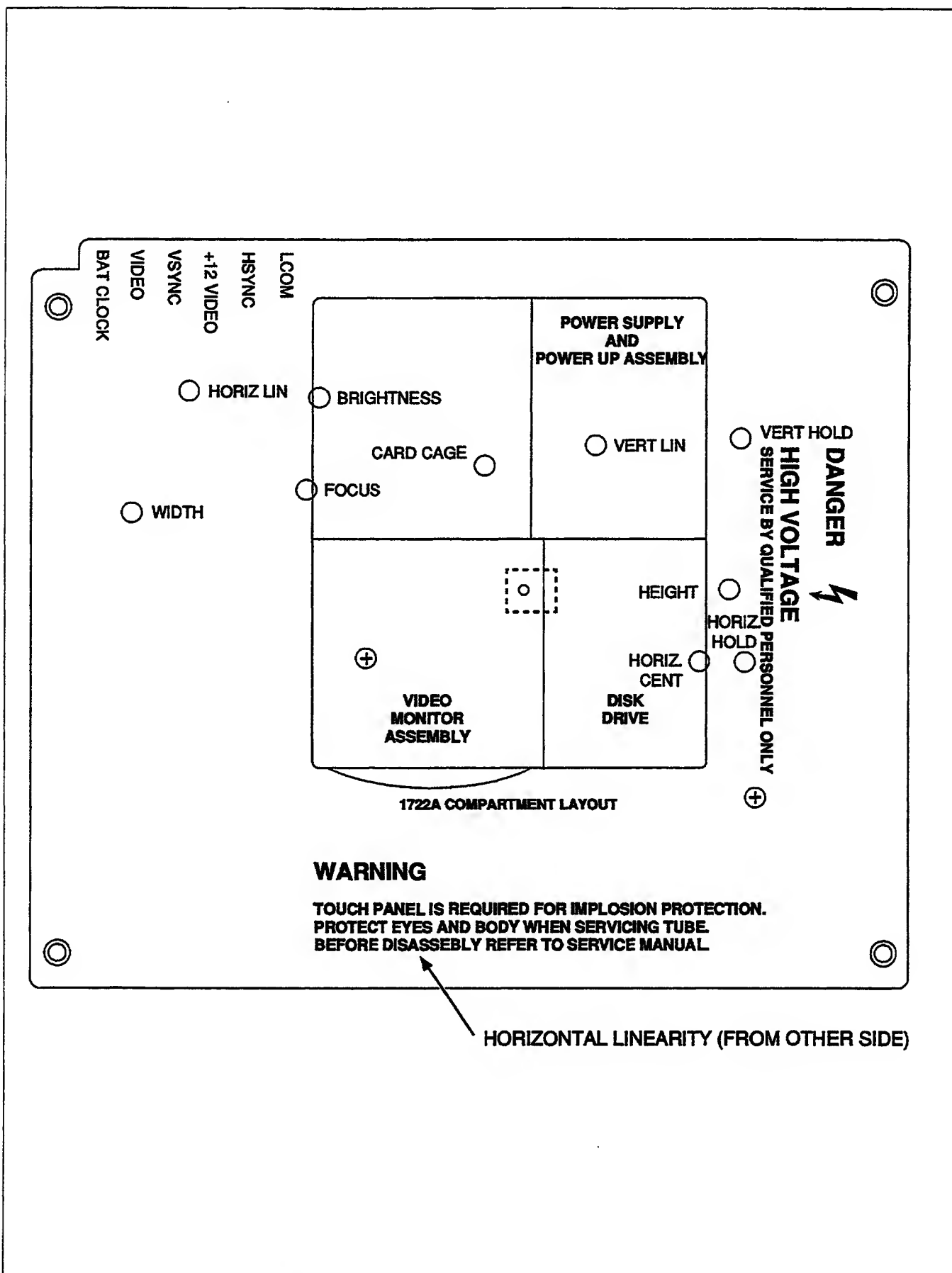


Figure 3-21. Video Adjustment Locations (Ball/Dottronix)



Then repeat Vertical Alignments 1 and 2 until the rows are in alignment.

3-98. VERTICAL ALIGNMENT 3

Adjust the VERTICAL LINEARITY control to position the center row (8's) of the test pattern halfway between its current position and the appropriate center line of the Alignment Gauge.

3-99. VERTICAL ALIGNMENT 4

Repeat Vertical Alignments 1, 2, 3, and 4 until the rows are in alignment. If all rows are in alignment after a specific vertical alignment is done, stop vertical alignment at that point.

3-100. CENTERING CHECK

Check again for correct centering. If necessary, perform Centering 1 and 2 procedures again. Then remove the Alignment Gauge, and check that the display is centered in the alignment pattern. If necessary, adjust the HORIZONTAL PHASE control slightly to center the display.

3-101. BRIGHTNESS CONTROL CHECK

Use the following sequence to check and adjust the brightness:

1. Adjust the CONTRAST control to maximum.
2. If necessary, adjust SUB BRIGHT until any visible raster disappears.
3. Adjust the CONTRAST control until the text is barely visible. Then reverse this control approximately 1/4 turn.
4. Adjust the EXTERNAL INTENSITY control on the VGK counterclockwise to a comfortable viewing level.

3-102. Floppy Disk Drive Speed Adjustment Procedure

The following adjustment procedure is for use with Shugart and TEAC Disk Drives used in earlier models.

NOTE

NEC and Panasonic disk drives were used after 2/1/1988. These drives incorporate phase-locked-loop speed circuitry and do not have any speed adjustments. If you encounter such a disk drive that is out of speed tolerance, consult your local Service Center for replacement.

1. For the Shugart drive, remove the top cover of the 1722A. For the TEAC drive, remove the bottom cover. (See the Access Procedures earlier in this section.)
2. Boot up the 1722A System Diagnostic Disk and select the disk-speed test as follows:

- a. Select "Test Menu" from the Main Menu.
- b. Select "All Off" then "Floppy Disk Drive" from the Test Menu.
- c. Select "Subtest Menu" from the Test Menu.
- d. Select "All Off" from the Subtest Menu.
- e. Select "Disk Speed Check/Adjust" from the Subtest Menu.
- f. Select "START TEST".

3. The disk speed is displayed in milliseconds per revolution. Use a Fluke Adjustment Tool (P/N 153049) to adjust the disk speed on the Shugart drive by inserting the tool through the slot in the top of the disk drive cover and adjusting the disk-speed pot on the disk drive. For the TEAC drive, insert the tool through the rectangular hole in the disk drive support bracket on the bottom of the drive. Adjust the speed to within the range of 197 to 206 msec.

CAUTION

To avoid damaging the disk drive, do not use a metal screwdriver to adjust the disk speed.

4. Touch the 1722A display to stop the test. Remove the disk and replace the top cover of the 1722A.

3-103. Floppy Disk Controller Calibration

The following procedures cover calibration of the floppy disk controller. There have been two types of floppy controllers used on the SBC. Current production assemblies (Rev F and later) use the WD1797 Floppy Controller with an external data separator and write precompensation circuit. Revision D assemblies used the WD2797 Floppy Controller, which has write precompensation and data recovery circuits built into the chip and requires a different calibration procedure.

The schematics section includes schematic diagrams and component location diagrams for both versions of the SBC.

3-104. PREPARATION

1. Turn the line power off.
2. Remove the SBC from the card cage.
3. Note the revision level marked on the assembly.
4. Put the SBC on an extender card.
5. Power the unit on without a disk installed in the drive and wait 10 minutes for the temperature to stabilize.
6. Move the calibration jumper from RUN to CAL.

NOTE

The SBC must be powered on with the jumper in the RUN position.

3-105. VCO FREQUENCY ADJUSTMENT (REV F AND LATER)

NOTE

This procedure requires a frequency counter (Fluke 7261A or equivalent).

3-106. Equipment Setup

Configure the frequency counter as follows:

- FREQ A
- AUTO resolution
- AC coupling
- X1 attenuation
- PRESET trigger
- + slope
- Use a X10 scope probe as the frequency counter probe

3-107. Adjustment

1. Connect the frequency counter probe to the VCO test point and logic ground.
2. Adjust the VCO trimmer pot (R25) until the VCO frequency is 500 kHz ± 5 kHz.

3-108. VCO FREQUENCY ADJUSTMENT (REV D ONLY)

NOTE

This procedure requires a frequency counter (Fluke 7261A or equivalent).

3-109. Equipment Setup

Configure the frequency counter as follows:

- FREQ A
- AUTO resolution
- AC coupling
- X1 attenuation
- PRESET trigger
- + slope
- Use a X10 scope probe as for the frequency counter probe

3-110. Adjustment

1. Connect the frequency counter probe to the VCO test point and logic ground.
2. Adjust the VCO trimmer cap (C110) until the VCO frequency is 210 kHz ± 1 kHz.

3-111. WRITE PULSE-WIDTH ADJUSTMENT (REV D ONLY)

NOTE

This adjustment requires an oscilloscope (Tektronix 425 or equivalent).

3-112. Equipment Setup

Configure the oscilloscope as follows:

- Trigger on channel 1
- + slope
- DC coupling
- 2V/div
- 0.05 μ s/div

3-113. Adjustment

1. Connect the scope probe to the WR PW test point and to GND.
2. Adjust the WR PW trimmer pot (R6) until the write pulse width is 250 ns ± 5 ns.

3-114. READ PULSE-WIDTH ADJUSTMENT (REV D ONLY)

NOTE

This procedure requires an oscilloscope (Philips PM-3065 or equivalent).

3-115. Equipment Setup

Configure the oscilloscope as follows:

- Trigger on channel 1
- + slope
- DC coupling
- 2V/div
- 0.1 μ s/div

3-116. Adjustment

1. Connect the scope probe to the RD PW test point and to GND.
2. Adjust the RD PW trimmer pot (R7) until the read pulse width is 500 ns ± 10 ns.

3-117. Button-Up

After all the alignments have been made:

1. Disconnect all test equipment.
2. Place the jumper back in the RUN position.
3. Turn off the power to the 1722A.
4. Place the SBC back into the 1722A chassis.

5. Replace and tighten the screws in the card cage cover.
6. Replace the top and bottom chassis covers.

3-118. PREVENTIVE MAINTENANCE

The Preventive Maintenance Program for the 1722A consists of three parts:

1. System Diagnostic Procedure
2. Filter Cleaning or Replacement
3. Cabinet and TSO Cleaning.

3-119. System Diagnostic Procedure

Run the System Diagnostic Procedure every 90 days. This ensures that the system is operating correctly.

3-120. Filter Replacement and Cleaning

Use the following procedure to clean the air filter on the rear of the instrument every 90 days or as site conditions dictate. The air filter is an exposed foam element located on the back panel. (See Figure 3-10 for the 1722A or Figure 3-11 for the 1752A.)

1. Place your fingers on the face of the foam filter element.
2. Slide the foam element to one side until one edge is exposed.
3. Grasp the exposed edge and pull gently.
4. The filter element will come out of the space between the back panel and the fan.

5. Clean the filter in warm water and soap. If the element is extremely dirty, replace it with a new filter.

NOTE

Do not use compressed air to clean or dry the filter element.

6. Reinstall the filter by sliding one edge into the slot and compressing the filter until all of it can be inserted flat into the space provided.

3-121. Cabinet and Touch-Sensitive Overlay Cleaning

Clean the Cabinet and Touch-Sensitive Overlay every 90 days or as site conditions dictate. Use a moist, soft (non-abrasive) cloth and a mild soap solution to clean them.

3-122. SHIPPING

If the Controller is to be returned to the factory or shipped to another location, use the original packing carton with all fillers properly in place. Fluke does not recommend shipping the Controller in a substitute container. To obtain an approved container, call any Fluke Sales Office.

In order to protect the magnetic head assembly in the disk drive from vibration and impact during transportation, be sure to insert the Disk Drive Shipping Insert into the disk drive. The insert is provided in the 1722A when it is shipped from the factory and is also available under Fluke part number 707984.

Section 4

List of Replaceable Parts

TABLE OF CONTENTS

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A2 Motherboard PCA	1722A-4002	4-5 4-18	4-3 4-19
A3 Power-Up (PUP) PCA	1722A-4003	4-6 4-20	4-4 4-21
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A5 Front Panel PCA	1722A-4005	4-8 4-25	4-6 4-26
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A6A1 Programmer's Keyboard PCA	1722A-4007	4-10 4-28	4-8 4-29
A12 Solar Cell PCA	1752A-4008	4-11 4-28	- -
A14 Keyboard Filter PCA	17XXA-4020	4-12 4-28	- -
Option -006 256K RAM Expansion PCA	1722A-4008	4-13 4-30	4-9 4-31
Option -007 512K RAM Expansion PCA	1722A-4008	4-13 4-30	4-9 4-31
Option -008 IEEE-488/RS-232-C Interface	1722A-4009	4-14 4-32	4-10 4-33
Option -009 Dual Serial Interface PCA	1722A-4010	4-15 4-34	4-11 4-36
Option -010 Analog Measurement Processor	1752A-4030	4-16 4-37	4-12 4-39
Option -011 Analog Output PCA	2400A-4009	4-17 4-40	4-13 4-42
Option -012 Counter/Totalizer PCA	2400A-4043	4-18 4-43	4-14 4-45
Option -016 1M RAM Expansion PCA	1722A-4008	4-13 4-30	4-9 4-31
Option -017 2M RAM Expansion PCA	1722A-4008	4-13 4-30	4-9 4-31
Option -018 256K NV RAM PCA (REV. 0)		4-20 4-47	- -
Option -018 256K NV RAM PCA (REV. A)	17XXA-4018-PH2-1	4-19 4-46	4-15 4-48
Option -019 512K NV RAM PCA (REV. 0)		4-20 4-47	- -
Option -019 512K NV RAM PCA (REV. A)	17XXA-4018-PH2-2	4-19 4-46	4-15 4-48
Option -020 1M NV RAM PCA	17XXA-4018-PH2-3	4-19 4-46	4-15 4-48
Option 1722A-440 Hard Disk, 40M		4-21 4-49	4-16 4-50
Option 1711A/AA-440 Winchester Hard Disk, 40M	1711A/AA-440	4-22 4-51	4-17 4-52

4-1. INTRODUCTION

This section contains an illustrated parts list for the 1722A. Parts are listed alphanumerically by assembly and reference designator. Each part listed is shown in an accompanying illustration.

The parts lists include the following information for each part:

1. Reference Designation.
2. Description.
3. Fluke Stock Number.
4. Federal Supply Code for Manufacturers. (See the back of this section for a list of names and codes.)
5. Manufacturer's Part Number.
6. Total Quantity of components per assembly.

4-2. REPLACEMENT MODULES, CABLES, AND CONNECTORS

Table 4-1 lists Fluke part numbers for all replacement modules in the 1722A Instrument Controller, as well as part numbers for the various loopback cables and connectors required for the IEEE-488 and RS-232-C tests.

4-3. FIELD SERVICE KITS

A Field Service Kit (Fluke P/N 729343) is available which contains the standard 1722A modules listed in Table 4-1. The standard 1752A modules, also listed in Table 4-1, are available in a Field Service Kit, Fluke P/N 767533. These kits are intended for use by qualified service personnel. Using Module Exchange as backup support, one kit should be sufficient to support approximately ten units.

4-4. REPLACEMENT PROMS AND PALS

The part numbers for PROMs (programmable read-only memory) and PALS (programmable array logic) vary according to the revision level of the PCA. Table 4-2 lists the part numbers for each revision level used.

4-5. HOW TO OBTAIN PARTS

Use the Fluke Stock Number when ordering all components from the John Fluke Mfg. Co., Inc. or an authorized representative. In the U.S., order directly from the Fluke Parts Dept. by calling 1-800-526-4731.

Some components may be ordered directly from the manufacturer using the manufacturer's part number.

In the event that the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Instrument Model and Serial Number
2. Fluke Stock Number
3. Reference Designator

4. Printed circuit assembly (pca) part number and revision letters
5. Description
6. Quantity

Price information for parts is available from the John Fluke Mfg. Co., Inc., and its authorized representatives. Prices are also available in a Fluke Replacement Parts Catalog, which is available on request.

CAUTION

A ⚡ symbol indicates a device that may be damaged by static discharge.

Refer to the end of this section for a list of technical service centers.

4-6. MANUAL STATUS INFORMATION

Assembly revision levels are documented in the "Manual Status Information" table later in this section. To identify the configuration of the pca's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pca.

4-7. NEWER INSTRUMENTS

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

4-8. TECHNICAL SERVICE CENTERS

A list of technical service centers is included at the end of this section.

4-9. PARTS LISTS

Refer to the following pages for parts lists of standard and optional assemblies.

List of Replaceable Parts
PARTS LISTS

Manual Status Information

REF	ASSEMBLY NAME	FLUKE P/N	REVISION LEVEL
A1	Video/Graphics/Keyboard (VGK) Interface Module	897483	M
A2	Motherboard PCA	699066	J
A3	Power-Up (PUP) PCA	704353	B
A4	Single-Board Computer (SBC) Module (1722A)	705285	N
A4	Single-Board Computer (SBC) Module (1752A)	767541	N
A5	Front Panel Assembly	704296	E
A6	Programmer's Keyboard	704387	F
A7	Keyboard Filter	849252	
002	17XXA-002 Parallel Interface	717397	
004	17XXA-004 Magnetic Bubble Memory (See Note)	657346 777235	
005	17XXA-005 Magnetic Bubble Memory (See Note)	657353 773391	
006	256K RAM Expansion Module	718684	F
007	512K RAM Expansion Module	718692	F
008	IEEE-488/RS-232-C Interface Module	718221	F
009	Dual Serial Interface	718734	B
010	Analog Measurement Processor	736876	F
011	Analog Output Module	610329	H
012	Counter Totalizer Module	630186	E
013	1752A-013 Mainframe Interface Assembly	749242	
016	1M RAM Expansion Module	799072	C
017	2M RAM Expansion Module	799106	C
018	256K Non-Volatile Memory (NVRAM)	804017	-
019	512K Non-Volatile Memory (NVRAM)	804062	-
020	1M Non-Volatile Memory (NVRAM)	809264	C
440	1722A-440 Winchester Hard Disk, 40M-Byte	862412	(all)
V7800	Multifunction Board	882303	
V7800-002	Analog Output Expansion (12 Ch.)	882311	
V7800-004	Digital Output Expansion	882316	
V7800-040	Analog Input Multiplexer Master	882357	
V7800-040	W Wide Slot Analog Input Multiplexer Master	882410	

NOTE: 17XXA-004 and 17XXA-005 Magnetic Bubble Memory, top Fluke P/N is for high profile unit, bottom Fluke P/N is for low profile unit. High profile unit occupies two slots. High and low profile units are electrically equivalent.

Table 4-1. Replacement Modules, Cables, and Connectors

DESCRIPTION	FLUKE PART NUMBER	
	1722A	1752A
STANDARD MODULES		
Power-Up Assembly (PUP)	704353	Same
Power Supply	718064	Same
Floppy Disk Drive	825356	Same
Single-Board Computer (SBC)	804146	Same
Video/Graphics/Keyboard Interface (VGK)	661587	Same
CRT and Video Electronics	884697	Same
Touch-Sensitive Overlay	705301	Same
Keyboard	718106	Same
Analog Measurement Processor (1752A-010)	750620	736876
OPTIONAL MODULES		
Parallel Interface (Option -002)	717397	Same
256K byte Bubble Memory (Option -004)	657346 or 777235*	Same
512K byte Bubble Memory (Option -005)	657353 or 777391*	Same
256K byte RAM Expansion (Option -006)	718684	Same
512K byte RAM Expansion (Option -007)	718692	Same
IEEE-488/RS-232C Interface (Option -008)	718221	Same
Dual Serial Interface (Option -009)	718734	Same
Analog Output (Option 1752A-011)		610329
Counter/Totalizer (Option 1752A-012)		630186
Mainframe Interface Assembly (Option 1752A-013)		750612
MISCELLANEOUS		
PIB Loopback Cable	632968	Same
RS-232 Loopback Connector	732107	Same
RS-232 Null Modem Cable	518696	Y1705
IEEE-488 Cable (2 meter)	682401	682401
I/O Extender Cable (9 meter)		532887
Extender Chassis (1702A)		750711
Power Cord	284174	Same
Solar Cell Board		765206
3A Fuse (115V operation)	109280	Same
2A Fuse (230V operation)	109181	Same
Disk Drive Shipping Insert	707984	Same
System Disk	718072	759167
System Diagnostic Disk	718080	759175
Service Manual	732156	Same
OEM Manual	919969	Same
* Note: Please order replacement modules from the part number listed on the module itself.		

Table 4-2. Replacement PROMs and PALs

ASSEMBLY	REV	DESCRIPTION	REF DES	VER	JF/PN
Single Board Computer	All (1722A)	EPROM boot set	U68, U81	1.7	712810
	All (1752A)	EPROM boot set	U68, U81	1.7	712810
	All	Boot Prom Set	U68, U81	2.1	805143
	All	PAL, AGGIE bus	U20	1.0	712711
	All	PAL, AGGIE state	U22	1.0	712729
	All	PAL, DRAM	U33	1.0	712737
	All	PAL, exception	U18	1.0	712745
	D-F	PAL, floppy	U14	1.0	712752
	G-H		U14	1.1	736975
	All	PAL, postmap	U50	1.0	712760
	All	PAL, premap	U34	1.0	712778
	D	PAL, ras	U66	1.0	712786
	E-F		U66	1.1	718825
	G-H		U66	1.2	737031
	All	PAL, register control	U29	1.0	712794
	D-F	PAL, waitgen	U31	1.0	712802
	G-H		U31	1.1	736983
Video/Graphics/Keyboard (VGK)	All	EPROM, character	U32	1.1	712703
	D,D-2,E				
	D-3,E-1,F	EPROM, firmware	U29	1.4	762633
	All	PAL, argus	U11	1.0	712646
	All	PAL, Address	U18	1.0	712653
	All	PAL, double size	U40	1.0	712661
	All	PAL, clock	U22	1.0	712679
	All	PAL, attribute	U54	1.1	712687
Keyboard	All	CPU, keyboard	U3	1.1	718171
Parallel Interface	All	PROM, par interface	U18,U22	1.6	613216
256K and 512K Memory Expansion Modules	All	PAL, translation	U86	1.0	716480
	All	PAL, status decode	U92	1.0	716498
	All	PAL, error	U75	1.0	716506
	All	PAL, refresh control	U82	1.0	716514
IEEE-488/	All	PAL, address	U3	1.0	711622
RS-232-C	All	PAL, logic	U4	1.0	711630
Dual Serial Interface	All	EPROM, DSI Firmware	U4	1.1	749416
Analog Measurement Processor	All	EPROM, firmware	U1	1.1	776260

Table 4-3. 1722A/1752A Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	VIDEO/GRAPHICS/KEYBOARD (VGK) IF PCA		89536		1	1
A 2	MOTHERBOARD PCA	699066	89536	699066	1	
A 3	POWER-UP (PUP) PCA	704353	89536	704353	1	
A 4	SINGLE BOARD COMPUTER (SBC) PCA		89536		1	2
A 5	FRONT PANEL PCA	704296	89536	704296	1	
A 6	PROGRAMMER'S KEYBOARD ASSEMBLY	644153	89536	644153	1	15
A 7	TOUCH PANEL ASSEMBLY	705301	89536	705301	1	3
A 8	VIDEO MON., 5X9IN., MONOCHROME, KIT	884697	89536	884697	1	4
A 9	DISK DRIVE, FLOPPY, 5.25IN., HALF HEIGHT	825356	89536	825356	1	4
A 10	PWR SUP, 200W, 5V@30A, -12V@4A, +12V@8/4A	718064	89536	718064	1	4
A 12	SOLAR CELL PCA	765206	89536	765206	1	5
A 13	ANALOG MEASUREMENT PROCESSOR PCA	736876	89536	736876	1	5, 6, 7
A 14	KEYBOARD FILTER PCA	849252	89536	849252	1	
B 1	FAN, 12VDC, 34CFM, 3.15" SQ	776278	89536	776278	1	
E 1	TERM, FASTON, REC., .187, 18-22 AWG, INSUL	747485	06383	DNF18-187	1	
E 2	BINDING POST, METAL, PLATED	225623	89536	225623	1	
E 3	BINDING POST HEAD, PLATED	225615	89536	225615	1	
E 4	TERM, RING 1/4 & 1/32, SOLDER	102566	79963	813	1	
F 1	FUSE, .25X1.25, 3A, 250V, FAST	109199		AGC-3	1	
FL 1	FILTER, LINE, 115VAC/3A, 250VAC/2A	715128	05245	3EQ8	1	
H 1	AIR FILTER	605899	25099	605899	1	
H 2	WASHER, FLAT, SS, .125, .317, .030	146225		COMMERCIAL	3	
H 3	WASHER, LOCK, SPLIT, STL, .115, .223, .025	110395		COMMERCIAL	2	
H 4	WASHER, LOCK, SPLIT, STL, .168, .307, .040	111070		COMMERCIAL	4	
H 5	WASHER, FLAT, STL, .149, .375, .031	110270		COMMERCIAL	9	
H 6	SCREW, PH, P, SEMS, STL, 6-32, .313	530287		COMMERCIAL	6	
H 7	SCREW, PH, P, LOCK, STL, 4-40, .375	152124	73734	19024	2	
H 8	SCREW, PH, P, LOCK, SS, 6-32, .250	320093	74594	320093	28	
H 9	SCREW, PH, P, SEMS, STL, 6-32, .250	178533		COMMERCIAL	11	
H 10	SCREW, PH, P, SEMS, STL, 6-32, .375	177022		COMMERCIAL	8	
H 11	SCREW, PH, P, SEMS, STL, 6-32, .500	177030		COMMERCIAL	9	
H 12	SCREW, CAP, SCKT, SS, 8-32, .375	295105	74445	295105	4	
H 13	SCREW, PH, P, LOCK, STL, 8-32, .375	114116	89536	114116	10	
H 14	SCREW, PH, P, SEMS, STL, 8-32, .375	436030		COMMERCIAL	4	
H 15	SCREW, PH, P, THD CUT, SS, 4-24, .375	183574		COMMERCIAL	5	
H 16	NUT, HEX, BR, 1/4-28	110619		COMMERCIAL	2	
H 17	SCREW, PH, P, STL, M3X6	854034		COMMERCIAL	6	
H 19	WASHER, FLAT, BRASS, #6, 0.028 THK	111310		COMMERCIAL	4	
H 20	SCREW, PH, P, SEMS, STL, 6-32, .750	309963		COMMERCIAL	4	
H 21	SCREW, PH, P, LOCK, STL, 8-32, .250	228890	73734	19062	4	
H 22	SCREW, PH, P, LOCK, SS, 4-40, .312	335141	74594	335141	3	
J 1	SOCKET, 1 ROW, 0.100 CTR, 2 POS	602706	00779	640442-2	1	
MP 1	RIGHT SIDE CHASSIS	749374	89536	749374	1	
MP 2	LEFT SIDE CHASSIS	749382	89536	749382	1	
MP 3	BRACKET, POWER SUPPLY	749275	89536	749275	1	
MP 4	COVER, POWER SUPPLY	749366	89536	749366	1	
MP 5	PLATE, REMOTE OPTION	762559	89536	762559	1	
MP 6	COVER CRT ELECTRONICS	884692	89536	884692	1	
MP 7	FLOPPY SUPPORT	759118	89536	759118	1	
MP 8	CARD CAGE	749390	89536	749390	1	
MP 9	FLOPPY DIVIDER (B)	749283	89536	749283	1	
MP 10	REAR PANEL	749341	89536	749341	1	
MP 11	CORNER, FRONT, MED PEWTER	630723	89536	630723	2	
MP 12	CORNER, REAR	630764	89536	630764	2	
MP 13	BRACKET, FAN	760470	89536	760470	1	
MP 14	COVER, FILLER PANEL	897538	89536	897538	1	
MP 16	PLAS PART, BOLE PLUG, NYL, DOME, BLK, .250	854299	28520	2603	1	
MP 17	CRT ALIGNMENT INSERT	711325	89536	711325	4	
MP 18	DECAL, FRONT PANEL	849195	89536	849195	1	
MP 20	HLDR, FUSE, 1/4 X 1-1/4, LOPROFILE, PNLMT	424416	61935	FEC031.1631/FEK031.1613	1	
MP 21	BEZEL, HALF HEIGHT, PAINTED DK UMBER	824847	89536	824847	1	
MP 22	TOUCH PANEL FRONT GASKET	604272	2K262	604272	1	
MP 23	CARD GUIDE	749358	89536	749358	6	
MP 24	CABLE ACCESS, TIE, 4.00L, .10W, .75 DIA	172080	06383	SST-1M	6	
MP 25	CABLE TIE ANCHOR, ADBSV, .160TIE	407908	06383	ABMM-A-C	2	
MP 26	DECAL, IMPLOSION PROTECTION	577387	89536	577387	2	
MP 27	FOOT, RUBBER, ADHES, BLK, .50 DIA, .14 THK	513820		SJ-5012	2	
MP 28	LABEL, ADHESIVE, IC, HIGH TEMPERATURE	720904	85480	DAT-1-637-10	25	
MP 29	COVER, REAR CARD CAGE		89536		1	9
MP 30	PLATE, BLANK		89536		1	10
MP 31	COVER, TOP	754663	89536	754663	1	
MP 32	COVER, BOTTOM	754671	89536	754671	1	
MP 33	SIDE EXTRUSION	859947	89536	859947	2	

List of Replaceable Parts
PARTS LISTS

Table 4-3. 1722A/1752A Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 34	INSERT EXTRUSION	859942	89536	859942	2	
MP 35	† BAIL, INSTRUMENT	707877	95080	707877	2	
MP 36	FOOT, SINGLE BAIL TYPE (DARK UMBER)	653923	89536	653923	4	
MP 37	DECAL, TITLE		89536		1	11
MP 38	DECAL, FRONT CORNER 5 1/4, MED PEWTER	685289	22670	685289	2	
MP 39	DECAL, REAR CORNER 5 1/4, MED PEWTER	685297	22670	685297	2	
MP 40	DECAL, TRIM	707810	22670	707810	2	
MP 41	GROUND STRIP, BECU, SPRING FINGER	370619	34641	97-500-02	9	
MP 42	SHIPPING DISKETTE	707984	89536	707984	1	
MP 43	† DISK SET		89536		1	12
MP 44	TLC FLOPPY DISK POCKET	650473	89536	650473	3	
MP 45	MAGNET, FERRITE, 4 GAUSS	876032	0CXF1	130102-004	2	
MP 46	DECAL, FLUKE-PHILIPS, WHITE, SMALL	835280	22670	835280	1	
MP 47	DECAL CSA	525527	22670	525527	1	
MP 48	FOAM, BOARD RETENTION	897525	89536	897525	2	
MP 49	PROTECTIVE COVER	787283	89536	787283	1	5
MP 50	DECAL, REAR PANEL	759142	89536	759142	1	5
MP 51	PLATE, BOTTOM	787325	89536	787325	1	5
MP 52	PLATE FILLER (LARGE)	754697	89536	754697	1	5
MP 68	DECAL, FUSE RATING	922570	89536	922570	1	
MP 69	SHIELD, NPS 200 POWER SUPPLY	521187	89536	521187	1	
P 1	MOUNTING STRAP, CRT (WIRE)	650630	89536	650630	1	
S 1	SWITCH, ROCKER, DPST	615054	55224	JWZ2120-0301	1	
TM 1	FORM 1720A PROGRAM WORKSHEET	533547	89536	533547	1	
TM 2	SYSTEM MANUAL		89536		1	13
TM 3	BASIC PROGRAMMING MANUAL	718809	89536	718809	1	
TM 4	BASIC REFERENCE MANUAL	718817	89536	718817	1	
TM 5	GETTING STARTED MANUAL		89536		1	14
TM 6	DATA ACQUISITION AND CONTROL MANUAL	776245	89536	776245	1	5
W 1	SUPPORT BRACKET CRT MTG (WIRE)	650515	89536	650515	1	
W 2	CABLE, POWER	644120	89536	644120	1	
W 3	CABLE, POWER SUPPLY	705343	89536	705343	1	
W 4	CABLE, VIDEO POWER SIGNAL	712836	89536	712836	1	
W 5	CABLE, CRT GROUND	843201	89536	843201	1	
W 6	CABLE, FUSE	762500	89536	762500	1	
W 7	CABLE, CHASSIS GROUND	762518	89536	762518	1	
W 8	CABLE, BLACK POWER SWITCH	762542	89536	762542	1	
W 9	CABLE, WHITE POWER SWITCH	762526	89536	762526	1	
W 10	CORD, LINE, 5-15/IEC, 3-18AWG, SVT, 7.5 FT	284174	70903	17239	1	
NOTES:	† Static sensitive part. 1. FOR 1722A/1752A ORDER FLUKE STOCK NUMBER 661587 OR 897483. FOR 1722A/AP ORDER FLUKE STOCK NUMBER 744284 OR 897488. REFER TO A1 NOTE 1. 2. FOR 1722A/1752A V1.7 ORDER FLUKE STOCK NUMBER 705285. FOR 1722A/1752A V2. X ORDER FLUKE STOCK NUMBER 804146. FOR 1711A/AA V1. 7 ORDER FLUKE STOCK NUMBER 805002. FOR 1711A/AA V2. X ORDER FLUKE STOCK NUMBER 804997. FOR 1722A/AP ORDER FLUKE STOCK NUMBER 744318. 3. NO PARTS BREAKDOWN FOR THIS ASSEMBLY. 4. SEE SECTION 9. 5. USED ON 1752A ONLY. 6. SEE OPTION -010 FOR PARTS BREAKDOWN. 7. NOT INCLUDED WITH 1752A-1. 8. FOR 1722A QTY = 19. FOR 1752A QTY = 21. 9. FOR 1722A WITH VIDEO OUTPUT JACK ORDER FLUKE STOCK NUMBER 704429 FOR 1722A WITHOUT VIDEO OUTPUT JACK ORDER FLUKE STOCK NUMBER 897512. FOR 1752A ORDER FLUKE STOCK NUMBER 754770. FOR 1752A WITH OPTION V7800 ORDER FLUKE STOCK NUMBER 884742. 10. FOR 1722A ORDER FLUKE STOCK NUMBER 777250 QTY = 3. FOR 1752A ORDER FLUKE STOCK NUMBER 787317 QTY = 1. 11. FOR 1722A ORDER FLUKE STOCK NUMBER 707208. FOR 1752A ORDER FLUKE STOCK NUMBER 759134. 12. FOR 1722A ORDER FLUKE STOCK NUMBER 897496. FOR 1752A ORDER FLUKE STOCK NUMBER 897509. 13. FOR 1722A ORDER FLUKE STOCK NUMBER 718791. FOR 1752A ORDER FLUKE STOCK NUMBER 767624. 14. FOR 1722A ORDER FLUKE STOCK NUMBER 716613. FOR 1752A ORDER FLUKE STOCK NUMBER 760561. 15. OMITTED ON FLUKE MODEL 1722A-1.					

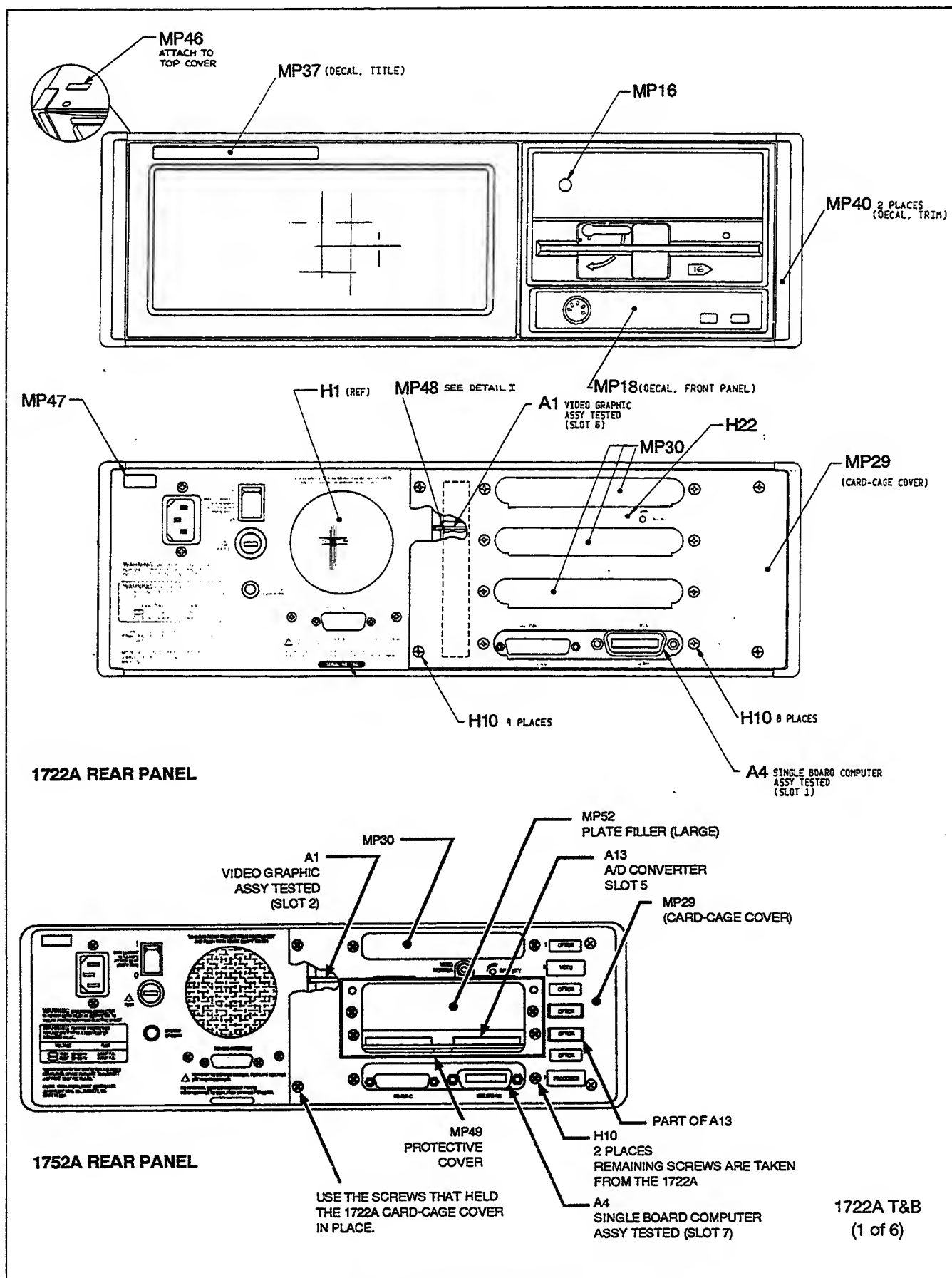
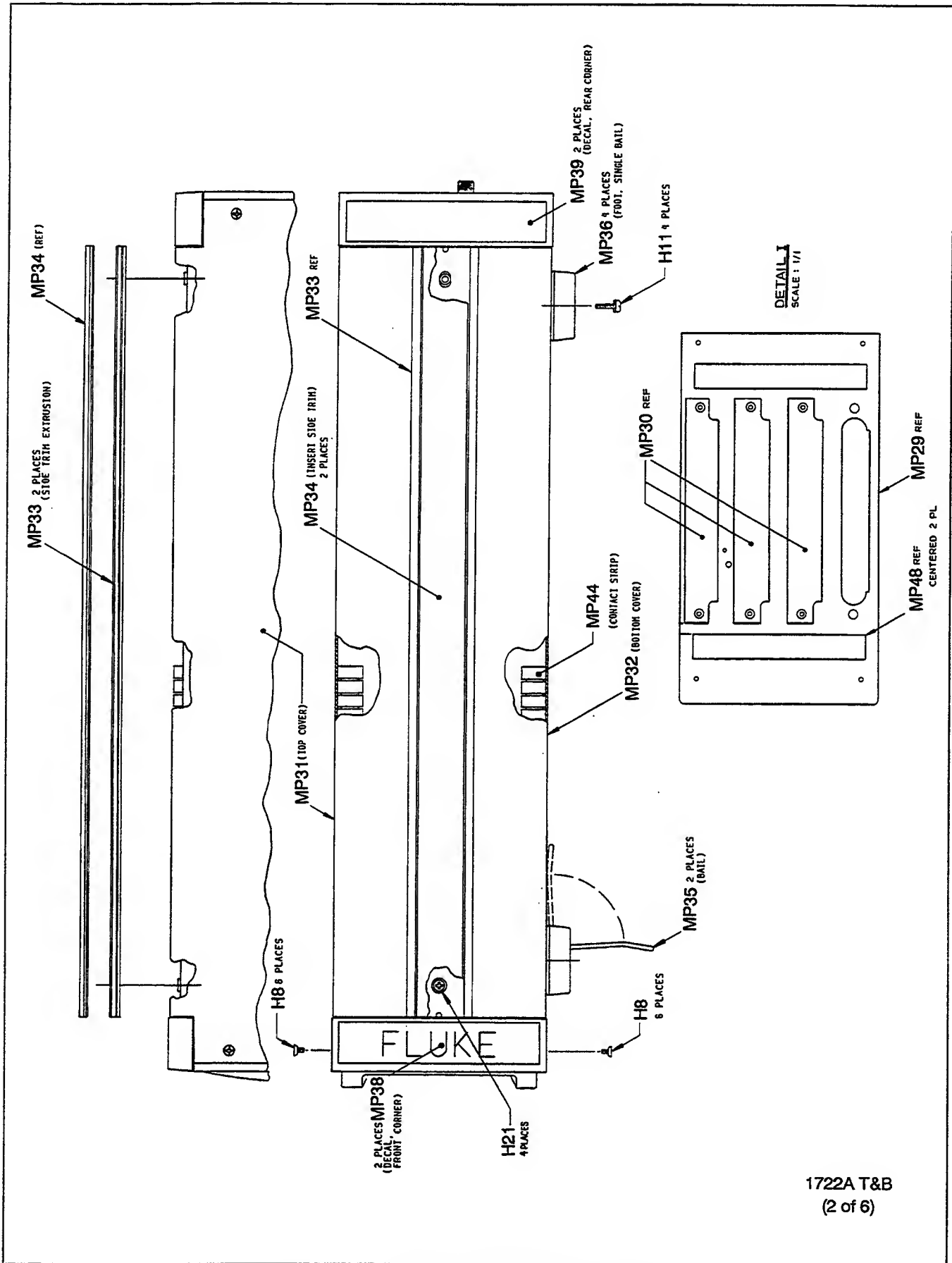
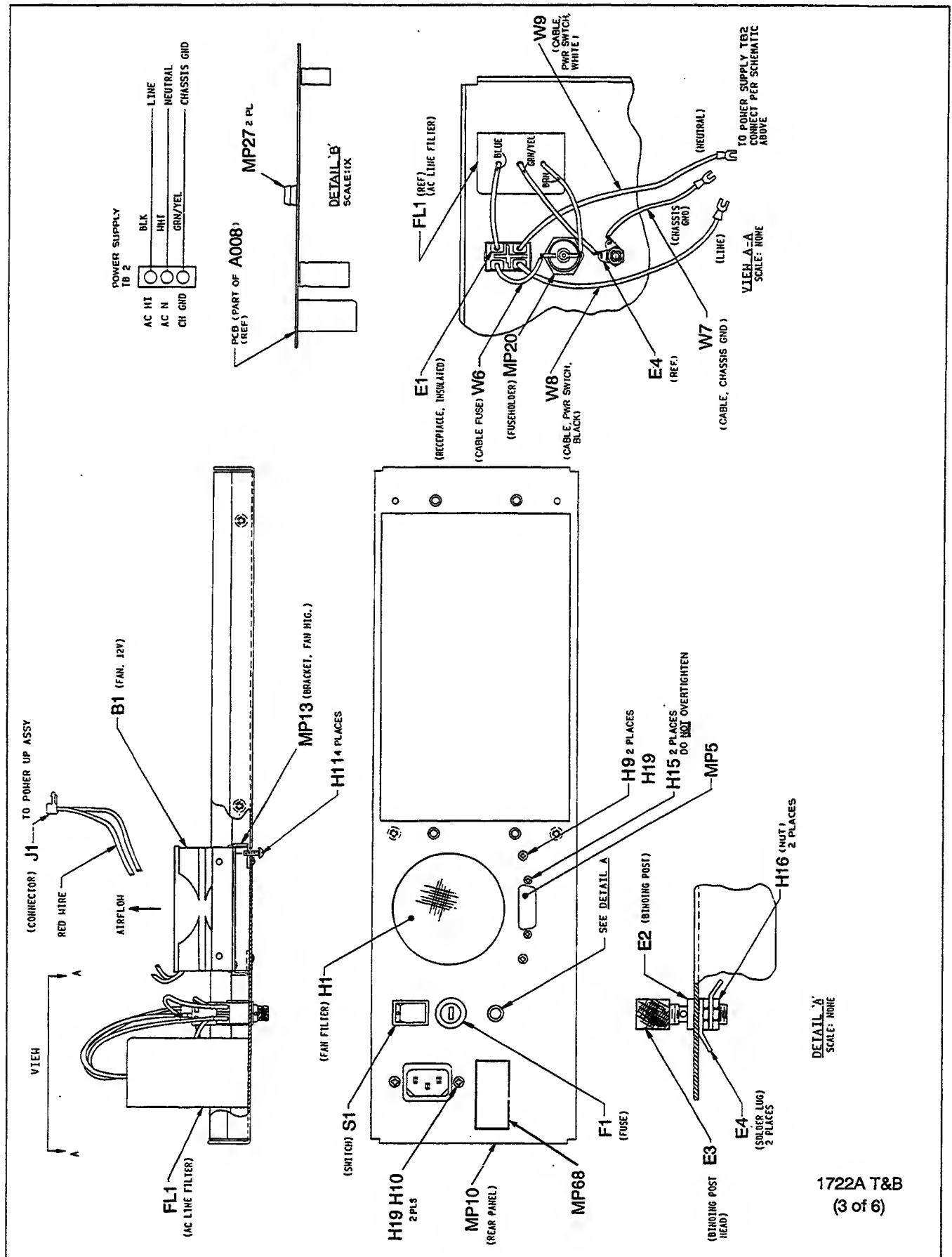
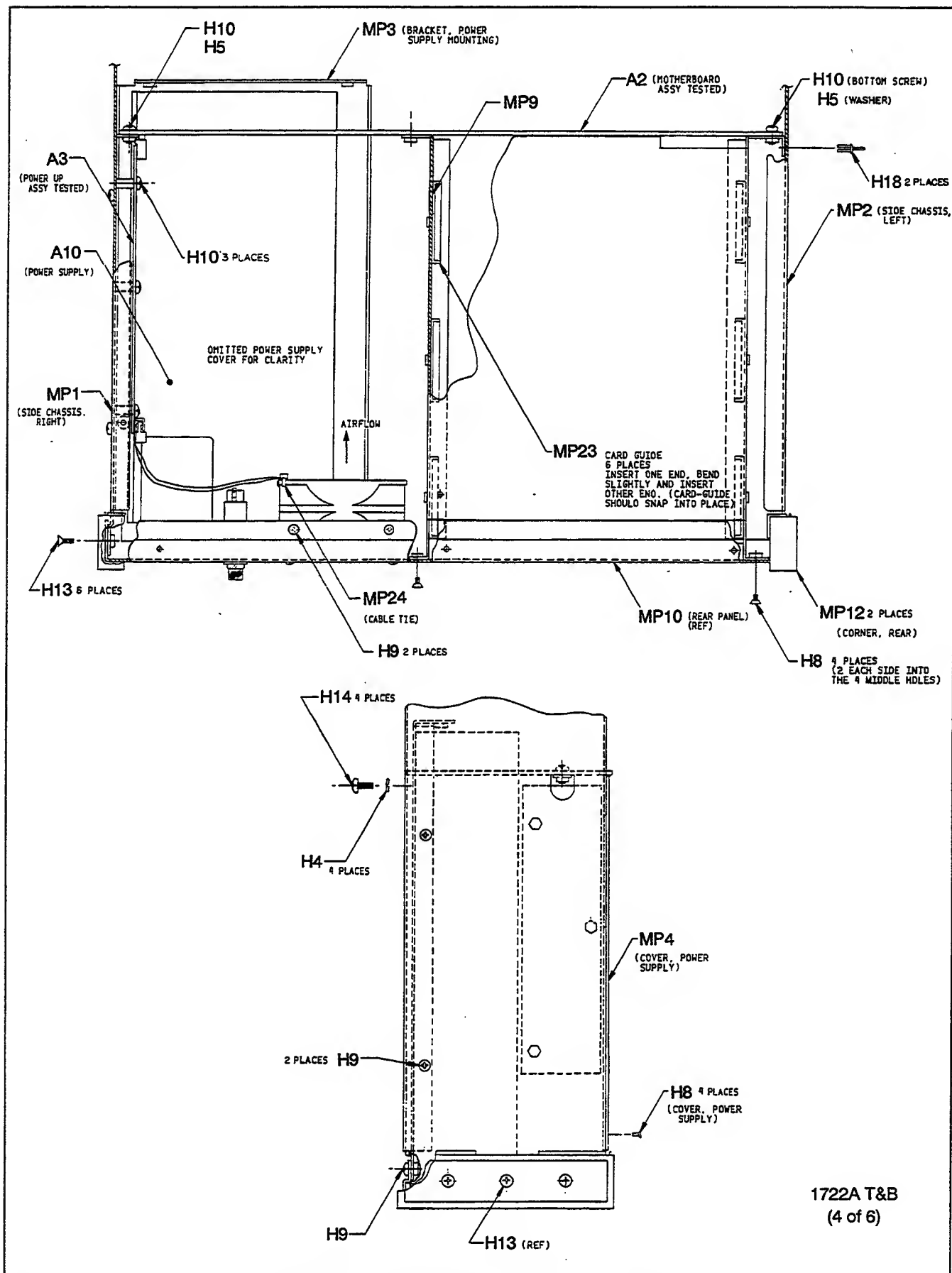


Figure 4-1. 1722A/1752A Final Assembly



1722A T&B
(2 of 6)





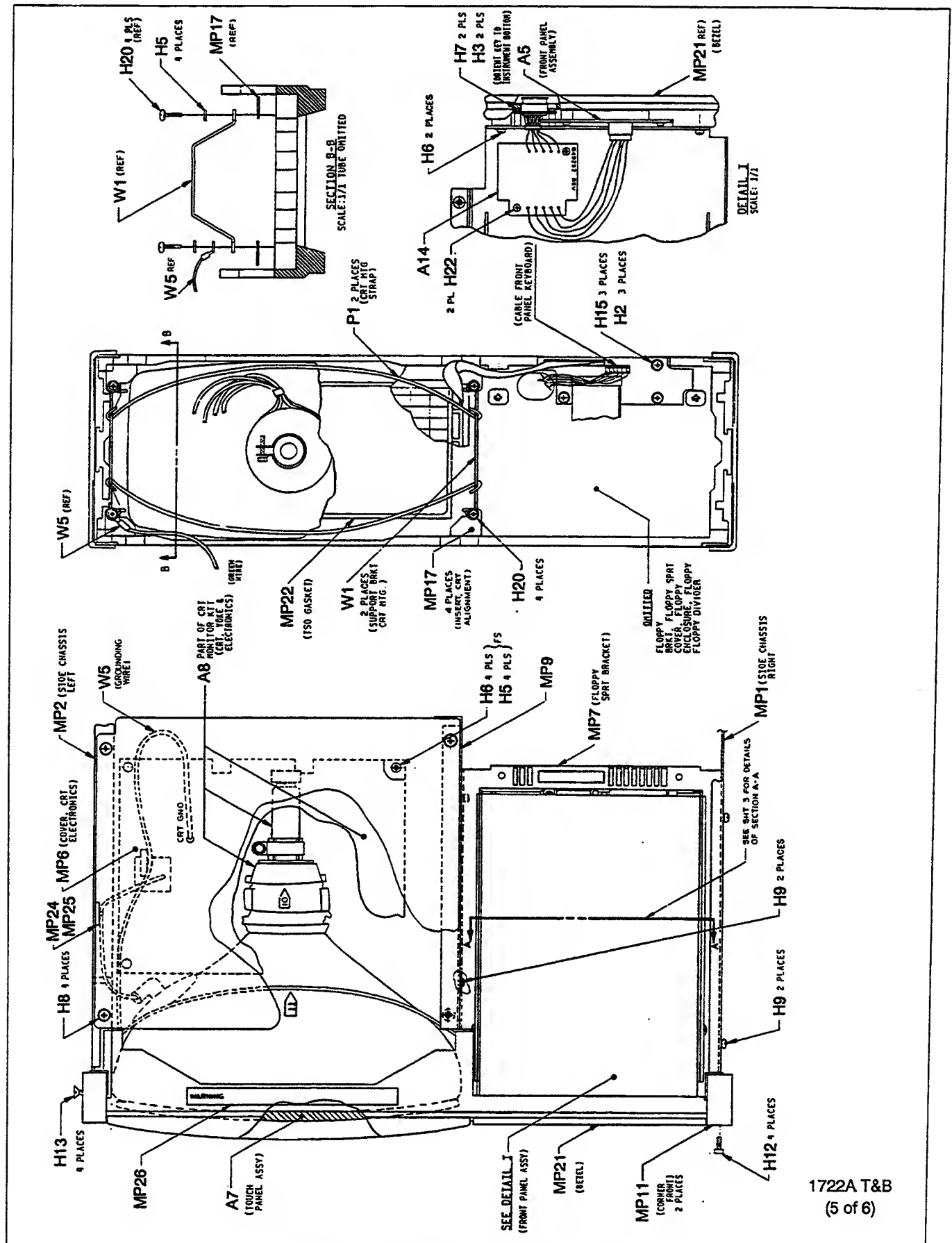


Figure 4-1. 1722A/1752A Final Assembly (cont)

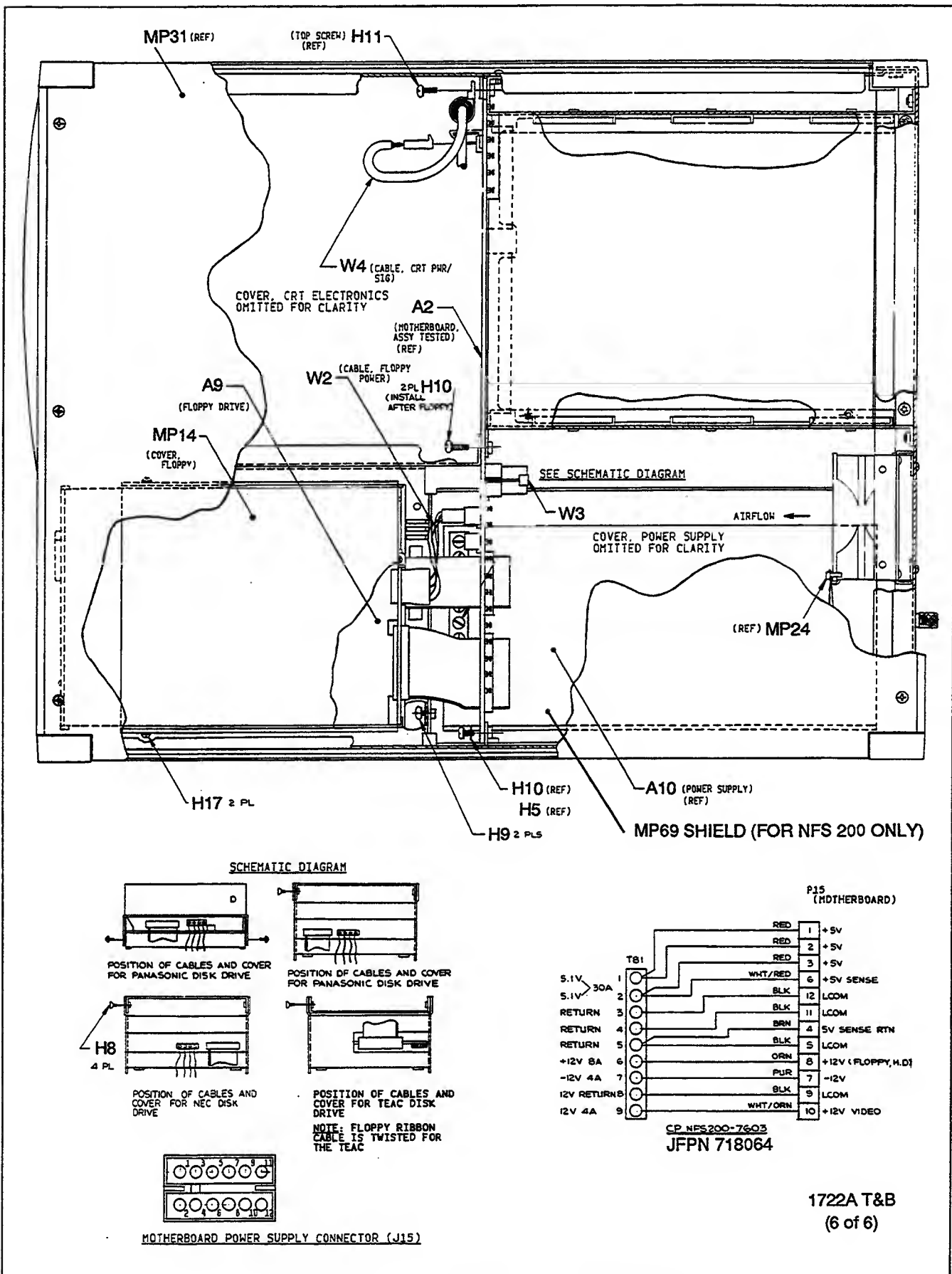


Table 4-4. A1 Video/Graphics/Keyboard (VGK) Interface PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 2, 3, 10- C 13, 15, 19, C 22, 25, 27- C 34, 36, 38, C 40, 42, 46, C 54, 58- 65, C 89, 98,100 C 4 C 5 C 120,121,122 FL 1 H 1 J 1 J 2 JFR 1 MP 1 MP 2 MP 3 MP 4 Q 1 Q 2 R 1, 8, 9 R 2 R 3 R 4 R 5 R 6 R 7, 13, 15 R 10 R 11, 12, 14 U 1, 7, 49 U 2, 89 U 3, 55, 72, U 87, 92, 96 U 4, 9, 14, U 17, 50 U 5 U 6 U 8 U 10, 36, 46 U 11, 18 U 12, 13, 19, U 38, 98 U 15 U 16, 20 U 21, 39, 44 U 22 U 23, 75 U 24, 25, 27, U 42 U 26, 66, 81 U 28, 33, 34 U 29 U 30 U 31 U 32 U 35 U 37 U 40 U 41 U 43, 68 U 45 U 47 U 48, 77, 78 U 51 U 52, 83- 85, U 91, 93, 99 U 53, 67, 80, U 82 U 54 U 57 U 58- 65 U 69, 74, 79, U 94, 97 U 71	CAP,POLYES,0.1UF,+10%,50V CAP,MICA,100PF,+5%,500V CAP,CER,1000PF,+10%,500V,XSS CAP,AL,47UF,+20%,10V,SOLV PROOF FILTER,EMI,12VDC,7A,HV SURGES SCREW,PH,P,LOCK,SS,4-40,.187 JACK,PWB,RT ANG HEADER,1 ROW,.100CTR,8 PIN HEADER,2 ROW,.100CTR,50 PIN GROUNDING SPRING EJECTOR,PWB,NYLON POST,CHASSIS GROUND SHIELD, VIDEO CONNECTOR REPLACEMENT TRANSISTOR,SI,NPN,SM SIG,GEN PURPOSE TRANSISTOR,SI,NPN,SMALL SIGNAL RES,CF,330,+5%,0.25W RES,CF,200,+5%,0.25W RES,CF,130,+5%,0.25W RES,CF,150,+5%,0.25W RES,CF,68,+5%,0.25W RES,VAR,CERM,200,+10%,0.5W RES,CF,10K,+5%,0.25W RES,CF,1.5,+5%,0.25W RES,CF,220,+5%,0.25W IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR IC,LSTTL,OCTL INV LINE DRVR W/3-STATE IC,LSTTL,HEX D F/F,+EDG TRG,W/CLEAR IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR IC,LSTTL,BCD-DEC DCDR/DRVR 15V OUT IC,CMOS,HEX BUFFER W/3-STATE OUTPUT OSCILLATOR,25.54MHZ,TTL CLOCK IC,NMOS,ASYN COMMUNICATION CONTROLLR IC,16L8A PROG LOGIC ARRAY IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT IC,LSTTL,2-4 LINE DEMUX IC,LSTTL,QUAD 2-1 LINE MUX W/STROBE IC,16R8 PROG LOGIC ARRAY IC,LSTTL,8BIT SER/PAR-IN,SER-OUT SHFT IC,LSTTL,OCTAL D TRANSPARENT LATCHES IC,LSTTL,OCTAL D F/F,+EDG TRG IC, 2K X 8 STAT RAM IC,16K X 8 EPROM IC,NMOS,16 BIT MICROCOMPUTER,SELECTED IC,NMOS,CRT CONTROLLER IC, 4K X 8 EPROM IC,LSTTL,HEX INVERTER IC,LSTTL,HEX BUFFER W/NOR ENABLE IC,16R6 PROG LOGIC ARRAY IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR IC,LSTTL,4BIT D REGISTER W/3-STATE IC,TTL,QUAD 2 INPUT AND GATE IC,LSTTL,DUAL 4 INPUT NAND GATE IC,LSTTL,3-8 LINE DCDR W/ENABLE IC,LSTTL,QUAD 2 INPUT NAND GATE IC,LSTTL,SYNC DIV BY 16 UP/DOWN CNTR IC,LSTTL,SYNC DIV BY 16 BINARY COUNTER IC,16R4A PROG LOGIC ARRAY IC,LSTTL,DUAL J-K F/F,+EDG TRIG IC,64K X 1 DYN RAM,256/4MS REFRESH IC,LSTTL,DUAL 4-1 LINE SELECT/MUX IC,LSTTL,QUAD 2 INPUT OR GATE	696484 696484 696484 696484 696484 696484 148494 357806 602334 807545 149567 500819 474213 732875 731125 706879 826487 880042 364232 218081 368720 441451 442301 343442 414532 721811 348839 442020 342626 454892 429480 393207 393207 393124 393124 419192 407759 659870 483552 712646 429035 429035 477406 393165 404194 712679 495671 504514 504514 473223 584144 89536 697680 698217 393058 483800 712661 393215 504480 393066 393280 407585 393033 698480 698480 495598 495598 712687 412999 721944 393181 393181 393108	37942 93790 60705 62643 51406 74594 11503 00779 00779 2M021 30035 89536 89536 04713 04713 59124 59124 59124 59124 59124 80294 59124 59124 59124 01295			

List of Replaceable Parts
PARTS LISTS

Table 4-4. A1 Video/Graphics/Keyboard (VGK) Interface PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
U 73,101	‡ IC,LSTTL,8BIT PAR/SER-IN,SER-OUT SHFT	585539	01295	SN74LS165AN	2	
U 76	‡ IC,LSTTL,8-1 LINE MUX W/STROBE	393173	01295	SN74LS151N	1	
U 86, 88, 95	‡ IC,LSTTL,4 BIT BINARY FULL ADDER	408740	01295	SN74LS283N	3	
U 90	‡ IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	1	
U 100	‡ IC,TTL,DUAL AND DRVR W/OPEN COLLECTOR	393959	01295	SN75451BP	1	
XU 11, 18, 22,	SOCKET,IC,20 PIN	454421	00779	2-640464-1	5	
XU 40, 54	SOCKET,IC,24 PIN	454421				
XU 28, 32- 34	SOCKET,IC,28 PIN	376236	00779	2-640361-1	4	
XU 29	SOCKET,IC,28 PIN	448217	91506	228-AG39D	1	
XU 30, 31	SOCKET,IC,40 PIN	429282	00779	2-640379-1	2	
Z 1	RES,CERM,SIP,10 PIN,9 RES,10K,+/-2%	414003	91637	CSC10A-01-103G	1	
Z 2	RES,CERM,SIP,8 PIN,7 RES,10K,+/-2%	412924	91637	CSC08A-01-103G	1	
Z 3	RES,CERM,SIP,10 PIN,5 RES,10K,+/-2%	529990	91637	CSC10A-03-103G	1	
NOTES:	‡ Static sensitive part. 1. C120,J1,Q1,R3 & R4 USED ON A1 FLUKE NUMBER 661587 AND 744284, AND OMITTED FROM FLUKE 897483 and 897488. REFER TO FINAL ASSEMBLY NOTE 1. 2. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS. 3. FOR 1722A/1752A ORDER FLUKE STOCK NUMBER 712703. FOR 1722A/AP ORDER FLUKE STOCK NUMBER 736967. 4. FOR 1722A/1752A ORDER FLUKE STOCK NUMBER 762633. FOR 1722A/AP ORDER FLUKE STOCK NUMBER 712695.					

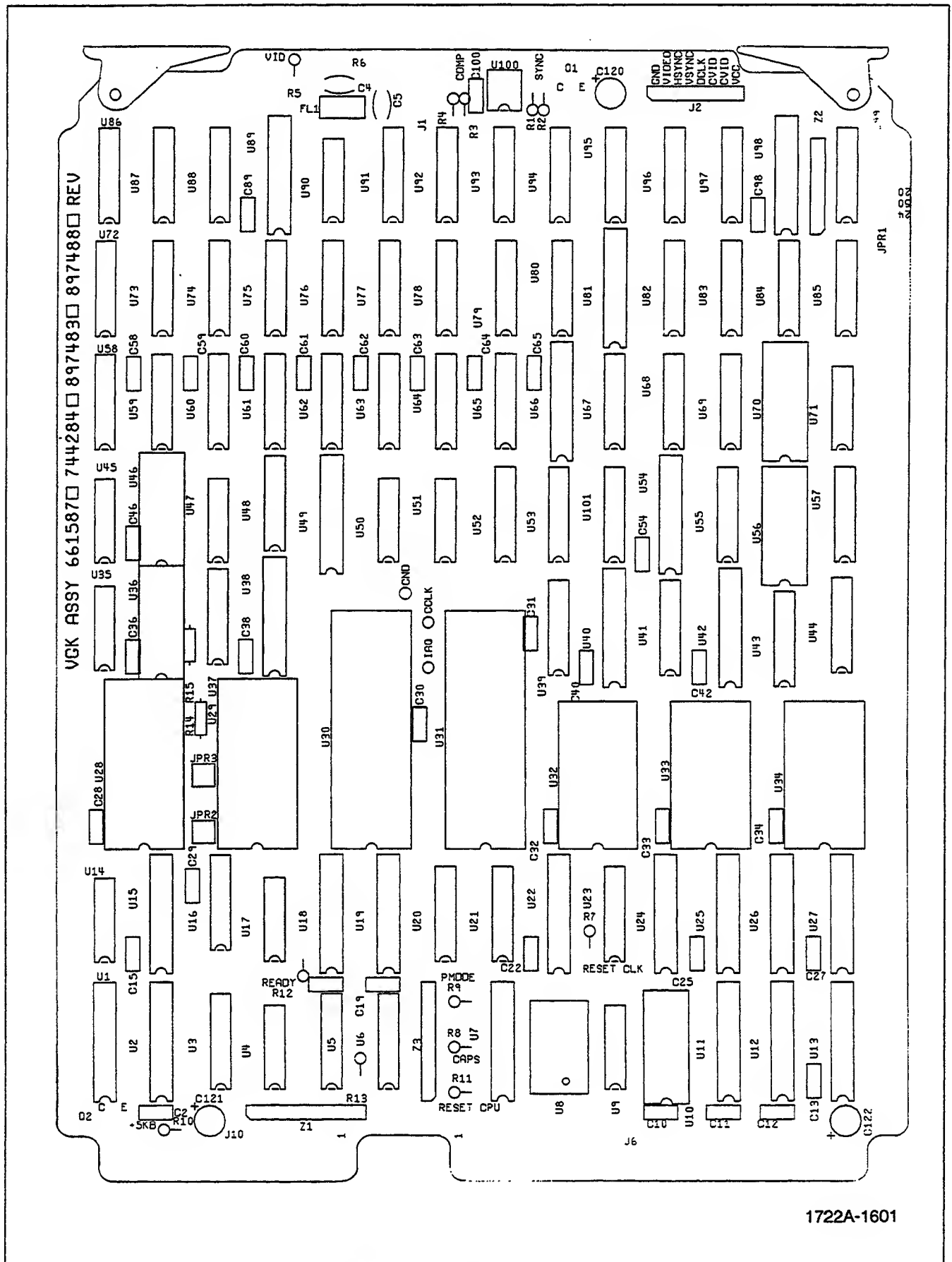
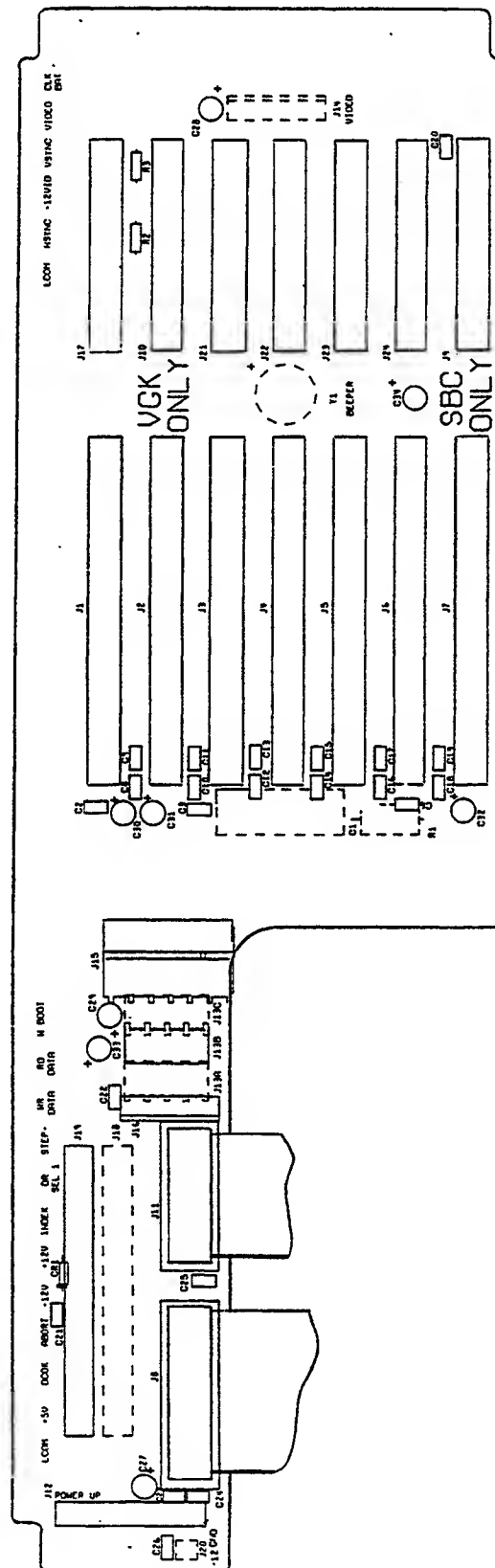


Figure 4-2. A1 Video/Graphics/Keyboard (VGK) Interface PCA

List of Replaceable Parts
PARTS LISTS

Table 4-5. A2 Motherboard PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,POLYST,0.1UF,+/-10%,120V	167460	84411	1263UW104108120V	1	
C 2, 3, 6,	CAP,CER,0.22UF,+/-20%,50V,Z5U	519157	04222	SR205E224MAT	22	
C 8- 26		519157				
C 27- 33	CAP,TA,15UF,+/-20%,20V	519686	56289	199D156X0020DA2	7	
C 34	CAP,TA,1UF,+/-10%,35V	161919	56289	199D105X0035AA2	1	
CR 1	DIODE,SI,100 PIV,1.0 AMP	698555	04713	1N4002	1	
E 1- 17, 20	TERM,UNINSUL,FEEDTHRU,HOLE,TURRET	321364	88245	2010C-5	18	
J 1- 7	CONN,PWB EDGE,REC,.100CTR,72 POS	520155	00779	1-530843-9	7	
J 9, 10, 17,	CONN,PWB EDGE,REC,.100CTR,44 POS	520148	00779	1-530843-5	7	
J 21- 24		520148				
J 12	HEADER,1 ROW,.156CTR,10 PIN	376400	27264	26-60-0100	1	
J 13	CONN,MATE-N-LOK,HEADER,4 PIN	512269	00779	350211-1	1	
J 14	HEADER,1 ROW,.156CTR,6 PIN	380378	00779	640388-6	1	
J 15	CONN,MATE-N-LOK,HEADER,12 PIN	706010	00779	350220-1	1	
J 16	HEADER,1 ROW,.100CTR,9 PIN	631168	00779	640456-9	1	
J 18, 19	HEADER,2 ROW,.100CTR,50 PIN	855122	28213	3596-6003	2	
R 1	RES,CC,1K,+/-10%,1W	109371	01121	GB1021	1	
R 2, 3	RES,CF,390,+/-5%,0.25W	441543	59124	CF1/4 391J	2	
W 1	CABLE, FLOPPY SIGNAL	705434	89536	705434	1	
W 2	CABLE,FRONT PANEL	503011	89536	503011	1	
Y 1	AF TRANSD,SPEAKER,16MM,SEALED	743187	82277	BRT1615P-01	1	
NOTES:	† Static sensitive part.					



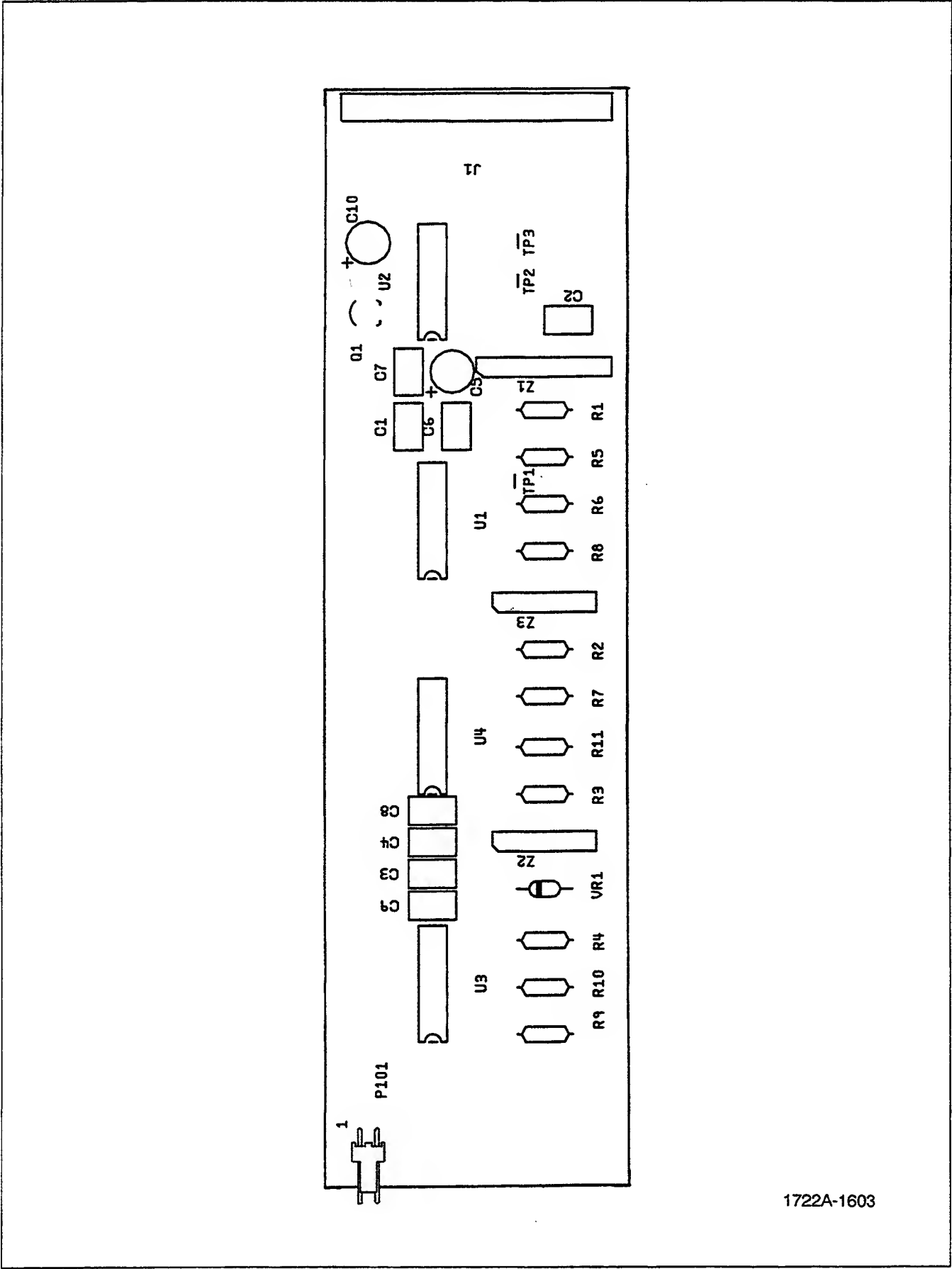
1722A-1602

Figure 4-3. A2 Motherboard PCA

List of Replaceable Parts
PARTS LISTS

Table 4-6. A3 Power-Up (PUP) PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 4, 6- C 9	CAP,POLYES,0.22UF,+10%,50V	696492	37942	168-2-224K50AB	8	
C 5	CAP,AL,47UF,+50-20%,16V	696492				
C 10	CAP,AL,6.8UF,+20%,16V	436006	62643	SM16VB-47	1	
J 1	SOCKET,1 ROW,PWB,0.156C,RT ANG,10 POS	613992	62643	LL16VB685M5X12LLV	1	
P 101	HEADER,1 ROW,.100CTR,RT ANG,2 PIN	376384	27264	09-52-3101	1	
Q 1	TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	830463	95354	1100-11-102-02	1	
R 1	RES,CF,180,+5%,0.25W	218396	04713	2N3904	1	
R 2, 3	RES,MF,30.1K,+1%,0.125W,100PPM	441436	59124	CF1/4 181J	1	
R 4	RES,MF,147,+1%,0.125W,100PPM	168286	91637	CMF-55 3012F T-1	2	
R 5	RES,MF,301,+1%,0.125W,100PPM	288415	91637	CMF-55 1470F T-1	1	
R 6	RES,MF,5.23K,+1%,0.125W,100PPM	267740	91637	CMF-55 3010F T-1	1	
R 7	RES,MF,2K,+1%,0.125W,100PPM	294876	91637	CMF-55 5231F T-1	1	
R 8	RES,MF,26.7K,+1%,0.125W,100PPM	235226	91637	CMF-55 2001F T-1	1	
R 9, 10	RES,MF,10K,+1%,0.125W,100PPM	245779	91637	CMF-55 2672F T-1	1	
R 11	RES,CF,4.7K,+5%,0.25W	168260	91637	CMF-55 1002F T-1	2	
TP 1- 3	TERM,FASTON,TAB,.110,SOLDER	348821	59124	CF1/4 472J	1	
U 1	IC,LSTTL,QUAD 2 INPUT NAND GATE	512889	00779	62395-1	3	
U 2	IC,COMPARATOR,QUAD,14 PIN DIP	393033	01295	SN74LSOON	1	
U 3	IC,LSTTL,QUAD 2 IN NAND W/SCHMT TRIG	387233	04713	LM339N	1	
U 4	IC,LSTTL,QUAD 2 IN NOR GATE W/OPN COL	504449	01295	SN74LS132N	1	
VR 1	ZENER,UNCOMP,6.2V,2%,20.0MA,0.4W	414037	01295	SN74LS33N	1	
Z 1	RES,CERM,SIP,8 PIN,4 RES,1K,+2%	325803	04713	1N753C	1	
Z 2	RES,CERM,SIP,6 PIN,5 RES,4.7K,+2%	714345	91637	CSC08A-03-102G	1	
Z 3	RES,CERM,SIP,6 PIN,5 RES,1K,+2%	494690	91637	CSC06A-01-472G	1	
		408310	91637	CSC06A-01-102G	1	
NOTES:	f Static sensitive part.					



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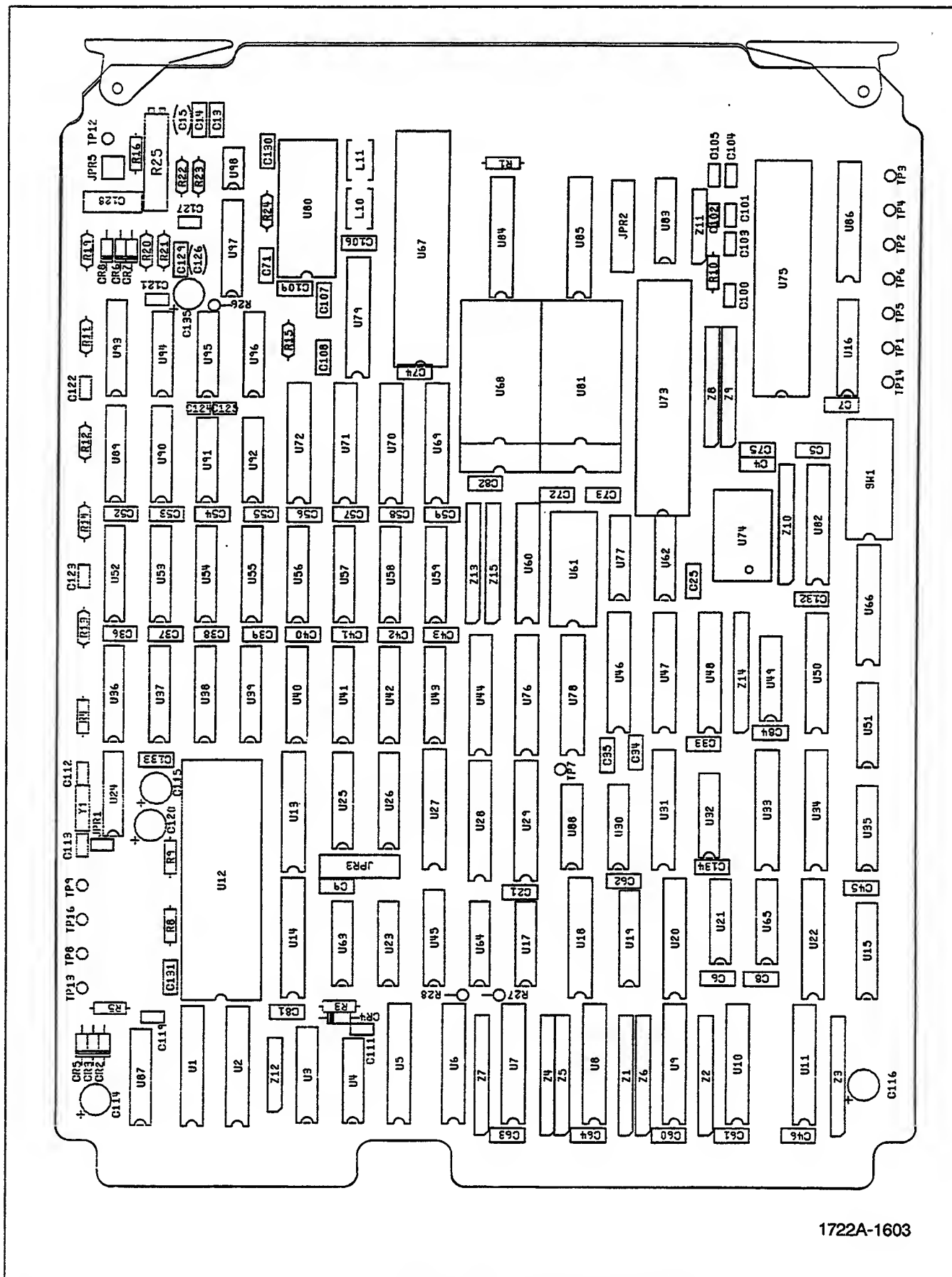
Figure 4-4. A3 Power-up (PUP) PCA

Table 4-7. A4 Single-Board Computer (SBC) PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
BT 1	BATTERY,LITHIUM,3.7V,0.85AH	658476	68630	15-51-01-410-000	1	
C 13, 21, 25,	CAP,POLYES,0.1UF,+10%,50V	696484	37942	168-2-104K50AB	47	
C 33- 43, 45,		696484				
C 46, 52- 64,		696484				
C 71- 75, 81,		696484				
C 82, 84,106-		696484				
C 109,130-134,		696484				
C 409		696484				
C 14	CAP,MICA,100PF,+5%,500V	148494	93790	CD15FD101J03	1	
C 15	CAP,CER,1000PF,+10%,500V,X5S	357806	60705	562CX5FBA102EF102K	1	
C 100-105	CAP,CER,330PF,+5%,100V,C0G	528620	04222	SR201A331JAT	6	
C 111	CAP,CER,0.22UF,+20%,50V,Z5U	519157	04222	SR205E224MAT	1	
C 112	CAP,CER,39PF,+2%,100V,C0G	512962	04222	SR151A390GAT	1	
C 113	CAP,CER,10PF,+2%,100V,C0G	512343	51406	RPE110A100G1	1	
C 114-116	CAP,AL,47UF,+20%,10V,SOLV PROOF	602334	62643	SRAC10VB47RM6X7C3	3	
C 119	CAP,CER,100PF,+2%,100V,C0G	512848	04222	SR151A101GAA	1	
C 120,135	CAP,AL,100UF,+20%,6.3V,SOLV PROOF	615906	62643	SRAC6VB101M6X7C3	2	
C 121-123,125	CAP,CER,120PF,+2%,100V,C0G	543819	04222	SR151A121JAT	4	
C 124	CAP,CER,220PF,+5%,100V,C0G	512111	04222	SR151A221JAA	1	
C 126	CAP,MICA,360PF,+1%,500V	170407	93790	CD15FD361F03	1	
C 127	CAP,CER,1000PF,+20%,100V,X7R	402966	04222	SR151C102MAA	1	
C 128	CAP,POLYES,0.01UF,+10%,250V	325548	68919	MKS4-103-K-250V	1	
C 129	CAP,POLYES,0.22UF,+10%,50V	696492	37942	168-2-224K50AB	1	
CR 2, 4	DIODE,SI,BV=75V,IO=150MA,500MW	203323	09214	IN4448	2	
CR 3	ZENER,UNCOMP,5.6V,5%,20.0MA,0.4W	277236	04713	1N752A	1	
CR 5	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNAL	523738	28480	5082-2835	1	
CR 6- 8	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNAL	313247	28480	5082-6264 T25	3	
H 2	WASHER,FLAT,BRASS,#4,0.025	110775		COMMERCIAL	2	
H 3	WASHER,FLAT,ALUM,0.125X0.250X0.062	381749		COMMERCIAL	2	
H 4	CONN ACC,MICRO-RIBBON,JACK SCREW	681940	74868	57-1912-01	2	
J 18	CONN,MICRO-RIBBON,REC,PWB,RA,24 POS	658039	00779	553811-1	1	
J 19	CONN,D-SUB,PWB,RT ANG,25 PIN	706218	00779	747022-5	1	
JPR 1- 3, 5	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	757294	00779	850108-1	4	
L 10, 11	CHOKE,6TURN	320911	89536	320911	2	
MP 1	PLATE,IEEE/RS232	704411	89536	704411	1	
MP 2	EJECTOR,PWB,NYLON	706879	30035	CE-110-062	2	
R 1, 16	RES,CF,4.7K,+5%,0.25W	348821	59124	CF1/4 472J	2	
R 3	RES,CF,1M,+5%,0.25W	348987	59124	CF1/4 105J	1	
R 4, 9, 27,	RES,CF,10K,+5%,0.25W	348839	59124	CF1/4 102J	4	
R 28		348839				
R 5	RES,CF,1K,+5%,0.25W	343426	59124	CF1/4 102J	1	
R 8	RES,CF,180K,+5%,0.25W	348946	59124	CF1/4 184J	1	
R 10	RES,CF,47K,+5%,0.25W	348896	59124	CF1/4 473J	1	
R 11- 13	RES,MF,2.94K,+1%,0.125W,100PPM	261628	91637	CMF-55 2941F T-1	3	
R 14	RES,MF,12.1K,+1%,0.125W,100PPM	234997	91637	CMF-55 1212F T-1	1	
R 15	RES,MF,2.43K,+1%,0.125W,100PPM	312637	91637	CMF-55 2431F T-1	1	
R 19	RES,MF,4.75K,+1%,0.125W,100PPM	260679	91637	CMF-55 4751F T-1	1	
R 20	RES,MF,2.8K,+1%,0.125W,100PPM	325670	91637	CMF-55 2801F T-1	1	
R 21	RES,MF,274K,+1%,0.125W,100PPM	237297	91637	CMF-55 2743F T-1	1	
R 22	RES,MF,475K,+1%,0.125W,50PPM	348466	91637	CMF-55 4753F T-2	1	
R 23	RES,MF,4.02K,+1%,0.125W,100PPM	235325	91637	CMF-55 4021F T-1	1	
R 24	RES,MF,1K,+1%,0.125W,100PPM	168229	91637	CMF-55 1001F T-1	1	
R 25	RES,VAR,CERM,1K,+20%,0.5W	267856	80294	3009F-1-102	1	
R 26	RES,CF,8.2K,+5%,0.25W	441675	59124	CF1/4 822J	1	
S 1	SWITCH,DIP,SPST,10 POS	504878	00779	435640-7	1	
U 1	IC,FTTL,OCTAL INV BUFFER W/3-STATE	698001	04713	MC74F240N	1	
U 2, 9, 10,	IC,LSTTL,OCTAL BUFFER/LINE DRIVER	634105	01295	SN74LS541N	4	
U 82		634105				
U 3	IC,CMOS,DUAL 4BIT SER-IN,PAR-OUT SHFT	340125	04713	MC14015BCP	1	
U 4	IC,CMOS,QUAD 2 IN NAND W/SCHMT TRIG	404632	04713	MC14093BCP	1	
U 5, 6, 27	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	3	
U 7, 8	IC,LSTTL,OCTAL BUS TRNSVR W/3-ST OUT	477406	01295	SN74LS245N	2	
U 11, 28, 46-	IC,FTTL,OCTAL BUFFER W/3-STATE OUTPUT	686311	04713	MC74F244N	5	
U 48		686311				
U 12	IC,NMOS,FLOPPY DISK FORMATR CONTROLLR	723502	53848	FDC1797-02P	1	
U 13, 44, 60	IC,ALSTTL,OCTAL BUS XCVR W/3-STATE	647214	01295	SN74ALS245AN	3	
U 14	IC,16R8 PROG LOGIC ARRAY	736975	89536	736975	1	1
U 15, 16	IC,LSTTL,8-3 LINE PRIORITY ENCDR,3-ST	483669	01295	SN74LS348N	2	
U 17, 51, 64	IC,FTTL,HEX INVERTER	634444	04713	MC74F04N	3	
U 18	IC,16R6 PROG LOGIC ARRAY	712745	89536	712745	1	1
U 19	IC,FTTL,DUAL JK F/F,+EDG TRG,W/CL&SET	654673	04713	MC74F109N	1	
U 20	IC,16L8A PROG LOGIC ARRAY	712711	89536	712711	1	1
U 21	IC,LSTTL,QUAD BUS BFR W/3-STATE OUT	472746	01295	SN74LS125AN	1	
U 22	IC,16R8 PROG LOGIC ARRAY	712729	89536	712729	1	1
U 23, 30, 94,	IC,FTTL,DUAL D F/F,+EDG TRG,W/CL&SET	659508	04713	MC74F74N	4	
U 95		659508				

Table 4-7. A4 Single-Board Computer (SBC) PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
U 24	IC,CMOS,SERIAL I/O CALENDER & CLOCK	586412	33297	UPD4990AC	1	
U 25, 26	IC,LSTTL,8BIT ADDRESSABLE LATCH,W/CLR	419242	01295	SN74LS259N	2	
U 29	IC,16L8A PROG LOGIC ARRAY	712794	89536	712794	1	1
U 31	IC,16R4A PROG LOGIC ARRAY	712802	89536	712802	1	1
U 32, 88, 91	IC,FTTL,QUAD 2 INPUT AND GATE	650523	04713	MC74F08N	3	
U 33	IC,16R6 PROG LOGIC ARRAY	712737	89536	712737	1	1
U 34	IC,10L8,PROG LOGIC ARRAY	712778	89536	712778	1	1
U 35, 49, 63	IC,LSTTL,DUAL DIV BY 16 BINARY CNTR	483578	01295	SN74LS393N	3	
U 36- 43, 52-	IC,64K X 1 DYN RAM,256/4MS REFRESH	721944	01295	TMS4164-12NL	16	
U 59		721944				
U 45	IC,FTTL,8 LINE MUX W/SELECT	697763	04713	MC74F151N	1	
U 50	IC,16L8A PROG LOGIC ARRAY	712760	89536	712760	1	1
U 61	IC,NMOS,ASYN COMMUNICATION CONTROLLER	483552	01295	TMS9902ANL-40	1	
U 62	IC,FTTL,QUAD 2 INPUT OR GATE	659904	04713	MC74F32N	1	
U 65	IC,FTTL,TRIPLE 3 INPUT AND GATE	650549	04713	MC74F11N	1	
U 66	IC,16R4A PROG LOGIC ARRAY	737031	89536	737031	1	1
U 67	IC,NMOS,GPIB ADAPTER	585240	01295	TMS9914ANL	1	
U 68, 81	IC, 4K X 8 EPROM		89536		1	1, 2
U 69- 72	IC, 4K X 4 STAT RAM	686204	34335	AM2168-55DC	4	
U 73	IC,LSTTL,MEMORY MAPPERS W/3-STAT OUTS	685834	01295	SN74LS612N	1	
U 74	OSCILLATOR,23.9616MHZ,TTL CLOCK	696963	01537	K1145AM23.9616	1	
U 75	IC,NMOS,16 BIT MICROPROCESSOR	685842	01295	TMS99105A	1	
U 76, 85	IC,FTTL,OCTAL BIDIRECTIONAL XCEIVER	723460	07263	74F245PC	2	
U 77	IC,TTL,QUAD RS232C LINE DRIVER	414052	04713	MC1488P	1	
U 78, 84, 86	IC,FTTL,OCTAL TRNSPRNT LTCH W/3-STATE	686238	04713	MC74F373N	3	
U 79	IC,LSTTL,OCTAL GPIB XCVR W/OPEN COL	585224	01295	SN75160BN	1	
U 80	IC,LSTTL,OCTAL IEEE-488 BUS TRANSCVR	686022	01295	SN75162BN	1	
U 83	IC,TTL,QUAD RS232C LINE RECEIVER	524850	01295	SN75189AN	1	
U 87	IC,LSTTL,RETRG MONOSTAB MULTIV W/CLR	404186	01295	SN74LS123N	1	
U 89, 90, 93	IC,LSTTL,DUAL MONOSTAB MULTIV W/SCHMT	404202	01295	SN74LS221N	3	
U 92	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	
U 96	IC,STTL,TRIPLE 3 INPUT NAND GATE	483628	01295	SN74S10N	1	
U 97	IC,STTL,DUAL VOLTAGE CONTROLD OSCILTR	535922	01295	SN74S124N-00	1	
U 98	IC,OP AMP,GEN PURPOSE,COMPENSATED	402750	04713	MC1741CP1	1	
XU 12, 67, 73,	SOCKET,IC,40 PIN	429282	00779	2-640379-1	4	
XU 75		429282				
XU 14, 18, 20,	SOCKET,IC,20 PIN	454421	00779	2-640464-1	10	
XU 22, 29, 31,		454421				
XU 33, 34, 50,		454421				
XU 66		454421				
XU 68, 81	SOCKET,IC,28 PIN	448217	91506	228-AG39D	2	
Y 1	CRYSTAL,32.768KHZ,+/-0.003%	501817	87516	861-T-32.768	1	
Z 1- 7	RES,CERM,SIP,10 PIN,16 RES,330/680,5%	520429	91637	MSP10A-05-331/681J	7	
Z 8	RES,CERM,SIP,10 PIN,9 RES,4.7K,+/-2%	484063	91637	CSC10A-01-472G	1	
Z 9, 10	RES,CERM,SIP,10 PIN,9 RES,10K,+/-2%	414003	91637	CSC10A-01-103G	2	
Z 11	RES,CERM,SIP,6 PIN,5 RES,4.7K,+/-2%	494690	91637	CSC06A-01-472G	1	
Z 12	RES,CERM,SIP,6 PIN,5 RES,150,+/-2%	408294	91637	CSC06A-01-151G	1	
Z 13- 15	RES,CERM,SIP,10 PIN,5 RES,22,+/-2%	713867	91637	CSC10A-03-220G	3	
NOTES:	1. Static sensitive part. 2. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS. FOR 1722A/1752A V1.7 ORDER CHIP SET FLUKE STOCK NUMBER 712810. FOR 1722A/1752A V2.X ORDER CHIP SET FLUKE STOCK NUMBER 805143. FOR 1711A/AA V1.7 ORDER CHIP SET FLUKE STOCK NUMBER 805028. FOR 1711A/AA V2.X ORDER CHIP SET FLUKE STOCK NUMBER 793026. FOR 1722A/AP U68 ORDER FLUKE STOCK NUMBER 736942. FOR 1722A/AP U81 ORDER FLUKE STOCK NUMBER 736959.					



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Table 4-8. A5 Front Panel PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
C 1, 3	CAP,CER,1000PF,+10%,500V,X5S	357806	60705	562CX5FBA102EF102K	2	
C 2, 4	CAP,MICA,100PF,+5%,500V	148494	93790	CD15FD101J03	2	
C 5- 20	CAP,CER,56PF,+2%,100V,C0G	512970	04222	SR151A560GAT	16	
MP 1	PUSHBUTTON, SMALL RECT. DK ORANGE	420620	89536	420620	1	
MP 2	PUSHBUTTON, RECT. LIGHT BLUE	406876	89536	406876	1	
P 104	HEADER,1 ROW,.100CTR,6 PIN	631176	00779	640456-6	1	
P 105	HEADER,1 ROW,.100CTR,8 PIN	474213	00779	103747-8	1	
P 106	HEADER,2 ROW,.100CTR,26 PIN	603662	00779	1-102973-3	1	
SW 1, 2	SWITCH,PUSHBUTTON,SPNO MOMENTARY	507319	31918	MD DISC	2	
NOTES:	f Static sensitive part.					

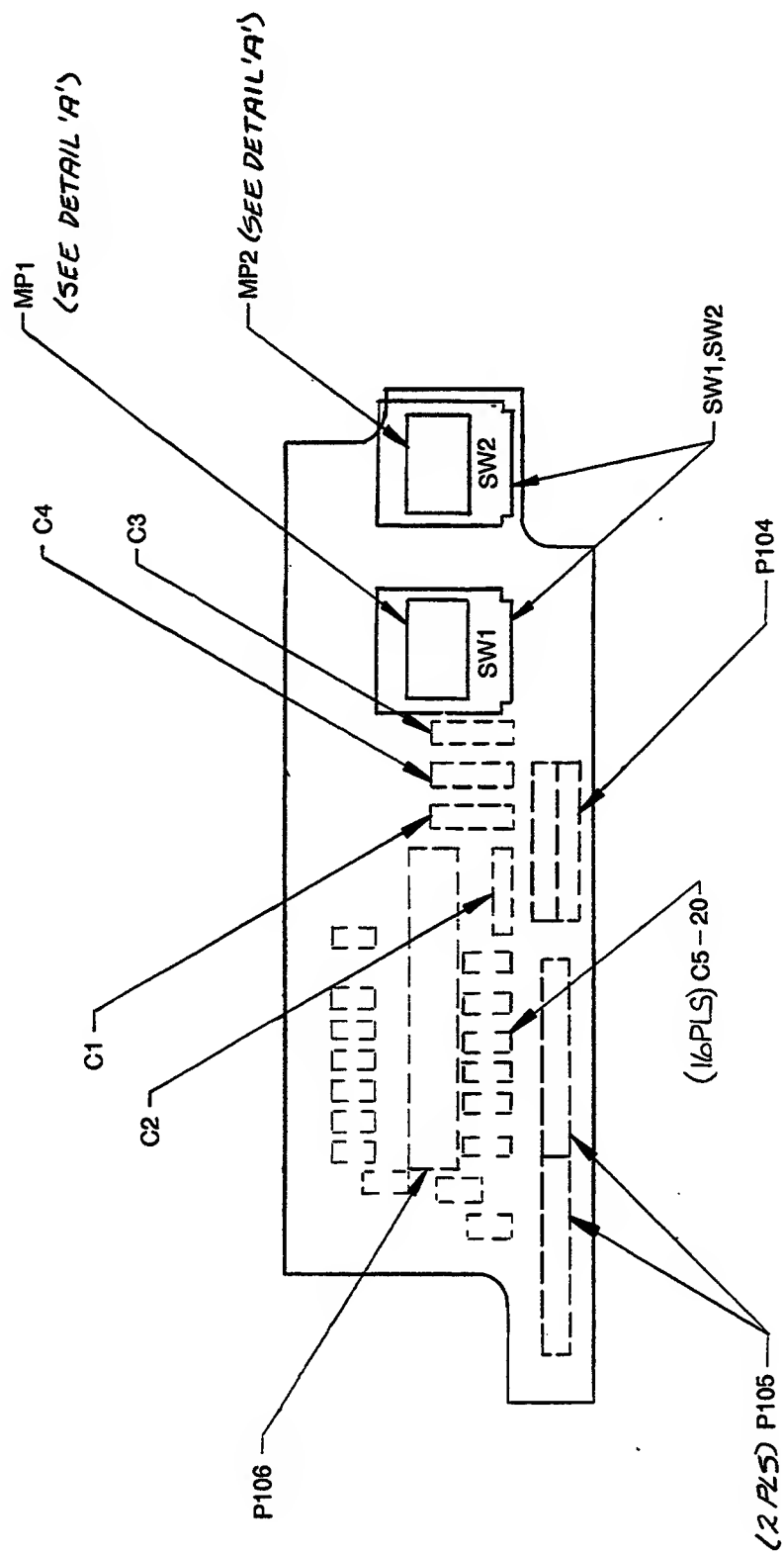


Table 4-9. A6 Programmer's Keyboard Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	† PROGRAMMER'S KEYBOARD PCA	718106	89536	718106	1	
H 1	SCREW,PH,P,LOCK,STL,6-32,.500	152173	73734	19046	4	
H 2	SCREW,PH,P,THD FORM,STL,5-20,.312	494641		COMMERCIAL	2	
MP 1	BOTTOM COVER,PAINTED	818583	89536	818583	1	
MP 2	TOP COVER,PAINTED	818575	89536	818575	1	
MP 3	DECAL,KEYBOARD TITLE	707778	89536	707778	1	
MP 4	FOOT,RUBBER,ADHES,BLK,.50 DIA,.14 THK	513820	28213	SJ-5012	2	
MP 5	DECAL, KEYBOARD BLANK	707786	89536	707786	1	
MP 6	CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	172080	06383	SST-1M	1	
W 1	KEYBOARD CABLE ASSY	656983	89536	656983	1	
NOTES:	† Static sensitive part.					

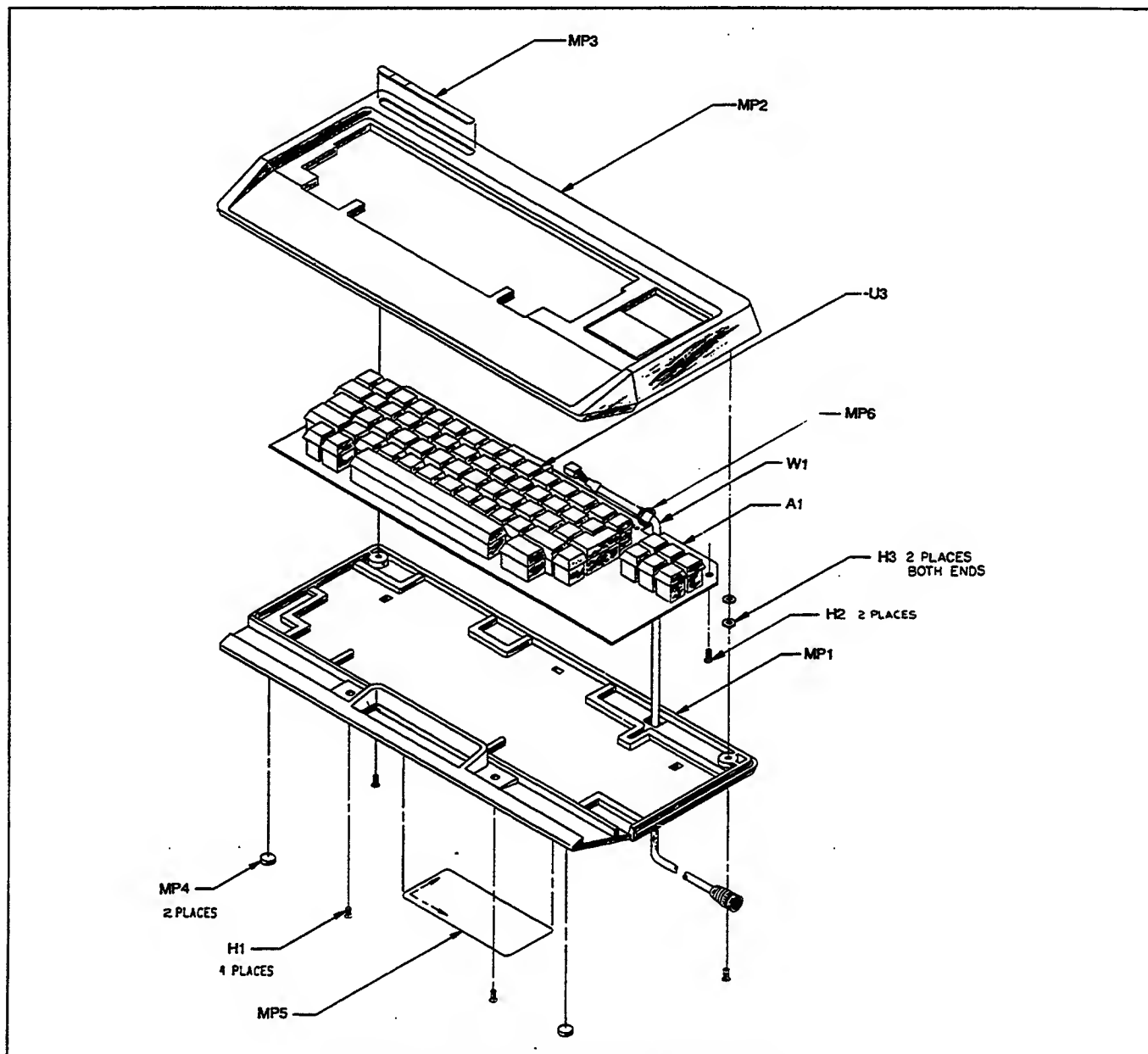


Figure 4-7. A6 Programmer's Keyboard Assembly

List of Replaceable Parts
PARTS LISTS

Table 4-10. A6A1 Programmer's Keyboard PCA

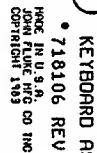
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 2, 4, 7	CAP,CER,0.22UF,+20%,50V,Z5U	519157	04222	SR205E224MAT	3	
C 9	CAP,AL,47UF,+50-20%,16V	436006	62643	SM16VB-47	1	
C 10	CAP,CER,5.6PF,+0.25PF,100V,C0H	512954	51406	RPE110C0H5R6C1	1	
C 11	CAP,CER,22PF,+2%,100V,C0G	512871	04222	SR151A220GAA	1	
C 13	CAP,TA,2.2UF,+10%,15V	364216	56289	199C225X9015AA2	1	
CR 1, 3	LED,RED,PCB MOUNT,LUM INT=2.0MCD	534859	53184	XC-5059R-2	2	
H 1	SCREW,PH,P,LOCK,STL,2-56,.250	149534	74594	149534	2	
J 1	HEADER,2 ROW,.100CTR,RT ANG,8 PIN	424200	00779	87230-4	1	
LS 1	AF TRANSD,PIEZO,24 MM	602490	51406	PKM24-4A1	1	
MP 1	KEYCAP SET	707331	89536	707331	1	
MP 2	SPACER,LED .250 LG	426882	89536	426882	2	
MP 3	SWITCH,PART,CRANK	682591	89536	682591	1	
MP 4	SWITCH,PART,LINK	682583	89536	682583	2	
MP 5	SWITCH,PART,GUIDE	682609	89536	682609	2	
R 1, 2	RES,CF,390,+5%,0.25W	441543	59124	CF1/4 391J	2	
SW 1- 64, 69,A1	SWITCH,PUSHBUTTON,SPST KEYBOARD	513473	31918	DC-61-03	66	
SW 70		513473				
U 1	IC,LSTTL,BCD-DEC CDCR/DRVR 15V OUT	419192	01295	SN74LS145N	1	
U 2	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	
U 3	IC,NMOS, 8 BIT MICROCOMPT,1KX8 EPROM	818559	89536	818559	1	1
XU 3	SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
Y 1	CRYSTAL,2.0000MHZ,+0.003%,HC18U	733352	61429	FOX-20S	1	
Z 1	RES,CERM,SIP,10 PIN,9 RES,10K,+2%	414003	91637	CSC10A-01-103G	1	
NOTES:	‡ Static sensitive part. 1. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS.					

Table 4-11. A12 Solar Cell PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 1	FOOT,RUBBER,ADHES,GRY,.44 DIA,.20 THK	358341	28213	SJ-5003	4	
R 1	RES,CF,200K,+5%,0.25W	441485	59124	CF1/4 204J	1	
S 1	SWITCH,SLIDE,2P3T	453183	79727	G-128S-0070	1	
TP 1, 2	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	2	
V 1	SOLARCELL,PHOTOVOLTAIC,1.5V,6UA	742262	97197	P36.644	1	
W 1	CABLE, SOLAR CELL	765222	89536	765222	1	
Z 1, 2	RES,CERM,DIP,16 PIN,8 RES,10,+5%	720987	91637	MDP16-03-10R0J	2	
NOTES:	‡ Static sensitive part.					

Table 4-12. A14 Keyboard Filter PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 5	CAP,CER,100PF,+2%,100V,C0G	512848	04222	SR151A101GAA	5	
L 1- 5	CHOKE,6TURN	320911	89536	320911	5	
MP 1	GROMMET,SLOT,RUBBER,.438,.062	100065	70485	505	1	
W 1	CABLE KIT, FRT PNL KEYBOARD FILTER	897517	89536	897517	1	
NOTES:	‡ Static sensitive part.					



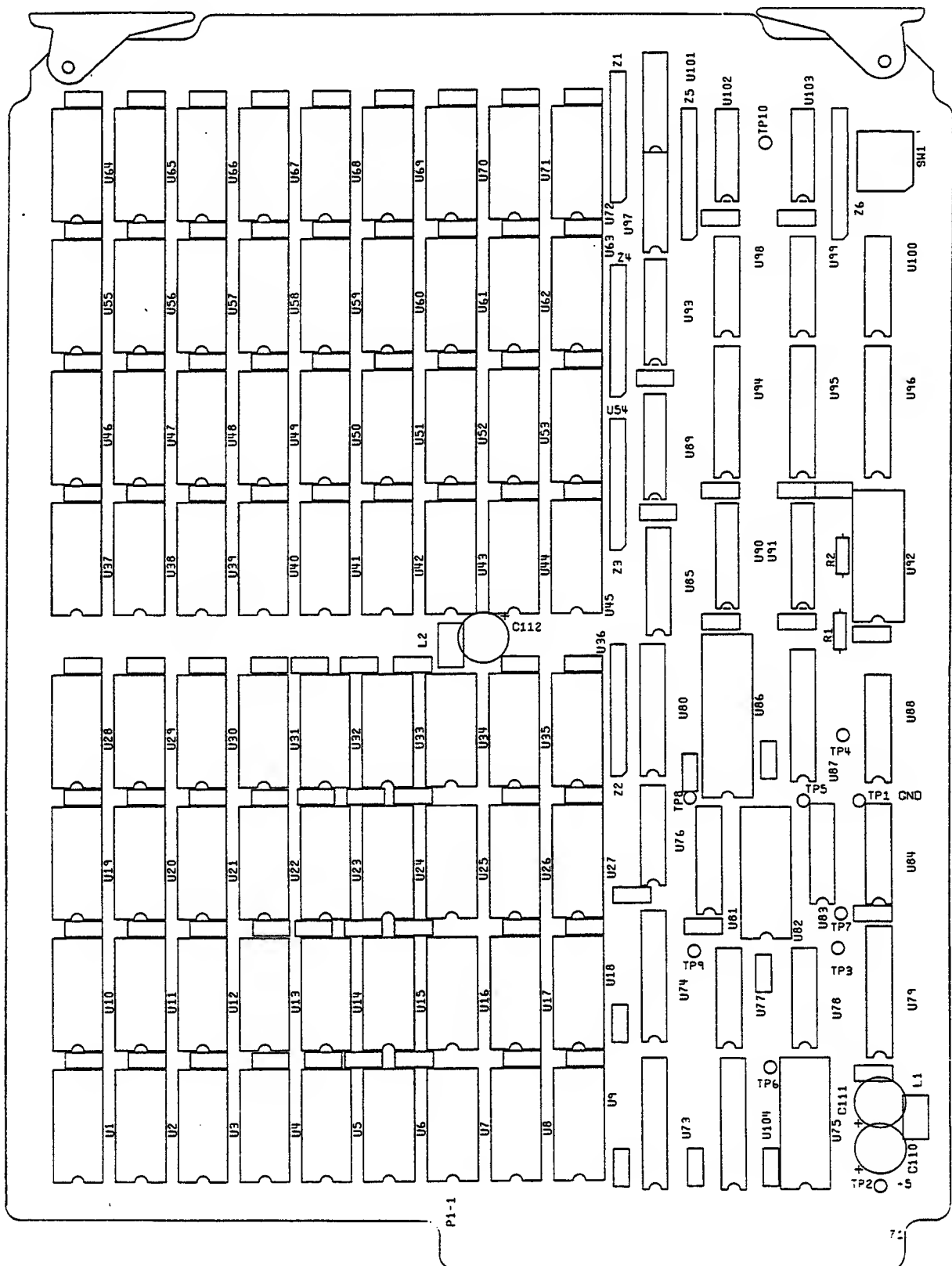
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Figure 4-8. A6A1 Programmer's Keyboard PCA

List of Replaceable Parts
PARTS LISTS

Table 4-13. Options -006(256K) -007(512K) -016(1M) -017(2M) RAM Expansion PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 10- 49	CAP,POLYES,0.1UF,+/-10%,50V	696484	37942	168-2-104K50AB		1
C 110-112	CAP,AL,100UF,+/-20%,6.3V,SOLV PROOF	615906	62643	SRAC6VB101M6X7C3	3	
L 1, 2	CHOKES,6TURN	320911	89536	320911	2	
MP 1	EJECTOR,PWB,NYLON	706879	30035	CE-110-062	2	
MP 2	DECAL, OPTION		89536		1	5
R 1, 2	RES,CF,1,+/-5%,0.25W	357665	59124	CF1/4 1R0J		2
SW 1	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
TP 1- 10	HEADER,1 ROW,.100CTR,6 PIN	478669	00779	103747-6	10	
U 1- 72	IC,64K X 1 DYN RAM,256/4MS REFRESH	721944	S4071	MSM3764A-12RS		3
U 73, 74	† IC,ALSTTL,OCTAL BUS XCVR W/3-STATE	647214	01295	SN74ALS245AN	2	
U 75	† IC,16R6 PROG LOGIC ARRAY	716506	89536	716506	1	4
U 76	† IC,FTTL,DUAL D F/F,+EDG TRG,W/CL&SET	659508	04713	MC74F74N	1	
U 77, 97	† IC,FTTL,9 BIT PARITY GEN/CHECKER	707513	04713	MC74F280N	2	
U 78,100	† IC,LSTTL,DUAL DIV BY 16 BINARY CNTR	483578	01295	SN74LS393N	2	
U 79, 80	† IC,FTTL,OCTAL INV BUFFER W/3-STATE	698001	04713	MC74F240N	2	
U 81	† IC,STTL,DUAL JK F/F,+EDG TRIG	363440	01295	SN74S112N	1	
U 82	† IC,16R6 PROG LOGIC ARRAY	716514	89536	716514	1	4
U 83	† IC,FTTL,QUAD 2 INPUT NAND GATE	654640	04713	MC74F00N	1	
U 84	† IC,STTL,4-2-3-2,INPUT,AND-OR-INV,W/OC	707455	01295	SN74S65N	1	
U 85	† IC,FTTL,DUAL 1 OF 4 DECODER	707414	04713	74F139N	1	
U 86	† HEX 16 INPUT AND-OR-INVERT ARRAY	716480	89536	718480	1	4
U 87, 94- 96, U 104	† IC,FTTL,OCTAL BUFFER W/3-STATE OUTPUT	686311	04713	MC74F244N	5	
U 88	† IC,FTTL,DUAL 4-INPUT MULTIPLEXER	659912	04713	MC74F153N	1	
U 89, 91	† IC,FTTL,QUAD 2 INPUT MULTIPLEXER	722082	04713	MC74F158N	2	
U 90, 93	† IC,FTTL,QUAD D F/F,+EDG TRG	722090	04713	MC74F175N	2	
U 92	† IC,16C1 PROG LOGIC ARRAY	716498	89536	716498	1	4
U 98, 99	† IC,FTTL,QUAD 2 INPUT XOR GATE	707273	04713	MC74F86N	2	
U 101	† IC,STTL,8 INPUT NAND GATE	407338	01295	SN74S30N	1	
U 102,103	† IC,FTTL,QUAD 2 INPUT AND GATE	650523	04713	MC74F08N	2	
XU 75, 82, 92	SOCKET,IC,20 PIN	454421	00779	2-640464-1	3	
XU 86	SOCKET,IC,24 PIN	643999	04221	703-4323-01-06-00	1	
Z 1- 5	RES,CERM,SIP,10 PIN,5 RES,22,+/-2%	713867	91637	CSC10A-03-220G	5	
Z 6	RES,CERM,SIP,10 PIN,9 RES,10K,+/-2%	414003	91637	CSC10A-01-103G	1	
NOTES:	† Static sensitive part. 1. FOR OPTION -006 QTY = 40. FOR OPTION -007 QTY = 57. FOR OPTION -016 QTY = 57. FOR OPTION -017 QTY = 92. 2. FOR OPTION -006 QTY = 1. NOT USED ON OPTION -007, R 1. FOR OPTION -016 QTY = 2. FOR OPTION -017 QTY = 1, R 2. 3. FOR OPTION -006 QTY = 36, U1-36. FOR OPTION -007 QTY = 72. NOT USED ON OPTION -016 ORDER FLUKE STOCK NUMBER 799932 QTY = 36, 256K X 1, U1-36. NOT USED ON OPTION -017 ORDER FLUKE STOCK NUMBER 799932 QTY = 72, 256K X 1. 4. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS. 5. FOR OPTION -006 ORDER FLUKE STOCK NUMBER 707570. FOR OPTION -007 ORDER FLUKE STOCK NUMBER 707588. FOR OPTION -016 ORDER FLUKE STOCK NUMBER 799205. FOR OPTION -017 ORDER FLUKE STOCK NUMBER 799213.					



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Figure 4-9. Option -006(256K) -007(512K) -016(1M) -017(2M) RAM Expansion PCA

Table 4-14. Option -008 IEEE/RS-232-C Interface PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,AL,47UF,+50-20%,16V	436006	62643	SM16VB-47	1	
C 2- 7	CAP,CER,330PF,+5%,100V,C0G	528620	04222	SR201A331JAT	6	
C 8	CAP,POLYES,0.1UF,+10%,50V	696484	37942	168-2-104K50AB	1	
C 9	CAP,MICA,100PF,+5%,500V	148494	93790	CD15FD101J03	1	
C 10	CAP,CER,1000PF,+10%,500V,X5S	357806	60705	562CX5FBA102EF102K	1	
C 11- 27	CAP,POLYES,0.22UF,+10%,50V	696492	37942	168-2-224K50AB	17	
H 1	CONN ACC,MICRO-RIBBON,JACK SCREW	681940	74868	57-1912-01	2	
H 2	EJECTOR,PWB,NYLON	706879	30035	CE-110-062	2	
H 3	WASHER,FLAT,ALUM,0.125X0.250X0.062	381749		COMMERCIAL	2	
H 4	WASHER,FLAT,BRASS,#4,0.025	110775		COMMERCIAL	2	
J 18	CONN,MICRO-RIBBON,REC,PWB,RA,24 POS	658039	00779	553811-1	1	
J 19	CONN,D-SUB,PWB,RT ANG,25 PIN	706218	00779	747022-5	1	
L 1, 2	CHOKO,6TURN	320911	89536	320911	2	
MP 1	PLATE,IEEE/RS232	704411	89536	704411	1	
MP 2	DECAL,OPTION	707604	89536	707604	1	
MP 3	DECAL,INSTRUMENT PORT	707562	89536	707562	1	
MP 4	DECAL,SERIAL PORT	707554	89536	707554	1	
SW 1	SWITCH,DIP,SPST,10 POS	504878	00779	435640-7	1	
SW 2	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
TP 1- 4	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	4	
U 1	† IC,NMOS,GPIB ADAPTER	585240	01295	TMS9914ANL	1	
U 2	† IC,NMOS,ASYN COMMUNICATION CONTRLLR	483552	01295	TMS9902ANL-40	1	
U 3	† HEX 16 INPUT AND-OR-INVERT ARRAY	711630	89536	711630	1	1
U 4	† IC,16LSA PROG LOGIC ARRAY	711622	89536	711622	1	1
U 5, 6	† IC,FTTL,OCTAL BUFFER W/3-STATE OUTPUT	686311	04713	MC74F244N	2	
U 7	† IC,FTTL,QUAD 2 INPUT OR GATE	659904	04713	MC74F32N	1	
U 8	† IC,TTL,QUAD RS232C LINE DRIVER	414052	04713	MC1488P	1	
U 9	† IC,TTL,QUAD RS232C LINE RECEIVER	524850	01295	SN75189AN	1	
U 10	† IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	1	
U 11	† IC,LSTTL,OCTAL GPIB XCVR W/OPEN COL	585224	01295	SN75160BN	1	
U 12	† IC,LSTTL,OCTAL IEEE-488 BUS TRANSCVR	686022	01295	SN75162BN	1	
U 13	† IC,LSTTL,OCTAL BUFFER/LINE DRIVER	634105	01295	SN74LS541N	1	
U 14	† IC,LSTTL,OCTAL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	
U 15	† IC,FTTL,QUAD 2 INPUT XOR GATE	707273	04713	MC74F86N	1	
XU 1	SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
XU 3	SOCKET,IC,24 PIN	643999	04221	703-4323-01-06-00	1	
XU 4	SOCKET,IC,20 PIN	454421	00779	2-640464-1	1	
Z 1, 5	RES,CERM,SIP,6 PIN,5 RES,10K,+2%	500876	91637	CSC06A-01-103G	2	
Z 2, 4	RES,CERM,SIP,10 PIN,9 RES,10K,+2%	414003	91637	CSC10A-01-103G	2	
Z 3	RES,CERM,SIP,8 PIN,4 RES,4.7K,+2%	573881	91637	CSC08A-03-472G	1	
NOTES:	† Static sensitive part. 1. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS.					

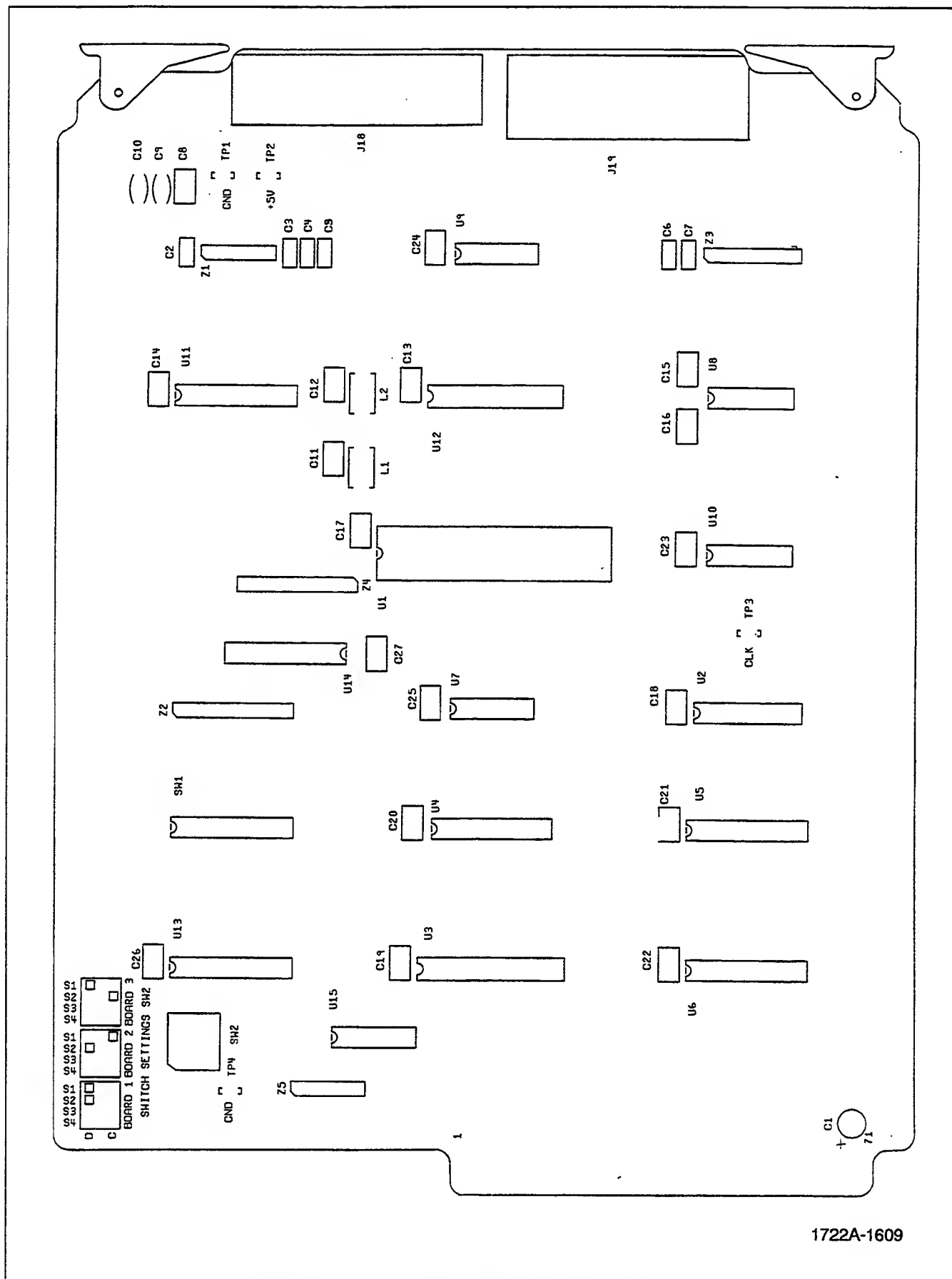


Figure 4-10. Option -008 IEEE/RS-232-C Interface PCA

List of Replaceable Parts
PARTS LISTS

Table 4-15. Option -009 Dual Serial Interface PCA

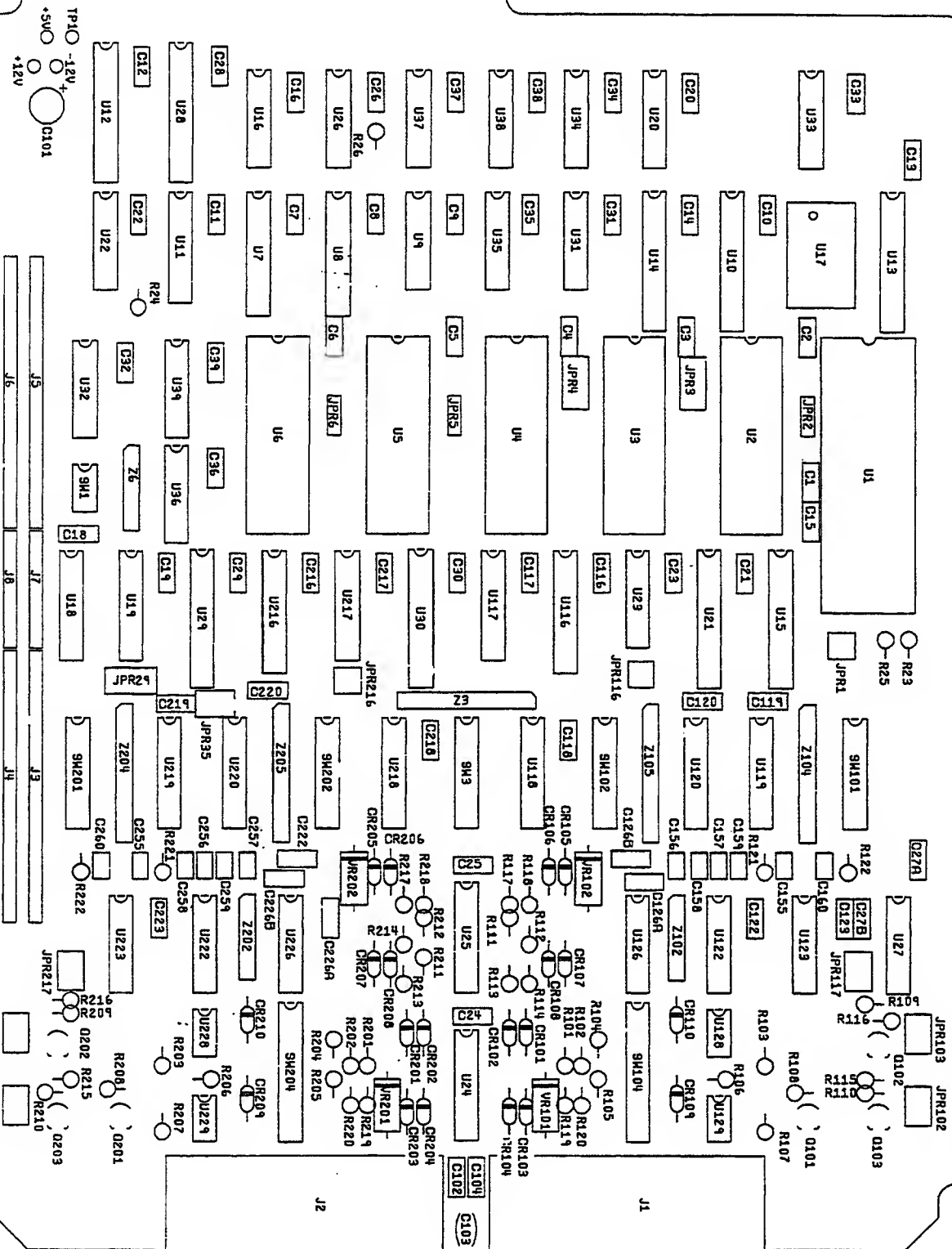
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 16, 18- C 23, 25- 39, C 116-120,122, C 123,126,216- C 220,222,223, C 226	CAP,POLYES,0.22UF,+10%,50V	696492 696492 696492 696492 696492 696492	37942	168-2-224K50AB	53	
C 101	CAP,AL,47UF,+20%,10V,SOLV PROOF	602334	62643	SRAC10VB47RM6X7C3	1	
C 102	CAP,POLYES,0.1UF,+10%,50V	696484	37942	168-2-104K50AB	1	
C 103	CAP,MICA,100PF,+5%,500V	148494	93790	CD15FD101J03	1	
C 104	CAP,CER,1000PF,+10%,500V,X5S	357806	60705	562CX5FBA102EF102K	1	
C 155-160,255- C 260	CAP,CER,330PF,+5%,100V,C0G	528620 528620	04222	SR201A331JAT	12	
CR 101-110,201- CR 210	DIODE,SI,50 PIV,1.0 AMP	379412 379412	04713	1N4933	20	
H 1	WASHER,FLAT,ALUM,0.125X0.250X0.062	381749		COMMERCIAL	4	
J 1, 2	CONN,D-SUB,PWB,RT ANG,25 PIN	706218	00779	747022-5	2	
J 3, 5	SOCKET,1 ROW,PWB,0.100CTR,20 POS	447110	30035	SS-109-1-20	2	
J 4, 6	SOCKET,1 ROW,PWB,0.100CTR,20 POS	443077	00779	643119-1	2	
J 7	SOCKET,1 ROW,PWB,0.100CTR,9 POS	436774	30035	SS-109-1-09	1	
J 8	SOCKET,1 ROW,PWB,0.100CTR,9 POS	424150	00779	643109-1	1	
JPR 1- 6, 29, JPR 35,102,103, JPR116,117,202, JPR203,216,217	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	757294 757294 757294 757294	00779	850108-1	16	
JPR 7	HEADER,2 ROW,.100CTR,50 PIN	732875	00779	2-102973-5	1	
JPR 8	HEADER,1 ROW,.100CTR,6 PIN	478669	00779	103747-6	1	
MP 1	EJECTOR,PWB,NYLON	706879	30035	CE-110-062	2	
MP 2	PLATE,RS232/RS232	704403	89536	704403	1	
MP 3	DECAL,OPTION	707612	89536	707612	1	
MP 4	DECAL,SERIAL PORT	707554	89536	707554	1	
Q 101,201	† TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	218396	04713	2N3904	2	
Q 102,103,202, Q 203	† TRANSISTOR,SI,PMP,SMALL SIGNAL	195974 195974	04713	2N3906	4	
R 23- 25,107, R 119-122,207, R 219-222	RES,CF,47K,+5%,0.25W	348896 348896 348896	59124	CF1/4 473J	13	
R 26	RES,CF,1K,+5%,0.25W	343426	59124	CF1/4 102J	1	
R 101,102,201, R 202	RES,CF,100,+5%,0.25W	348771 348771	59124	CF1/4 101J	4	
R 103,203	RES,CF,2K,+5%,0.25W	441469	59124	CF1/4 202J	2	
R 104,105,109, R 115,204,205, R 215,216	RES,CF,24,+5%,0.25W	442210 442210 442210	59124	CF1/4 240J	8	
R 106,206	RES,CF,220,+5%,0.25W	342626	59124	CF1/4 221J	2	
R 108,208	RES,CF,560,+5%,0.25W	385948	59124	CF1/4 561J	2	
R 110,116,209, R 210	RES,CF,300,+5%,0.25W	441519 441519	59124	CF1/4 301J	4	
R 111,112,117, R 118,211,212, R 217,218	RES,CF,51,+5%,0.25W	414540 414540 414540	59124	CF1/4 510J	8	
R 113,114,213, R 214	RES,CF,33,+5%,0.25W	414524 414524	59124	CF1/4 330J	4	
SW 1	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
SW 3,101,102	SWITCH,DIP,SPST,8 POS	414490	00779	435166-5	3	
SW 104,204	SWITCH,DIP,SPST,10 POS	504878	00779	435640-7	2	
U 1	† IC,NMOS,16 BIT MICROCOMPUTER	640417	01295	MP9572N	1	
U 2, 5, 6	† IC, 2K X 8 STAT RAM	584144	49569	IDT6116SA-45P	3	
U 4	IC,NMOS, 8K X 8 EPROM	749416	89536	749416	1	1
U 7, 8,116, U 216	† IC,NMOS,ASYNC COMMUNICATION CONTROLLER	483552 483552	01295	TMS9902ANL-40	4	
U 9	† IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	01295	SN74LS11N	1	

Table 4-15. Option -009 Dual Serial Interface PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
U 10	‡ IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	
U 11,117,217	‡ IC,LSTTL,8BIT ADDRABLE LATCH,W/CLR	419242	01295	SN74LS259N	3	
U 12- 15	‡ IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	4	
U 16, 33	‡ IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	2	
U 17	OSCILLATOR,8MHZ,TTL CLOCK	584169	91637	XC-43 B 8	1	
U 18, 19	‡ IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	2	
U 20	‡ IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	
U 21	‡ IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	
U 22	‡ IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	1	
U 23	‡ IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	
U 24	‡ IC,LSTTL,QUAD RS422 LINE RCVR,3-STATE	525303	04713	MC3486P	1	
U 25	‡ IC,LSTTL,QUAD DIFFERENTIAL LINE DRVR	525295	04713	MC3487P	1	
U 26, 32, 39	‡ IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	3	
U 27,126,226	‡ IC,TTL,QUAD RS232C LINE DRIVER	414052	04713	MC1488P	3	
U 28- 30	‡ IC,LSTTL,OCTL INV LINE DRVR W/3-STATE	429480	01295	SN74LS240N	3	
U 31	‡ IC,LSTTL,QUAD BUFFER W/3-STATE OUTPUT	585273	01295	SN74LS126AN	1	
U 34, 35	‡ IC,LSTTL,TRIPLE 3 INPUT NAND GATE	393074	01295	SN74LS10N	2	
U 36	‡ IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N	1	
U 37, 38	‡ IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	2	
U 118,119,218, U 219	‡ IC,LSTTL,8-1 MUX W/3-STATE OUTPUTS	407577	01295	SN74LS251N	4	
U 122,123,222, U 223	‡ IC,TTL,QUAD RS232C LINE RECEIVER	414045	01295	SN1489NP	4	
U 128,228	‡ ISOLATOR,OPTO,HI-SPEED,LED TO XSISTOR	407742	28480	6N136	2	
U 129,229	‡ ISOLATOR,OPTO,LED TO TRANSISTOR	380014	14936	MCT2	2	
VR 101,102,201, VR 202	‡ ZENER,TRANS SUPPRESSOR,6V	508655	11961	1N5908 Bulk	4	
XU 1	SOCKET,IC,40 PIN	429282	00779	2-640379-1	1	
XU 2- 6	SOCKET,IC,28 PIN	448217	91506	228-AG39D	5	
Z 3,104,204	RES,CERM,SIP,10 PIN,5 RES,47K,+/-2%	485193	91637	CSC10A-01-473G	3	
Z 6	RES,CERM,SIP,6 PIN,5 RES,10K,+/-2%	500876	91637	CSC06A-01-103G	1	
Z 102,202	RES,CERM,SIP,6 PIN,5 RES,4.7K,+/-2%	494690	91637	CSC06A-01-472G	2	
NOTES:	‡ Static sensitive part. 1. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS.					

List of Replaceable Parts

PARTS LISTS



1722A-1610

Figure 4-11. Option -009 Dual Serial Interface PCA

Table 4-16. Option -010 Analog Measurement Processor PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 6, 10, C 11, 14	CAP,POLYES,0.22UF,+10%,50V	696492	37942	168-2-224X50AB	9	
C 7	CAP,TA,10UF,+20%,10V	696492	56289	199D106X0010EA2	1	
C 8, 9, 79, C 80	CAP,AL,33UF,+20%,25V,SOLV PROOF	715250	62643	SRAC25VB33RM6X7C3	4	
C 12, 13	CAP,CER,18PF,+2%,100V,C0G	715250				
C 15, 17, 18	CAP,POLYES,0.01UF,+10%,50V	512335	51406	RPE110A184G1	2	
C 16, 19, 20	CAP,TA,2.2UF,+20%,20V	715037	37942	185-2-103K50A/A	3	
C 21, 38	CAP,POLYPR,220PF,+1%,100V	161927	56289	199D225X0020BA2	3	
C 22	CAP,POLYES,0.47UF,+10%,50V	886994	68919	FKP2221F100	2	
C 23, 24	CAP,AL,22UF,+20%,16V,SOLV PROOF	714725	37942	168-2-474X50AE	1	
C 25, 39- 41, C 44- 75, 83	CAP,POLYES,0.001UF,+10%,50V	614750	62643	SRAC16VB22RM5X7C3	2	
C 26, 27, 30- C 33	CAP,TA,10UF,+20%,25V	720938	37942	185-2-112K50AA	37	
C 28, 29	CAP,TA,4.7UF,+20%,25V	720938				
C 34, 35, 42, C 43	CAP,TA,1UF,+10%,35V	714774	56289	199D106X0025CG2	6	
C 36	CAP,POLYPR,0.047UF,+10%,50V	714774				
C 37	CAP,POLYES,0.1UF,+10%,50V	161943	56289	199D475X0025BA2	2	
C 76, 77	CAP,POLYPR,1000PF,+1%,100V	161919	56289	199D105X0035AA2	4	
C 78	CAP,AL,47UF,+20%,10V,SOLV PROOF	413328	84411	JF-8647310%50V	1	
C 81	CAP,CER,100PF,+2%,100V,C0G	696484	37942	168-2-104K50AB	1	
C 82	CAP,CER,0.22UF,+20%,50V,Z5U	844816	68919	FKP2 102F 100V	2	
CR 1	DIODE,SI,SCHOTTKY BARRIER,SMALL SIGNAL	602334	62643	SRAC10VB47RM6X7C3	1	
CR 2, 7	DIODE,SI,BV=75V,IO=150MA,500MW	512848	04222	SR151A101GAA	1	
CR 3- 6	DIODE,SI,50 PIV,1.0 AMP	519157	04222	SR205E224MAT	1	
CR 8	DIODE,GER,BV=100.0V,IO= 80MA,80 MW	313247	28480	5082-6264 T25	1	
E 1	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	203323	09214	IN4448	2	
F 1	FUSE,.25X1.25,0.125A,250V,FAST	379412	04713	1N4933	4	
H 1	HEADER ACC,POLARIZING KEY	149187	66891	IN270	1	
H 2	SCREW,PH,P,LOCK,STL,4-40,.250	757294	00779	850108-1	1	
H 3	SCREW,PH,P,LOCK,STL,2-56,.375	196790	71400	AGC1-8	1	
H 4	NUT,HEX,STL,2-56	542860	28213	3518-0000	2	
H 5	WASHER,LOCK,INTRNL,STL,.095ID	129890	74594	129890	4	
J 1, 2	HEADER,2 ROW,.100CTR,RT ANG,26 PIN	196634	74594	196634	4	
J 3	JACK,PWB,RT ANG	110668		COMMERCIAL	4	
J 4	HEADER,2 ROW,.100CTR,50 PIN	110676		COMMERCIAL	4	
JPR 2, 32	HEADER,1 ROW,.100CTR,6 PIN	572289	00779	746180-6	2	
L 1, 2	CHOKE,6TURN	423897	91967	6-205P	1	
MP 1	EJECTOR,PWB,NYLON	732875	00779	2-102973-5	1	
MP 2	CABLE ACCESS,TIE,4.00L,.10W,.75 DIA	478669	00779	103747-6	2	
MP 3	POST, CHASSIS GROUND	320911	89536	320911	2	
MP 4	DECAL,OPTION	494724	32559	CP-66	2	
Q 1, 4, 9- Q 12	TRANSISTOR,SI,PNP,SMALL SIGNAL	172080	06383	SST-1M	1	
Q 2, 3	TRANSISTOR,SI,VMOS,PWR,TO-237,VN10KM	754713	89536	754713	2	
Q 5, 6	TRANSISTOR,SI,N-JFET,REMOTE CUTOFF	759126	89536	759126	1	
Q 7, 8, 13- Q 76	TRANSISTOR,SI,N-JFET,TO-92	195974	04713	2N3906	6	
R 1, 2, 4, R 5, 8, 39, R 40, 95- 97	RES,CF,10K,+5%,0.25W	348839	59124	CF1/4 102J	10	
R 3,101	RES,CF,1K,+5%,0.25W	348839				
R 6, 20, 29, R 30, 98-100	RES,CF,4.7K,+5%,0.25W	348839	59124	CF1/4 102J	2	
R 7	RES,CF,2.2K,+5%,0.25W	348821	59124	CF1/4 472J	7	
R 9	RES,CF,100,+5%,0.25W	343400	59124	CF1/4 222J	1	
R 10	RES,CF,51,+5%,0.25W	348771	59124	CF1/4 101J	1	
R 11, 18, 28	RES,CF,33K,+5%,0.25W	414540	59124	CF1/4 510J	1	
R 12, 27, 33	RES,CF,51K,+5%,0.25W	348888	59124	CF1/4 333J	3	
R 14	RES,CF,430K,+5%,0.25W	376434	59124	CF1/4 513J	3	
R 15, 22	RES,CF,330K,+5%,0.25W	442483	59124	CF1-4 4303J	1	
R 16	RES,CF,2.7M,+5%,0.25W	376640	59124	CF1/4 334J	2	
R 17, 21	RES,CF,100K,+5%,0.25W	442608	59124	CF1/4 275J	1	
R 19	RES,CF,390K,+5%,0.25W	348920	59124	CF1/4 104J	2	
R 23, 24	RES,CF,0.51,+5%,0.25W	442475	59124	CF1/4 394J	1	
R 25	RES,MF,1M,+1%,0.125W,100PPM	381954	59124	CF1/4 0R51J	2	
R 26, 36	RES,MF,45.3K,+1%,0.125W,100PPM	268797	91637	CMF-55 1004F T-1	1	
R 31, 32	RES,CF,10,+5%,0.25W	234971	91637	CMF-55 4532F T-1	2	
R 34	RES,VAR,CERM,100K,+10%,0.5W	340075	59124	CF1/4 100J	2	
R 35	RES,MF,1.05M,+1%,0.125W,100PPM	369520	32997	3386R-1-104	1	
R 37	RES,MF,10K,+1%,0.125W,100PPM	260737	91637	CMF-55 1054F T-1	1	
R 38	RES,CF,6.2K,+5%,0.25W	168260	91637	CMF-55 1002F T-1	1	
		442368	59124	CF1/4 622J	1	

List of Replaceable Parts
PARTS LISTS

Table 4-16. Option -010 Analog Measurement Processor PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 41, 46, 47, R 50- 53, 56- R 59, 62- 65, R 68- 71, 74- R 77, 80- 83, R 86- 89, 92, R 93	RES,MF,FLMPRF,FUSIBLE,10K,+/-1%,0.5W	746081 746081 746081 746081 746081 746081 746081	91637	CMF-60 1002F	33	
R 42	RES,MF,1K,+/-1%,0.5W,FLMPRF,FUSIBLE	733915	91637	CMF-60 1001F T-1	1	
R 43	RES,CF,4.7,+/-5%,0.25W	441584	59124	CF1/4 4R7J	1	
R 44, 45	RES,CF,20K,+/-5%,0.25W	441477	59124	CF1/4 151J	2	
R 48, 49, 54, R 55, 60, 61, R 66, 67, 72, R 73, 78, 79, R 84, 85, 90, R 91	RES,WW,15,+/-0.04%,.33W	459958 459958 459958 459958 459958	05347	205A15R0.04%	16	
R 94	RES,CF,20,+/-5%,0.25W	442202	59124	CF1/4 200J	1	
RV 1	VARISTOR,8.2V,+/-35%,1.0MA	715052	S3385	SNR-8R0MD07	1	
S 1	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
TP 1- 3, 13	HEADER,1 ROW,.100CTR,2 PIN	643916	00779	103747-2	4	
U 1	IC,NMOS, 2K X 8 EEPROM	776260	89536	776260	1	1
U 2	IC, 2K X 8 STAT RAM	584144	49569	IDT6116SA-45P	1	
U 3, 25	IC,CMOS,12STAGE RIPPLE CARRY BIN CNTR	429605	04713	MC14040BCP	2	
U 4	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	1	
U 5	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	
U 6	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	
U 7, 9- 11	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	4	
U 8	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	
U 12, 13	IC,LSTTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	2	
U 14	IC,NMOS,8 BIT MICROPROCESSOR	647099	04713	MC68B09P	1	
U 15	IC,NMOS,6522A,VERSATILE INTRFC ADPT	723676	34576	R6522AP	1	
U 16, 17	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	2	
U 18	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	
U 19	IC,FTTL,DUAL 1 OF 4 DECODER	707414	04713	74F139N	1	
U 20	IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	1	
U 21	IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N	1	
U 22	IC,BIP,16BIT DAC,15BIT ACCUR,VOLT OUT	723668	13919	DAC703KE	1	
U 23	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	
U 24	IC,CMOS,PHASE LOCKED LOOP,16 PIN DIP	403584	04713	MC14046BCP	1	
U 26	IC,LINER,BIPOLAR 398. SAMPLE/HOLD	723692	18324	LF398N	1	
U 27, 28	IC,OP AMP,DUAL,JFET INPUT,8 PIN DIP	495119	12040	LF353BN	2	
U 29	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	1	
U 30	IC,VOLT REG,FIXED,+15 VOLTS,1.5 AMPS	413187	04713	MC7815CT	1	
U 31	IC,VOLT REG,FIXED,-15 VOLTS,1.5 AMPS	413179	04713	MC7915CT	1	
U 32	IC,6.95V,2 PPM T.C., VOLTAGE REF	723775	27014	LM399AH	1	
U 33, 34	IC,CMOS, 4 CHANNEL DIFF ANALOG MUX	723650	34371	IH608CPE	2	
U 35, 36	IC,CMOS, 16 CHANNEL ANALOG MUX	723684	34371	IH5116CPI	2	
U 37	IC,LSTTL,RETRG MONOSTAB MULTIVIB W/CLR	404186	01295	SN74LS123N	1	
U 38	IC,FTTL,QUAD D F/F,+EDG TRG	722090	04713	MC74F175N	1	
VR 1	ZENER,UNCOMP,4.7V,5%,20.0MA,0.4W	524058	04713	1N750	1	
VR 2	ZENER,UNCOMP,15.0V,5%,8.5MA,0.4W	266601	04713	1N965	1	
XF 1, 2	HLDR,FUSE,1/4,PWB MT	485219	91833	3529	2	
XU 1, 35, 36	SOCKET,IC,28 PIN	448217	91506	228-AG39D	3	
XU 2, 22	SOCKET,IC,24 PIN	376236	00779	2-640361-1	2	
XU 14, 15	SOCKET,IC,40 PIN	429282	00779	2-640379-1	2	
XU 28	SOCKET,IC,8 PIN	478016	00779	2-640463-1	1	
Y 1	CRYSTAL,8MHZ,+/-0.5%,HC-18/U	485060	5W664	NDK-HC-18/U-080	1	
Z 1	RES,CERM,SIP,10 PIN,9 RES,10K,+/-2%	414003	91637	CSC10A-01-103G	1	
Z 2, 3	REF DIVIDER RES NET ASSY TESTED -510A	645341	89536	645341	2	
Z 4	RNET,8840A OUTPUT DIVIDER	655811	89536	655811	1	
Z 5	RES,CERM,DIP,16 PIN,8 RES,10K,+/-5%	500710	91637	MDP16-03-103J	1	
Z 6	RES,CERM,SIP,6 PIN,5 RES,3.6K,+/-2%	478818	91637	CSC06A-01-362G	1	
NOTES:	‡ Static sensitive part. 1. SEE TABLE 4-2 FOR PART NUMBER OF EARLIER REVISIONS.					

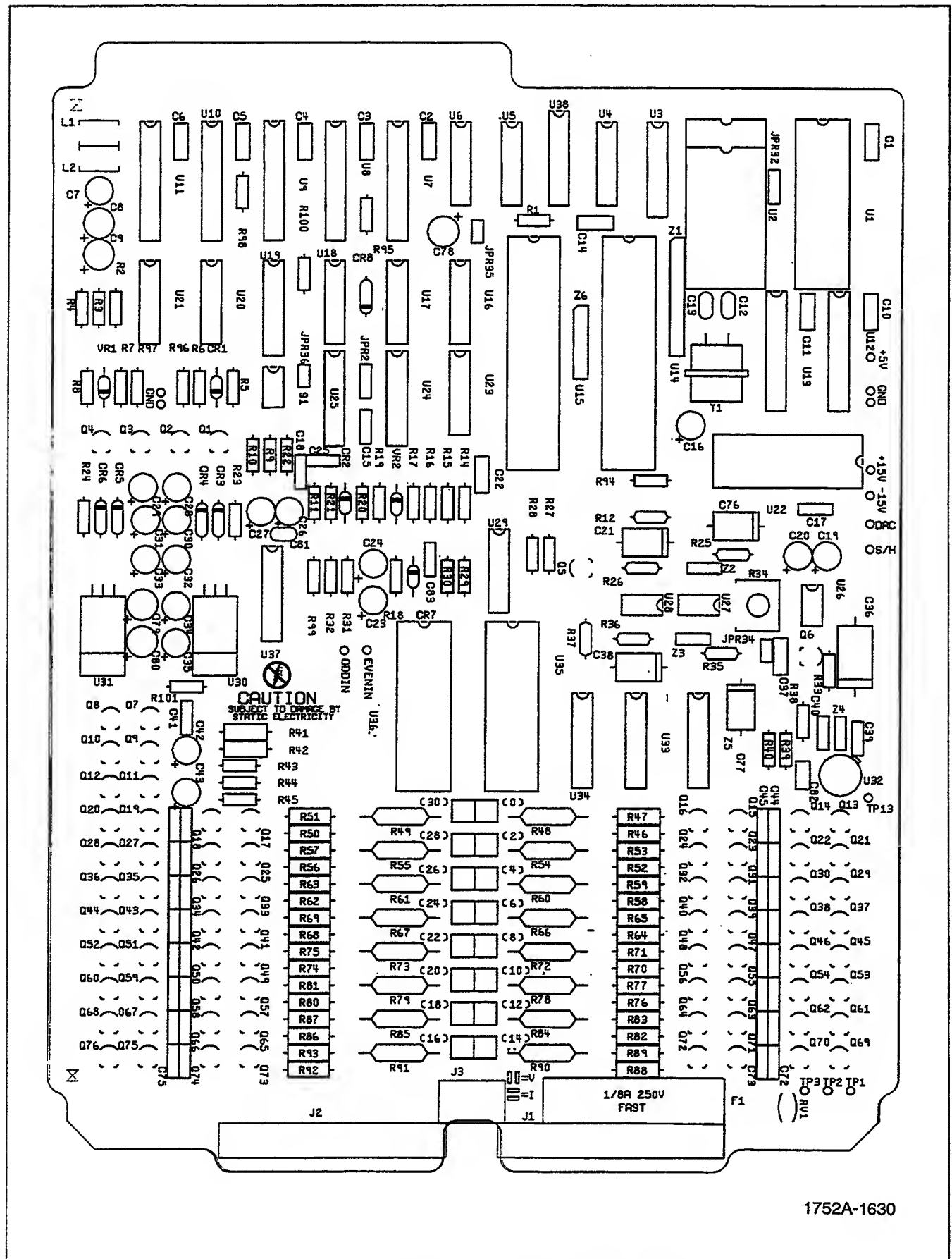


Figure 4-12. Option -010 Analog Measurement Processor PCA

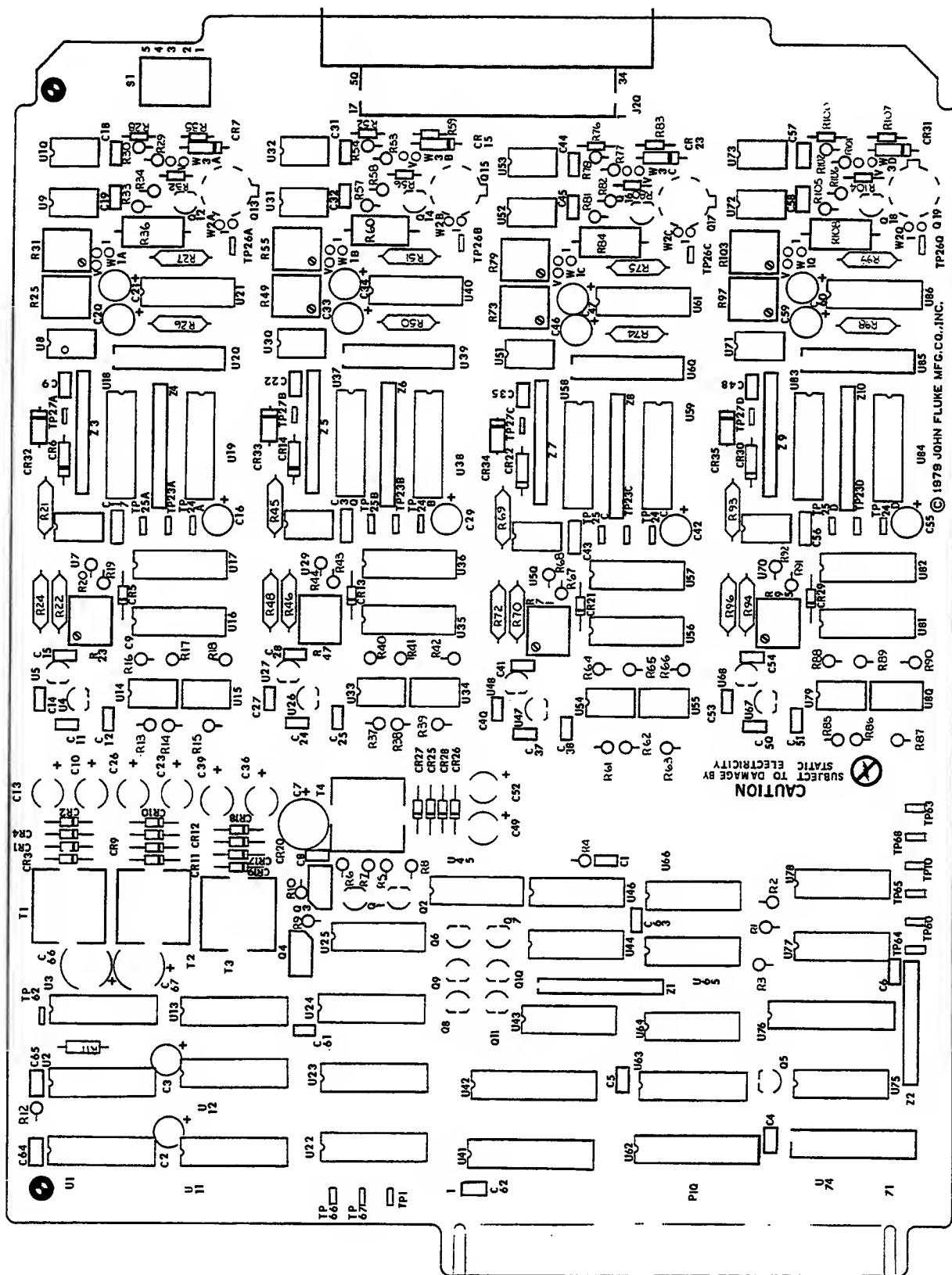
List of Replaceable Parts
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Table 4-17. Option -011 Analog Output PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,CER,15PF,+/-2%,100V,C0G	369074	59660	8101-100-C0G-150-G	1	
C 2, 3	CAP,TA,10UF,+/-20%,10V	176214	56289	199D106X0010EA2	2	
C 4- 6, 8,	CAP,CER,0.22UF,+/-20%,50V,25U	519157	04222	SR205E224MAT	25	
C 11, 12, 14,		519157				
C 15, 24, 25,		519157				
C 27, 28, 37,		519157				
C 38, 40, 41,		519157				
C 50, 51, 53,		519157				
C 54, 61- 65		519157				
C 7, 66, 67	CAP,TA,68UF,+/-20%,15V	193615	56289	199D686X0015EA2	3	
C 9, 22, 35,	CAP,CER,33PF,+/-2%,100V,C0G	513226	04222	SR151A330GAA	4	
C 48		513226				
C 10, 13, 23,	CAP,TA,10UF,+/-20%,35V	417683	56289	199D106X0035DA2	8	
C 26, 36, 39,		417683				
C 49, 52		417683				
C 16, 29, 42,	CAP,TA,2.2UF,+/-20%,20V	161927	56289	199D225X0020BA2	4	
C 55		161927				
C 17, 30, 43,	CAP,CER,33PF,+/-2%,50V,C0G	354852	04222	SR211A330GAA	4	
C 56		354852				
C 18, 19, 31,	CAP,CER,1000PF,+/-20%,100V,X7R	402966	04222	SR151C102MAA	8	
C 32, 44, 45,		402966				
C 57, 58		402966				
C 20, 21, 33,	CAP,TA,5.6UF,+/-20%,25V	368969	56289	199D565X0025CA2	8	
C 34, 46, 47,		368969				
C 59, 60		368969				
CR 1- 5, 9-	DIODE,SI,BV=75V,IO=150MA,500MW	203323	09214	IN4448	20	
CR 13, 17- 21,		203323				
CR 25- 29		203323				
CR 7, 15, 23,	DIODE,SI,100 PIV,1.0 AMP	698555	04713	1N4002	4	
CR 31		698555				
CR 32- 35	DIODE,SI,20 PIV,1.0 AMP	507731	04713	MBR120P	4	
H 1	WASHER,FLAT,BRASS,#4,0.025	110775		COMMERCIAL	2	
H 3	CONN ACC,D-SUB,JACK SCREW,4-40	448092		COMMERCIAL	2	
J 20	CONN,D-SUB,PWB,RT ANGL,50 PIN,.590	501452	00779	206971-2	1	
MP 1	DECAL, ANALOG OUTPUT	762468	89536	762468	1	
MP 2	EJECTOR,PWB,NYLON	494724	32559	CP-66	2	
MP 3	HEAT DIS,SLEEVE,TO-5	380220	13103	1115B	4	
MP 13, 15, 17,	INSUL PART,TRANSISTOR MOUNT,DAP,TO-5	152207	07047	10123-DAP	4	
MP 19		152207				
Q 1, 2	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	04713	2N3906	2	
Q 3, 4	TRANSISTOR,SI,BV= 50V, 10W,TO-202	477331	04713	MPSU01A	2	
Q 5, 8- 11	TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	218396	04713	2N3904	5	
Q 6, 7	TRANSISTOR,SI,NPN,SMALL SIGNAL	330803	04713	MPS6560	2	
Q 12, 14, 16,	TRANSISTOR,SI,N-JFET,TO-92	271924	17856	J2750	4	
Q 18		271924				
Q 13, 15, 17,	TRANSISTOR,SI,NPN,SMALL SIGNAL	179374	04713	2N2218	4	
Q 19		179374				
R 1, 3	RES,CF,1K,+/-5%,0.25W	343426	59124	CF1/4 102J	2	
R 2, 5, 6,	RES,CF,10K,+/-5%,0.25W	348839	59124	CF1/4 102J	5	
R 11, 12		348839				
R 4	RES,CF,150K,+/-5%,0.25W	348938	59124	CF1/4 154J	1	
R 7, 8	RES,CF,43,+/-5%,0.25W	442244	59124	CF1/4 43R0J	2	
R 9, 10	RES,CF,200,+/-5%,0.25W	441451	59124	CF1/4 201J	2	
R 13- 15, 37-	RES,CF,150,+/-5%,0.25W	343442	59124	CF1/4 151J	12	
R 39, 61- 63,		343442				
R 85- 87		343442				
R 16, 40, 64,	RES,CF,2.2K,+/-5%,0.25W	343400	59124	CF1/4 222J	4	
R 88		343400				
R 17, 18, 41,	RES,CF,4.7K,+/-5%,0.25W	348821	59124	CF1/4 472J	8	
R 42, 65, 66,		348821				
R 89, 90		348821				
R 19, 43, 67,	RES,CF,47K,+/-5%,0.25W	348896	59124	CF1/4 473J	4	
R 91		348896				
R 20, 44, 68,	RES,CF,2.2M,+/-5%,0.25W	342659	59124	CF1/4 225J	4	
R 92		342659				
R 21, 45, 69,	RES,MF,7.68K,+/-1%,0.125W,100PPM	370999	91637	CMF-55 7681F T-1	4	
R 93		370999				
R 22, 46, 70,	RES,MF,32.4K,+/-1%,0.125W,100PPM	182956	91637	CMF-55 3242F T-1	4	
R 94		182956				
R 23, 47, 71,	RES,VAR,CERM,5K,+/-10%,0.5W	493593	80294	3299W-1-502	4	
R 95		493593				
R 24, 48, 72,	RES,MF,55.09K,+/-0.1%,0.125W,50PPM	404038	91637	CMF-55 5509B T-2	4	
R 96		404038				
R 25, 31, 49,	RES,VAR,CERM,25K,+/-10%,0.5W	500769	80294	3299W-1-253	8	
R 55, 73, 79,		500769				
R 97,103		500769				
R 26, 50, 74,	RES,MF,40K,+/-0.1%,0.125W,25PPM	321489	91637	CMF-55 4002B T-9	4	
R 98		321489				
R 27, 51, 75,	RES,MF,10K,+/-1%,0.125W,25PPM	328120	91637	CMF-55 1002F T-9	4	
R 99		328120				

Table 4-17. Option -011 Analog Output PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
R 28, 32, 52, R 56, 76, 80, R 100,104	RES,CC,10,+/-10%,0.125W	321125 321125 321125	01121	BB1001	8	
R 29, 30, 33, R 34, 53, 54, R 57, 58, 77, R 78, 81, 82, R 101,102,105, R 106	RES,CF,5.1K,+/-5%,0.25W	368712 368712 368712 368712 368712 368712	59124	CF1/4 512J	16	
R 35, 59, 83, R 107	RES,CC,51,+/-5%,0.125W	266262 266262	01121	BB5105	4	
R 36, 60, 84, R 108	RES WW 100 OHM	112151 112151	89536	112151	4	
S 1	SWITCH,DIP,DPST,PIANO,5 POS	454769	00779	1-435802-6	1	
T 1- 4	HIGH FREQ TRANSFORMER	531988	89536	531988	4	
TP 1, 10, 23- TP 27	TERM,FASTON,TAB,.110, SOLDER	512889 512889	00779	62395-1	7	
U 1, 2, 24	IC,CMOS,8-1 LINE MUX/DEMUX ANALOG SW	452805	04713	MC14051BCP	3	
U 3	IC,CMOS,PRSET BIN/DEC UP/DOWN COUNTER	452904	04713	MC14029BCP	1	
U 4, 26, 47, U 67	IC,VOLT REG,FIXED,+15 VOLTS,0.1 AMPS	453035 453035	01295	UA78L15ACLP	4	
U 5, 27, 48, U 68	IC,VOLT REG,FIXED,-15 VOLTS,0.1 AMPS	454801 454801	04713	MC79L15ACP	4	
U 7, 29, 50, U 70	IC,OP AMP,GENERAL PURPOSE,TO-78 CASE	413732 413732	04713	LM308N	4	
U 8- 10, 30- U 32, 51- 53, U 71- 73	IC,OP AMP,JFET INPUT,8 PIN DIP	525055 525055 525055	01295	LF355P	12	
U 11, 12, 22, U 23	IC, 4 X 4 ROM ,3-STATE OUT	524538 524538	01295	SN74LS670N	4	
U 13	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	04713	MC14027BCP	1	
U 14, 33, 54, U 79	ISOLATOR,OPTO,HI-SPEED,LED TO XSISTOR	407742 407742	28480	6N136	4	
U 15, 34, 55, U 80	ISOLATOR,OPTO,HI-SPEED,DUAL	429894 429894	28480	HCPL-2531	4	
U 16, 35, 56, U 81	IC,CMOS,DUAL D F/F,+EDG TRIG	340117 340117	04713	MC14013BCP	4	
U 17, 36, 57, U 82	IC,CMOS,QUAD 2 IN NAND W/SCHMT TRIG	404632 404632	04713	MC14093BCP	4	
U 18, 19, 37, U 38, 58, 59, U 83, 84	IC,CMOS,8BIT SHFT RGS W/3-ST&I/O LTCH	524520 524520 524520	04713	MC14094BCP	8	
U 20, 39, 60, U 85	IC,CMOS,12BIT DAC,12BIT ACCUR,CUR OUT	524512 524512	24355	AD7541KN	4	
U 21, 40, 61, U 86	IC,CMOS,QUAD BILATERAL SWITCH	605329 605329	04713	MC14016BCP	4	
U 25, 65	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LSOON	2	
U 41, 42	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	2	
U 43	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	1	
U 44	IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	412734	01295	SN74LS122N	1	
U 45	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	04713	MC14001BCP	1	
U 46, 66	IC,LSTTL,DUAL JK F/F,W/SEP CLKS&CLRS	393157	01295	SN74LS107AN	2	
U 62, 76	IC,LSTTL,OCTL INV LINE DRVR W/3-STATE	429480	01295	SN74LS240N	2	
U 63	IC,STTL,13 INPUT NAND GATE	495606	01295	SN74S133NA	1	
U 64, 75	IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N	2	
U 74	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	1	
U 77	IC,LSTTL,TRIPLE 3 INPUT NAND GATE	393074	01295	SN74LS10N	1	
U 78	IC,LSTTL,DUAL DIV BY 16 BINARY CNTR	483578	01295	SN74LS393N	1	
VR 6, 14, 22, VR 30	ZENER,COMP,6.4V,2%,2PPM,0.5MA	393579 393579	55801	DT-2006	4	
W 1	JUMPER,DIP,0.100CTR	416842	91506	8136-651P2	1	
W 2	SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	1	
Z 1, 2	RES,CERM,SIP,8 PIN,7 RES,10K,+/-2%	412924	91637	CSC08A-01-103G	2	
Z 3- 10	RES,CERM,SIP,8 PIN,7 RES,47K,+/-2%	413286	91637	CSC08A-01-473G	8	
NOTES:	† Static sensitive part.					



2400A-1609

Table 4-18. Option -012 Counter/Totalizer PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1	CAP,MICA,220PF,+/-5%,500V	170423	93790	CD15FD221J03	1	
C 2	CAP,CER,0.05UF,+/-20%,100V,Z5V	149161	60705	565CBA101AR503MA05	1	
C 3	CAP,CER,47PF,+/-2%,100V,C0G	512368	04222	SR151A470GAA	1	
C 4	CAP,CER,1UF,+/-20%,50V,Z5U	436782	04222	SR305E105MAA	1	
C 5, 6	CAP,CER,470PF,+/-20%,100V,X7R	358275	04222	SR151C471MAA	2	
C 7, 8	CAP,AL,10UF,+/-20%,35V	603985	62643	LL35T106M5X11FTV	2	
C 9	CAP,AL,47UF,+/-20%,35V	603977	62643	LL35T474M8X11FTV	1	
C 10- 52	CAP,CER,0.22UF,+/-20%,50V,Z5U	519157	04222	SR205E224MAT	43	
C 53	CAP,CER,5600PF,+/-5%,50V,C0G	528596	04222	SR215A562JAA	1	
CR 1- 8, 11- CR 14	‡ DIODE,SI,BV=75V,IO=150MA,500MW	203323	09214	IN4448	12	
MP 1	‡ EJECTOR,PWB,NYLON	203323				
MP 2	EJECTOR,PWB,NYLON	494724	32559	CP-66	2	
MP 3	INSUL PART,TRANSISTOR MOUNT,DAP,TO-5	152207	07047	10123-DAP	2	
Q 1, 2	DECAL,OPTION	762476	89536	762476	1	
R 1	‡ TRANSISTOR,SI,BV=300V,10W,TO-5	380071	04713	2N5416	2	
R 2, 12, 13	RES,CF,750,+/-5%,0.25W	441659	59124	CF1/4 751J	1	
R 3, 4	RES,CF,47K,+/-5%,0.25W	348896	59124	CF1/4 473J	3	
R 5, 22, 23, R 25	RES,CF,120,+/-5%,0.25W	442293	59124	CF1/4 121J	2	
R 6	RES,CF,910,+/-5%,0.25W	442335	59124	CF1/4 911J	4	
R 7	RES,CF,430K,+/-5%,0.25W	442483	59124	CF1-4 4303J	1	
R 8, 10	RES,CF,1.2M,+/-5%,0.25W	348995	59124	CF1/4 125J	1	
R 9, 11	RES,CF,91K,+/-5%,0.25W	441709	59124	CF1/4 913J	2	
R 14, 15	RES,CF,10K,+/-5%,0.25W	348839	59124	CF1/4 102J	2	
R 16	RES,CF,1M,+/-5%,0.25W	348987	59124	CF1/4 105J	2	
R 17	RES,CC,10M,+/-5%,0.25W	194944	01121	CB1065	1	
R 18	RES,CF,200K,+/-5%,0.25W	441485	59124	CF1/4 204J	1	
R 19	RES,CF,33K,+/-5%,0.25W	348888	59124	CF1/4 333J	1	
R 20	RES,CF,20K,+/-5%,0.25W	441477	59124	CF1/4 151J	1	
R 21	RES,CF,390,+/-5%,0.25W	441543	59124	CF1/4 391J	1	
S 1	RES,CF,6.2K,+/-5%,0.25W	442368	59124	CF1/4 622J	1	
S 2	SWITCH,DIP,SPDT,5 POS	417766	11236	206-125	1	
T 1	SWITCH,DIP,DPST,PIANO,5 POS	454769	00779	1-435802-6	1	
TP 1, 10, 60- TP 62, 66, 67, TP 70- 74, 76, TP 80- 83	INVERTER TRANSFORMER	521872	89536	521872	1	
U 1, 8, 9, U 15, 16, 23	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	17	
U 2, 4, 5	‡ IC,LSTTL,UP/DWN BINRY CNTR W/3-STATE	512889				
U 3, 37, 55, U 66	‡ IC,LSTTL,DUAL DIV BY 16 BINARY CNTR	512889				
U 6, 48	‡ IC,LSTTL,DUAL JK F/F,W/SEP CLKS&CLRS	512889				
U 7, 35	‡ IC,LSTTL,TRIPLE 3 INPUT NAND GATE	504498	7J696	AM25LS2569PC	6	
U 10, 25, 43, U 60	‡ IC,LSTTL,QUAD SET/RESET LATCH	504498				
U 11	‡ IC,TTL,QUAD 2 INPUT AND GATE	483578	01295	SN74LS393N	3	
U 12, 14, 49	‡ IC,LSTTL,QUAD 2 INPUT OR GATE	393157	01295	SN74LS107AN	4	
U 13, 42, 54	‡ IC,LSTTL,8-1 LINE MUX W/STROBE	393157				
U 17, 19, 41	‡ IC,LSTTL,QUAD 2 INPUT NAND GATE	393074	01295	SN74LS10N	2	
U 18	‡ IC,LSTTL,QUAD 2 INPUT AND GATE	404210	01295	SN74LS279AN	2	
U 20	‡ IC,LSTTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	4	
U 21	‡ IC,LSTTL,QUAD 2 INPUT OR GATE	393066				
	‡ IC,LSTTL,DUAL 4-1 LINE SELECT/MUX	393173	01295	SN74LS151N	1	
	‡ IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	3	
	‡ IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	3	
	‡ IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	3	
	‡ IC,LSTTL,DUAL 4-1 LINE SELECT/MUX	393181	01295	SN74LS153N	1	
	‡ IC,LSTTL,QUAD 2 INPUT XOR GATE	408237	01295	SN74LS86AN	1	
	‡ IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR	393215	01295	SN74LS175N	1	

List of Replaceable Parts
PARTS LISTS

Table 4-18. Option -012 Counter/Totalizer PCA (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
U 22, 29, 34	† IC,LSTTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	3	
U 24	† IC,LSTTL,DUAL 2-4 LINE DCDR/DRVR	393199	01295	SN74LS155AN	1	
U 26, 36	† IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	2	
U 27	† IC,CMOS,HEX CONTACT BOUNCE ELIMINATOR	536557	04713	MC14490VP	1	
U 28, 30, 40	† IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	3	
U 31	† IC,LSTTL,2 2-IN/3 3-IN AOI GATES	412981	01295	SN74LS51N	1	
U 32, 45	† IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	2	
U 33, 47, 58,	† IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	4	
U 63	†	429035				
U 38	† IC,TTL,HEX INVERTER W/OPEN COLLECTOR	407593	01295	SN7406N	1	
U 39, 46	† IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	2	
U 44	† IC,LSTTL,QUAD 2 INPUT NAND GATE	394205	01295	SN74LS03N	1	
U 50	† IC,STTL,QUAD 2 INPUT NAND GATE	363580	01295	SN74S00N	1	
U 51	† IC,COMPARATOR,8 PIN DIP	352195	27014	LM311N	1	
U 52	† ISOLATOR,OPTO,HI-SPEED,8 PIN DIP	354746	47379	6N135	1	
U 53	† IC,STTL,OCTAL DRIVER W/3-STATE OUTPUT	507277	18324	74S244N	1	
U 56	† IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74AN	1	
U 57	† IC,STTL,DUAL JK F/F,+EDG TRIG	363440	01295	SN74S112N	1	
U 59	† IC,STTL,13 INPUT NAND GATE	495606	01295	SN74S133NA	1	
U 61	† IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	01295	SN74LS11N	1	
U 62	† IC,STTL,HEX INVERTER	418004	18324	N74S04N	1	
U 64	† IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N	1	
U 65	† IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	404186	01295	SN74LS123N	1	
U 67	OSCILLATOR,10MHZ,TTL CLOCK	605535	91637	X0-43A10	1	
U 68	† IC,OP AMP,QUAD,JFET INPUT,14 PIN DIP	483438	01295	TL084CN	1	
U 69	† IC,OP AMP,DUAL,JFET INPUT,8 PIN DIP	454454	01295	TL082CP	1	
W 1	JUMPER,DIP,0.100CTR	416842	91506	8136-651P2	1	
XU 61, 62	SOCKET,SINGLE,PWB,FOR 0.012-0.022 PIN	376418	22526	75060-012	2	
Z 1	RES,CERM,DIP,16 PIN,15 RES,10K,+5%	355305	91637	MDP16-03-103J	1	
Z 2	RES,CERM,DIP,16 PIN,8 RES,51,+5%	501502	91637	MDP16-03-510J	1	
NOTES:	† Static sensitive part.					

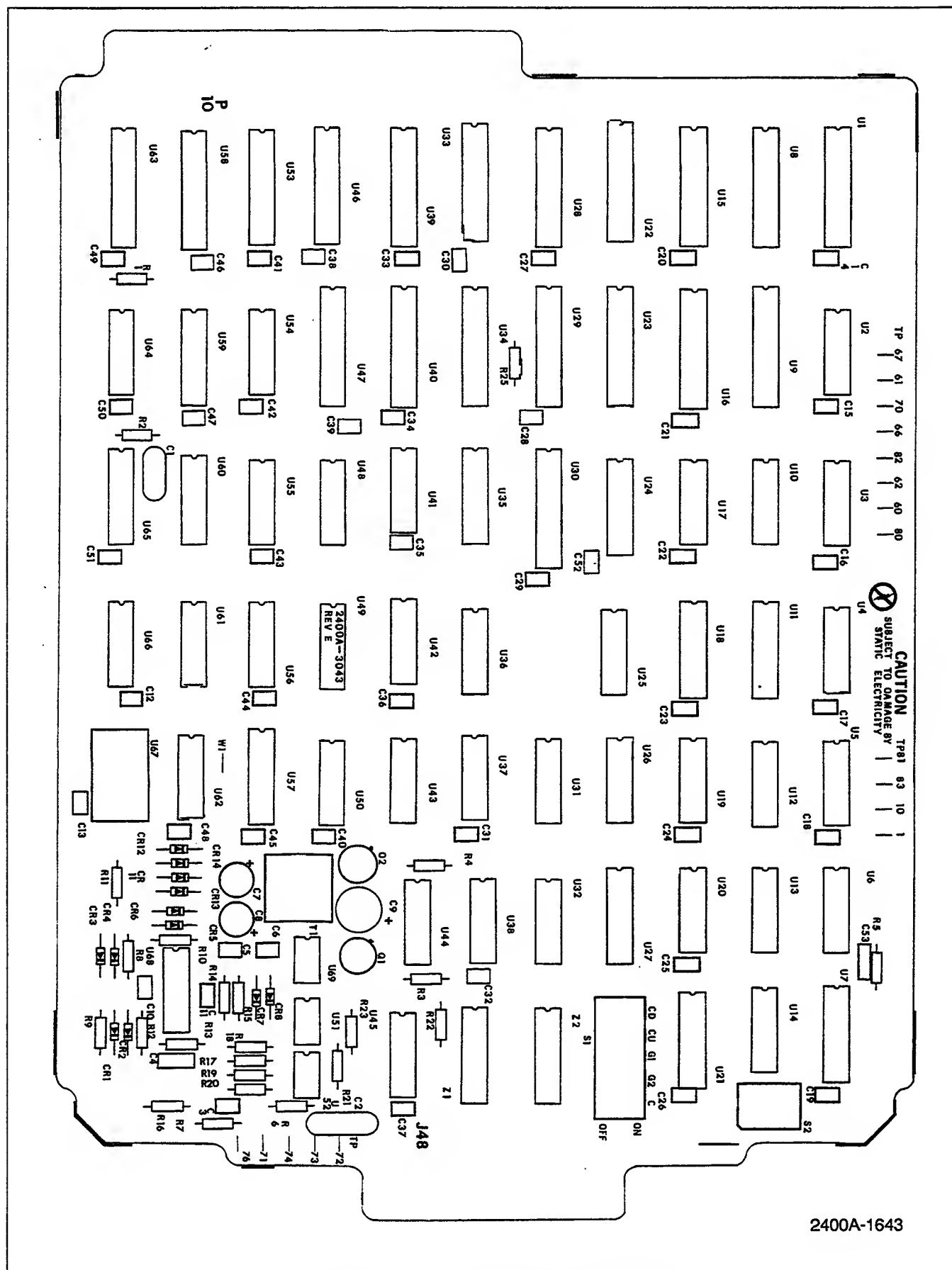


Figure 4-14. Option -012 Counter/Totalizer PCA

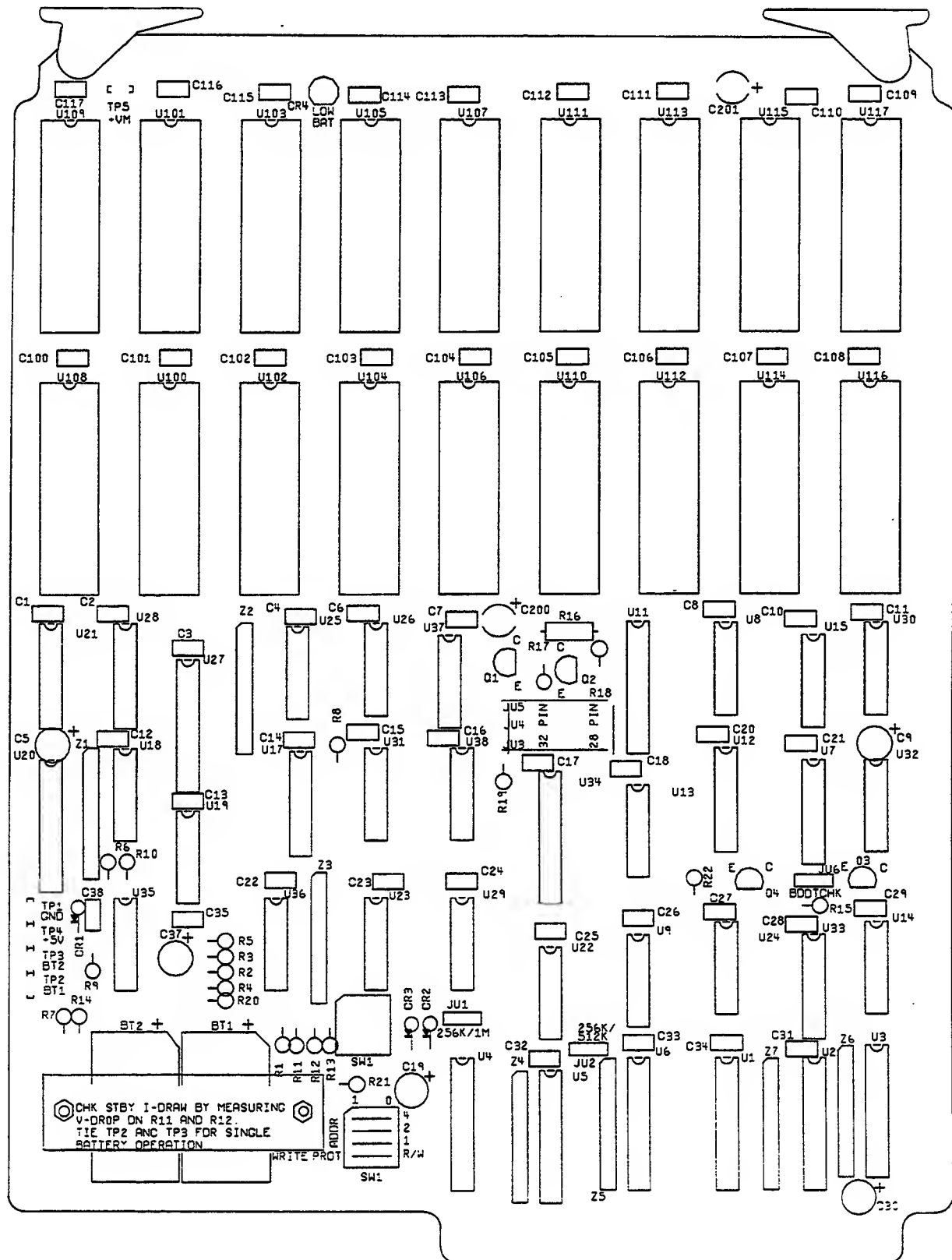
List of Replaceable Parts
PARTS LISTS

Table 4-19. Options -018(256K) -019(512K) -020(1M) Non-Volatile RAM PCA (Rev.A)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
BT 1, 2	BATTERY,LITHIUM,3.5V,0.75AH	782953	50120	LTC-7P	2	1
C 1- 4, 6-	CAP,CER,0.22UF,+20%,50V,Z5U	519157	04222	SR205E224MAT		
C 8, 10- 18,		519157				
C 20- 29, 31-		519157				
C 35,100-104,		519157				5
C 113-117		519157				
C 5, 9, 19,	CAP,TA,10UF,+20%,10V	176214	56289	199D106X0010EA2		
C 30, 37		176214				
C 38	CAP,CER,0.1UF,+20%,50V,Z5U	597575	04222	SR205E104MAA	1	2
C 200,201	CAP,TA,22UF,+20%,10V	658971	56289	199D226X0010CG2	2	
CR 1- 3	DIODE,SI,BV= 75.0V,RADIAL INSERTED	659516	81349	1N4448	3	
CR 4	LED,RED,PCB MOUNT,LUM INT= >0.6 MCD	385914	09214	SSL-22	1	
H 1	EJECTOR,PWB,NYLON	706879	30035	CE-110-062	2	3
H 2	SCREW,PH,P,SEMS,STL,4-40,.250	185918		COMMERCIAL	2	
JU 1- 5	WIRE,JUMPER,TEF,22AWG,WHT,.300	528257	60386	J.TEFLON .300		
MP 1	BRACKET, BATTERY	809814	89536	809814	1	
MP 2	OPTION DECAL		89536			1
MP 3	DECAL, BATTERY WARNING	843193	89536	843193		
Q 1	TRANSISTOR,SI,PNP,HI-SPEED SWITCH	331025	27014	S63735	1	
Q 2	TRANSISTOR,SI,NPN,SMALL SIGNAL,TO-92	218396	04713	2N3904	1	
R 1, 2, 5,	RES,CF,1M,+5%,0.25W	649970	59124	CF1/4 105J	5	1
R 13, 20		649970				
R 3	RES,CF,82K,+5%,0.25W	655027	59124	CF1/4 823J	1	
R 4	RES,CF,100K,+5%,0.25W	658963	59124	CF1/4 104J	1	
R 6	RES,CF,750K,+5%,0.25W	747543	59124	CF1/4 754J	1	5
R 7, 11, 12,	RES,CF,1K,+5%,0.25W	780585	59124	CF1/4 102J		
R 14, 21		780585				
R 8, 17	RES,CF,200,+5%,0.25W	810390	59124	CF1/4 201J	2	
R 9, 10, 18,	RES,CF,10K,+5%,0.25W	697102	59124	CF1/4 103J	4	1
R 19		697102				
R 16	RES,CC,68,+5%,0.5W	178384	01121	EB6805	1	
S 1	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
TP 1- 5	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	5	3
U 1- 3	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	3	
U 4	IC,ALSTTL,OCTL LINE DRVR W/3-STATE	741165	01295	SN74ALS244BN	1	
U 5, 6	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	2	
U 7	IC,LSTTL,2-4 LINE DEMUX	393165	01295	SN74LS139AN	1	1
U 8	IC,FTTL,HEX INVERTER	634444	04713	MC74F04N		
U 9	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	
U 11	IC,CMOS,NONVOLATILE CNTRLR/DECODER	820977	0B0A9	DS1211	1	
U 12	IC,ALSTTL,SYNC PRESET DECADE COUNTER	807834	01295	SN74ALS160BN	1	1
U 13	IC,CMOS,QUAD INPUT NOR GATE	851691	18324	74HCT02		
U 14	IC,ALSTTL,HEX INVERTER,DRIVER	807925	01295	SN74ALS1005N	1	
U 15	IC,FTTL,QUAD 2 INPUT OR GATE	659904	04713	MC74F32N	1	
U 17	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	1	5
U 18, 19, 25,	IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N		
U 26, 31		393272				
U 20, 27	IC,LSTTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	2	
U 21, 28	IC,LSTTL,8-1 MUX W/3-STATE OUTPUTS	407577	01295	SN74LS251N	2	2
U 22, 29	IC,FTTL,9 BIT PARITY GEN/CHECKER	707513	04713	MC74F280N		
U 23	IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	1	
U 24, 30	IC,ALS,DUAL D F/F,+EDG TRG,W/CLR	807842	01295	SN74ALS74AN	2	
U 32	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	1
U 33	IC,LSTTL,13 INPUT NAND GATE	586875	04713	SN74LS133N		
U 34	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	
U 35	IC,CMOS,TRIPLE 3 INPUT NOR GATE	355180	04713	MC14025BCP	1	
U 36	IC,COMPARATOR,QUAD,14 PIN DIP	387233	04713	LM339N	1	1
U 37	IC,CMOS,HEX INVERTERS	799924	18324	74HCT04N		
U 38	IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	1	
U 100-117	IC,CMOS,32K X 8 STATIC RAM,120 NSEC		89536			
XBT 1, 2	SOCKET,SINGLE,PWB,FOR 0.030-0.033 PIN	392944	00779	3-332070-0	2	4
XU 11	SOCKET,IC,20 PIN	454421	00779	2-640464-1	1	
Z 1- 5	RES,CERM,SIP,10 PIN,9 RES,2.2K,+2%	756734	91637	CSC10A-01-222G	5	
Z 6, 9	RES,CERM,SIP,10 PIN,9 RES,1K,+2%	448308	91637	CSC10A-01-102G	2	
NOTES:	1. Static sensitive part. 1. FOR OPTION -018 QTY = 41. FOR OPTION -019 QTY = 49. FOR OPTION -020 QTY = 41. 2. FOR OPTION -018 QTY = 5, JU1-5. FOR OPTION -019 QTY = 4, JU2-5. FOR OPTION -020 QTY = 4, JU1,JU3-5. 3. FOR OPTION -018 ORDER FLUKE STOCK NUMBER 809715. FOR OPTION -019 ORDER FLUKE STOCK NUMBER 809723. FOR OPTION -020 ORDER FLUKE STOCK NUMBER 843193. 4. FOR OPTION -018 ORDER FLUKE STOCK NUMBER 800995 QTY = 10, U100-109. FOR OPTION -019 ORDER FLUKE STOCK NUMBER 800995 QTY = 18, U100-117. FOR OPTION -020 ORDER FLUKE STOCK NUMBER 820985 QTY = 10, U100-109, 128K X 8.					

Table 4-20. Options -018(256K) -019(512K) Non-Volatile RAM PCA (Rev.0)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
BT 1	BATTERY,LITHIUM,3.5V,0.75AH	782953	50120	LTC-7P	1	
C 1- 4, 6-	CAP,CER,0.01UF,+20%,50V,Z5U	614214	04222	SR155E103MAT	30	
C 8, 10- 18,		614214				
C 20- 29, 31-		614214				
C 33, 35		614214				
C 5, 9, 19,	CAP,TA,10UF,+20%,10V	176214	56289	199D106X0010EA2	5	
C 30, 37		176214				
C 38,100-104,	CAP,CER,0.1UF,+20%,50V,Z5U	597575	04222	SR205E104MAA	1	
C 113-117		597575				
C 200,201	CAP,TA,22UF,+20%,10V	658971	56289	199D226X0010CG2	2	
D 1	DIODE,SI,100 PIV,1.0 AMP	698555	04713	1N4002	1	
H 1	WASHER,FLAT,BRASS,#4,0.025	110775		COMMERCIAL	2	
H 2	SCREW,PH,P,SEMS,STL,4-40,.500	353060		COMMERCIAL	2	
MP 1	BRACKET, BATTERY	809814	89536	809814	1	
MP 2	OPTION DECAL		89536		1	2
MP 3	DECAL, BATTERY WARNING	843193	89536	843193	1	
Q 1	TRANSISTOR,SI,PNP,HI-SPEED SWITCH	331025	27014	S63735	1	
R 1, 2, 5	RES,CF,1M,+5%,0.25W	348987	59124	CF1/4 105J	3	
R 3	RES,CF,82K,+5%,0.25W	348912	59124	CF1/4 823J	1	
R 4	RES,CF,100K,+5%,0.25W	348920	59124	CF1/4 104J	1	
R 6	RES,CF,470K,+5%,0.25W	342634	59124	CF1/4 474J	1	
R 8	RES,CF,1K,+5%,0.25W	343426	59124	CF1/4 102J	1	
R 10	RES,CF,10K,+5%,0.25W	348839	59124	CF1/4 102J	1	
RN 1- 5, 8	RES,CERM,SIP,10 PIN,9 RES,2.2K,+2%	756734	91637	CSC10A-01-222G	6	
RN 6, 7	RES,CERM,SIP,10 PIN,9 RES,1K,+2%	448308	91637	CSC10A-01-102G	2	
S 1	SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1	
U 1- 3	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	3	
U 4	IC,ALSTTL,OCTL LINE DRVR W/3-STATE	741165	01295	SN74ALS244BN	1	
U 5, 6	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	2	
U 7	IC,SELECTED 74LS139	843214	89536	843214	1	
U 8	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	
U 9	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	
U 11, 17	IC,SELECTED 74LS138	843206	89536	843206	2	
U 12	IC,ALSTTL,SYNC PRESET DECADE COUNTER	807834	01295	SN74ALS160BN	1	
U 13, 23	IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	2	
U 14	IC,ALSTTL,HEX INVERTER,DRIVER	807925	01295	SN74ALS1005N	1	
U 15	IC,FTTL,QUAD 2 INPUT OR GATE	659904	04713	MC74F32N	1	
U 16	IC,CMOS,BATTERY BACK-UP SWITCH	808006	34371	ICL7673CPA	1	
U 18, 19, 25,	IC,LSTTL,QUAD 2 IN XNOR GATE W/OPN CL	393272	01295	SN74LS266N	5	
U 26, 31		393272				
U 20, 27	IC,LSTTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	2	
U 21, 28	IC,LSTTL,8-1 MUX W/3-STATE OUTPUTS	407577	01295	SN74LS251N	2	
U 22, 29	IC,FTTL,9 BIT PARITY GEN/CHECKER	707513	04713	MC74F280N	2	
U 24, 30	IC,ALS,DUAL D F/F,+EDG TRG,W/CLR	807842	01295	SN74ALS74AN	2	
U 32	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	
U 33	IC,LSTTL,13 INPUT NAND GATE	586875	04713	SN74LS133N	1	
U 34	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	
U 35	IC,CMOS,TRIPLE 3 INPUT NOR GATE	355180	04713	MC14025BCP	1	
U 36	IC,COMPARATOR,8 PIN DIP	352195	27014	LM311N	1	
U 100-117	IC,CMOS,32K X 8 STATIC RAM,120 NSEC	800995	12581	HM62256LP-12	1	3
XU 11	SOCKET,IC,16 PIN	276535	00779	2-640358-1	1	
NOTES:	‡ Static sensitive part. 1. FOR OPTION -018 QTY = 11. FOR OPTION -019 QTY = 19, C38,C100-117. 2. FOR OPTION -018 ORDER FLUKE STOCK NUMBER 809715. FOR OPTION -019 ORDER FLUKE STOCK NUMBER 809723. 3. FOR OPTION -018 QTY = 10, U100-109. FOR OPTION -019 QTY = 18.					



17XXA-1618-PH2

Table 4-21. Option 1722A-440 Winchester Hard Disk, 40M

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
H 1	SCREW,FHU,P,LOCK,SS,6-32,.250	320093	74594	320093	8	
MP 1	17XXA HARD DISK,SVC REPL	862578	89536	862578	1	1
MP 1	17XXA HARD DISK,SVC REPL	880000	89536	880000	1	2
MP 1	17XXA HARD DISK,SVC REPL	923912	89536	923912	1	3
MP 3	HARD DRIVE SHIELD,FINISHED	862615	89536	862615	1	
MP 4	17XXA WINCHESTER,I/F SVC RQMT	848890	89536	848890	1	
MP 5	DECAL, 40 MEG WINCHESTER	848973	89536	848973	1	
U 68, 81	4 BOOT PROM SET, VER 2.X	805143	89536	805143	1	4
W 1	CABLE ASSEMBLY, HARD DISK	862581	89536	862581	1	
W 2	CABLE,POWER	644120	89536	644120	1	
W 3	LED CABLE ASSY	862610	89536	862610	1	
NOTES:	4 Static sensitive part. 1. FOR FDOS AND BOOT V2.0 OR GREATER. 2. FOR FDOS AND BOOT V2.1 OR GREATER. 3. FOR FDOS AND BOOT V2.2 OR GREATER. 4. SEE A4 IN SECTION 4 FOR PARTS BREAKDOWN AND LOCATION.					

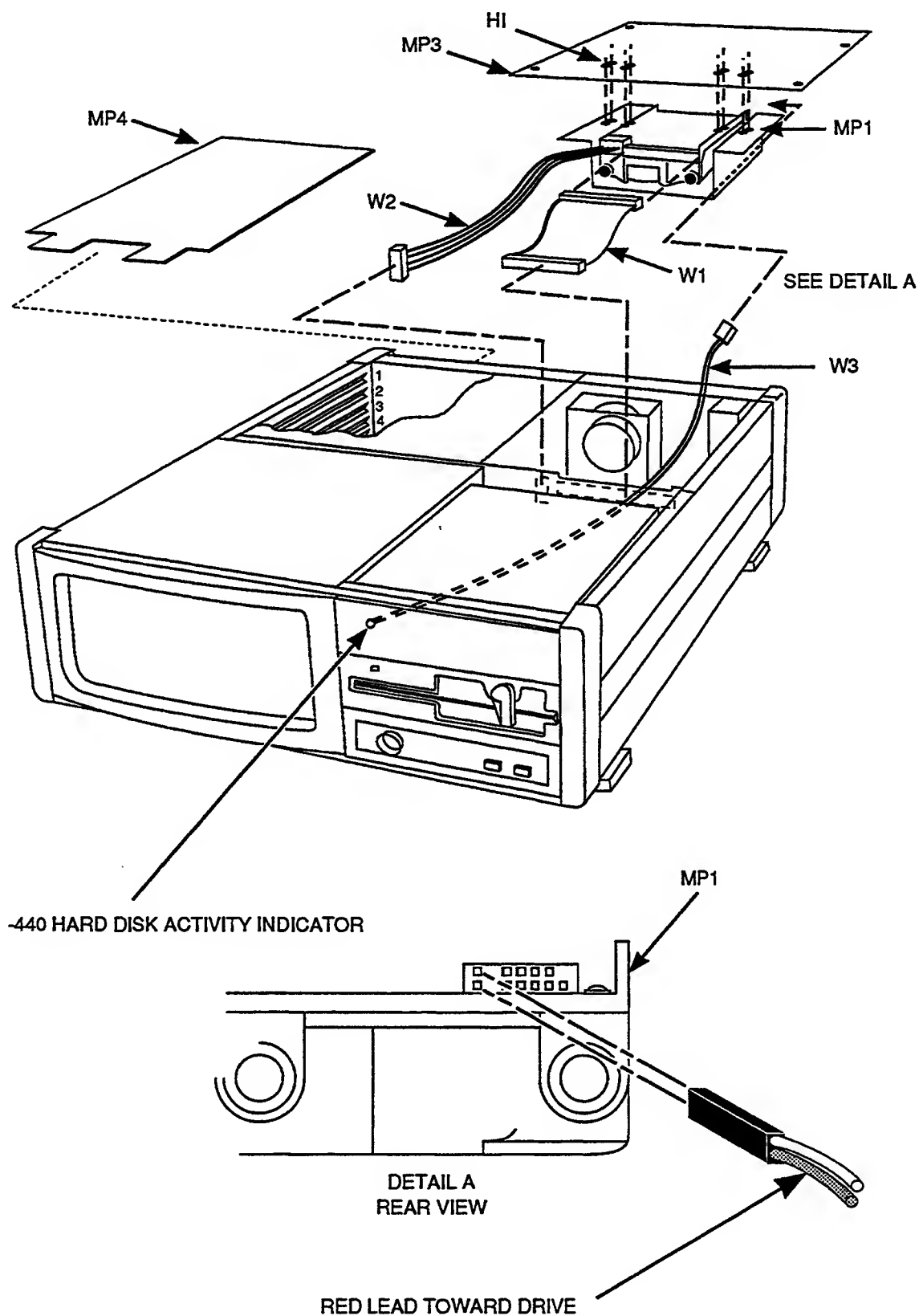
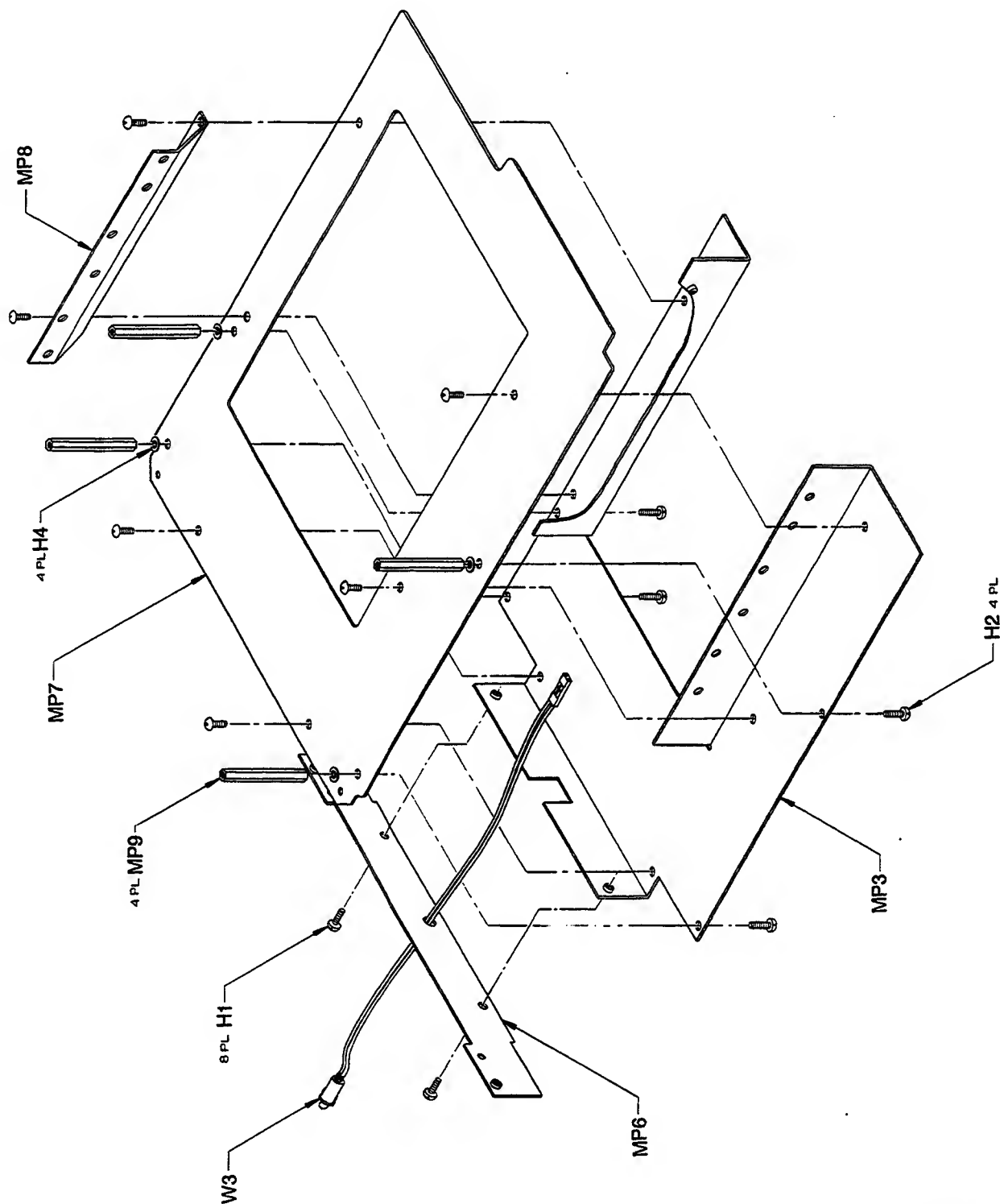


Table 4-22. Option 1711A/AA-440 Winchester Hard Disk, 40M

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
H 1	SCREW,PH,P,SEMS,STL,6-32,.250	178533		COMMERCIAL	8	
H 2	SCREW,PH,P,SEMS,STL,6-32,.375	177022		COMMERCIAL	11	
H 3	SCREW,PH,P,LOCK,SS,6-32,.437	362954	89536	362954	3	
H 4	WASHER,FLAT,BRASS,#6,0.028 THK	111310		COMMERCIAL	7	
MP 1	17XXA HARD DISK, SVC REPL	862578	89536	862578	1	1
MP 1	17XXA HARD DISK, SVC REPL	880000	89536	880000	1	2
MP 1	17XXA HARD DISK, SVS REPL	923912	89536	923912	1	3
MP 3	HARD DRIVE BRACKET	868526	89536	868526	1	
MP 4	17XXA WINCHESTER,I/F SVC RQMT	848890	89536	848890	1	
MP 5	DECAL, 40 MEG WINCHESTER	848973	89536	848973	1	
MP 6	FILLER PANEL, NARROW	868484	89536	868484	1	
MP 7	HARD DRIVE FRAME	868521	89536	868521	1	
MP 8	HARD DRIVE SUPPORT BRACKET	868562	89536	868562	1	
MP 9	SPACER,.250 HEX,AL,6-32,1.500	442640	89536	442640	4	
U 68, 81	† BOOT PROM SET, VER 2.1	805143	89536	805143	2	4
W 1	CABLE ASSEMBLY, HARD DISK	862581	89536	862581	1	
W 2	CABLE,POWER	644120	89536	644120	1	
W 3	LED,CABLE ASSY.	862672	89536	862672	1	
NOTES:		† Static sensitive part. 1. FOR FDOS AND BOOT V2.0 OR GREATER. 2. FOR FDOS AND BOOT V2.1 OR GREATER. 3. FOR FDOS AND BOOT V2.2 OR GREATER. 4. SEE A4 IN SECTION 4 FOR PARTS BREAKDOWN AND LOCATION.				



1711A/AA-440
(1 of 2)

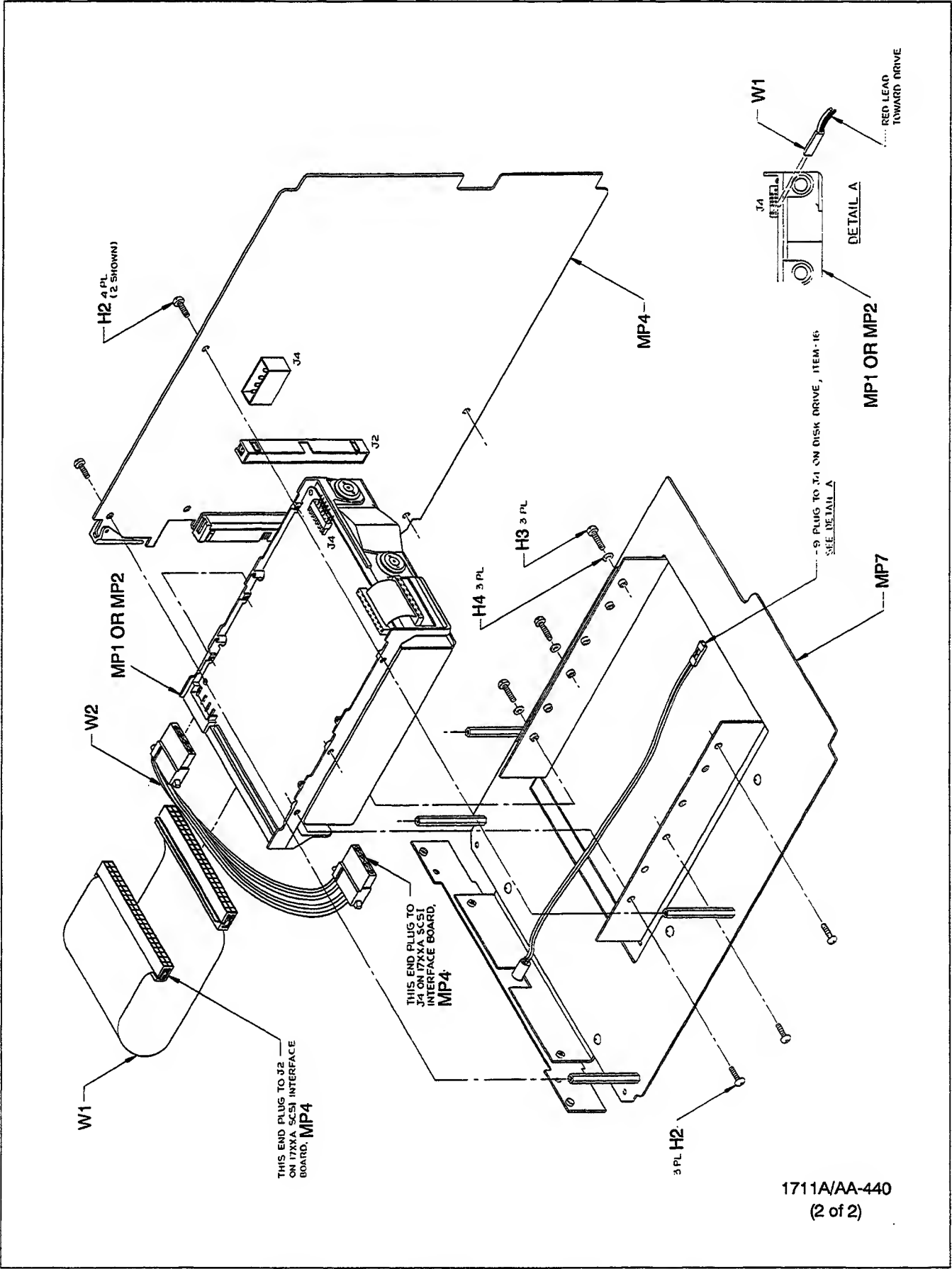


Figure 4-16. Option 1711A/AA-440 Hard Disk, 40M (cont)

MANUFACTURER'S FEDERAL SUPPLY CODES

00779 AMP, Inc. Harrisburg, PA	06V52 Schaffner EMC Inc. Union, NJ	24347 Penn Engineering Co. S. El Monte, CA	Melbourne, FL
01121 Allen-Bradley Co. Milwaukee, WI	0J4G8 Panasonic Industrial Co. Electronic Components Div. Secaucus, NJ	24355 Analog Devices Inc. Norwood, MA	34576 Rockwell International Corp. Digital Communications Div. Newport Beach, CA
01295 Texas Instruments Inc. Semiconductor Group Dallas, TX	0MS63 Quality Technologies Corp Sunnyvale, CA	25099 Cascade Gasket & Mfg. Co. Inc. Kent, WA	34641 Instrument Specialties Co., Inc. Eufless, TX
01537 Champion Technologies Inc. Formerly Motorola Communications & Electronics Inc. Franklin Park, IL	11236 CTS Corp. Berne Div. Thick Film Products Group Berne, IN	27014 National Semiconductor Corp. Santa Clara, CA	37942 Mallory Capacitor Corp. Sub of Emhart Industries Inc. Indianapolis, IN
04221 Midland-Ross Corp. Midtex Div. N. Mankato, MN	11503 Keystone Columbia Inc. Freemont, IN	27264 Molex Inc. Lisle, IL	47379 ISOCOM Campbell, CA
04222 AVX Corp. AVX Ceramics Div. Myrtle Beach, SC	11961 Semicon Inc. Burlington, MA	28213 Minnesota Mining & Mfg. Co. Consumer Specialties Div. 3M Center Saint Paul, MN	49569 IDT (International Development & Trade) Dallas, TX
04713 Motorola Inc. Semiconductor Products Sector Phoenix, AZ	12040 National Semiconductor Corp. Danbury, CT	28480 Hewlett-Packard Co. Corporate H2 Palo Alto, CA	4U402 Roederstein Electronics Inc. Statesville, NC
04946 Standard Wire and Cable Rancho Dominguez, CA	12581 Hitachi Metals International Ltd. Hitachi Magna-Lock Div. Big Rapids, MI	28520 Heyco Molded Products Kenilworth, NJ	50120 Eagle-Picher Industries Inc. Electronics Div., Couples Dept. Colorado Springs, CO
05245 Corcom Inc. Libertyville, IL	12969 Unitrode Corp. Lexington, MA	2K262 Boyd Corp. Portland, OR	51406 Murata Erie, No. America Inc. Symma, GA
05347 Ultronix Inc (Tel Labs) Grand Junction, CO	13103 Thermalloy Co., Inc. Dallas, TX	2M021 EFAB Mfg. Inc. Charlottesville, VA	53184 Xclton Corp. Latham, NY
06383 Panduit Corp. Tinley Park, IL	13919 Burr-Brown Corp. Tucson, AZ	30035 Jolo Industries Inc. Garden Grove, CA	53848 Standard Microsystems Corp. Hauppauge, NY
07047 Ross Milton Co., The Southampton, PA	14936 General Instrument Corp. Power Semiconductor Div. Hicksville, NY	31522 Metal Masters Inc. Guntown, MS	55224 SMK Electronics Placentia, CA
07263 Fairchild Semiconductor North American Sales Cupertino, CA	17856 Siliconix Inc. Santa Clara, CA	31918 ITT-Schadow Eden Prairie, MN	55285 Bercquist Co. Inc., The Minneapolis, MN
08718 ITT Cannon Electric Phoenix Div. Phoenix, AZ	18324 Signetics Corp. Military Products Div. Orem, UT	32559 Bivar, Inc. Irvine, CA	55566 R A F Electronic Hardware Inc. Seymour, CT
09214 General Electric Co. Semiconductor Products Dept. Auburn, NY	19451 Perine Machinery & Supply Co. Kent, WA	32997 Bourns Inc. Trimpot Div. Riverside, CA	55801 Compensated Devices, Inc. Melrose, MA
0B0A9 Dallas Semiconductor corp Dallas, TX	22526 DuPont, El DeNemours & Co. Inc. DuPont Electronic Dept. New Cumberland, PA	33297 NEC Electronics USA Inc. Electronic Arrays Inc. Div. Mountain View, CA	56289 Sprague Electric Co. Nashua, NH
0CXF1 Dataray Systems Oklahoma City, OK	22670 GM Nameplate, Inc. Seattle, WA	34114 Oak Industries Rancho Bernardo, CA	56524 Atlas Supply Inc. Formerly Atlas Packing & Rubber Seattle, WA
	23880 Stanford Applied Engineering Inc.(SAE) Santa Clara, CA	34335 Advanced Micro Devices (AMD) Sunnyvale, CA	59124 KOA-Speer Electronics Inc. Bradford, PA
		34371 Harris Corp. Harris Semiconductor Products Group	59660 Tucson Inc. Tucson, AZ

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5W664
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Div. of Nihon Dempa Kogyo LTD
Lynchburg, VA

60386
Squires Electronics Inc.
Cornelius, OR

60705
Cera-Mite Corp.
(formerly Sprague)
Grafton, WI

61429
Fox Electronics
Fort Myers, FL

61935
Schurter Inc.
Petaluma, CA

62643
United Chemi-con Inc.
Rosemont, IL

66891
BKC International Electronics Inc.
Lawrence, MA

68630
Tadiran Electronics Industries Inc.
New York, NY

68919
Inter-Technical Group Inc., The
Irvington, NY

6W060
Unbrako Ltd.
Leicester, England

70485
Atlantic India Rubber Co., Inc.
Goshen, IN

70903
Cooper Belden Electronic Wire & Cable
Geneva, IL

71400
Bussman
Div. of Cooper Industries Inc.
St. Louis, MO

72962
Elastic Stop Nut
Div. of Harvard Industries
Union, NJ

73734
Federal Screw Products Inc.
Chicago, IL

74445
Holo-Krome Co.
Elmwood, CT

74594
Component Resources Inc.
Div of EPI International Corp.
Beaverton, OR

74868
Amphenol Corp.
Danbury, CT

78189
Illinois Tool Works Inc.
Shakeproof Div.
Elgin, IL

79727
C - W Industries
Southampton, PA

79963
Zierick Mfg. Corp.
Mount Kisco, NY

7J696
AMD Plastics, Inc.
Eastlake, OH

80294
Bourms Instruments Inc.
Riverside, CA

81349
U.S. Government

82277
Intervox Corp.
Seattle, WA

82389
Switchcraft Inc.
Sub of Raytheon
Chicago, IL

83330
Dialight Corp.
Manasquan Div.
Manasquan, NJ
Formerly Kulka Smith, Inc.

83478
Rubbercraft Corp. of America, Inc.
West Haven, CT

84411
American Shizuki Corp.
Ogallala opns
Ogallala, NE

85480
W H Brady Co. Corp.
Industrial Products Div
Milwaukee, WI

86928
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87516
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Kansas City, KS

88245
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91833
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Cornell Dubilier Electronics
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97197
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Barrington, NJ

S3385
Sanken Electric
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c/o L-Squared
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Montevideo
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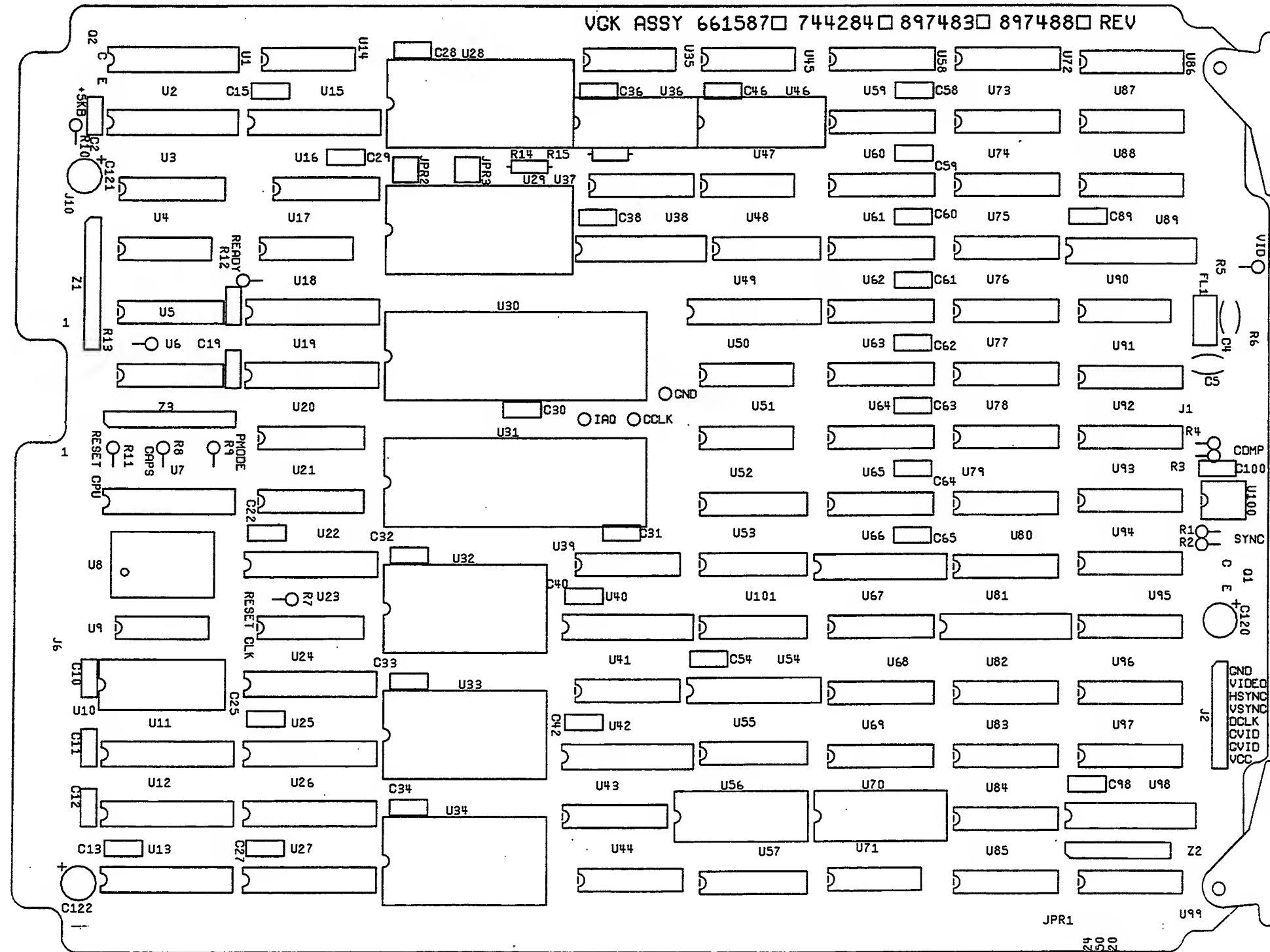
Coasin C.A.
Calle 9 Con Calle 4, Edif. Edinurbi
Apartado de Correos Nr-70-136
Los Ruices
Caracas 1070-A
TEL: 58 2 241-0309, 241-1248
TLX: (395) 21027 EMVEN VC

Section 5

Schematic Diagrams

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1722A-1601

Figure 5-1. A1 Video/Graphics/Keyboard (VGK) Interface Module

Schematic Diagrams

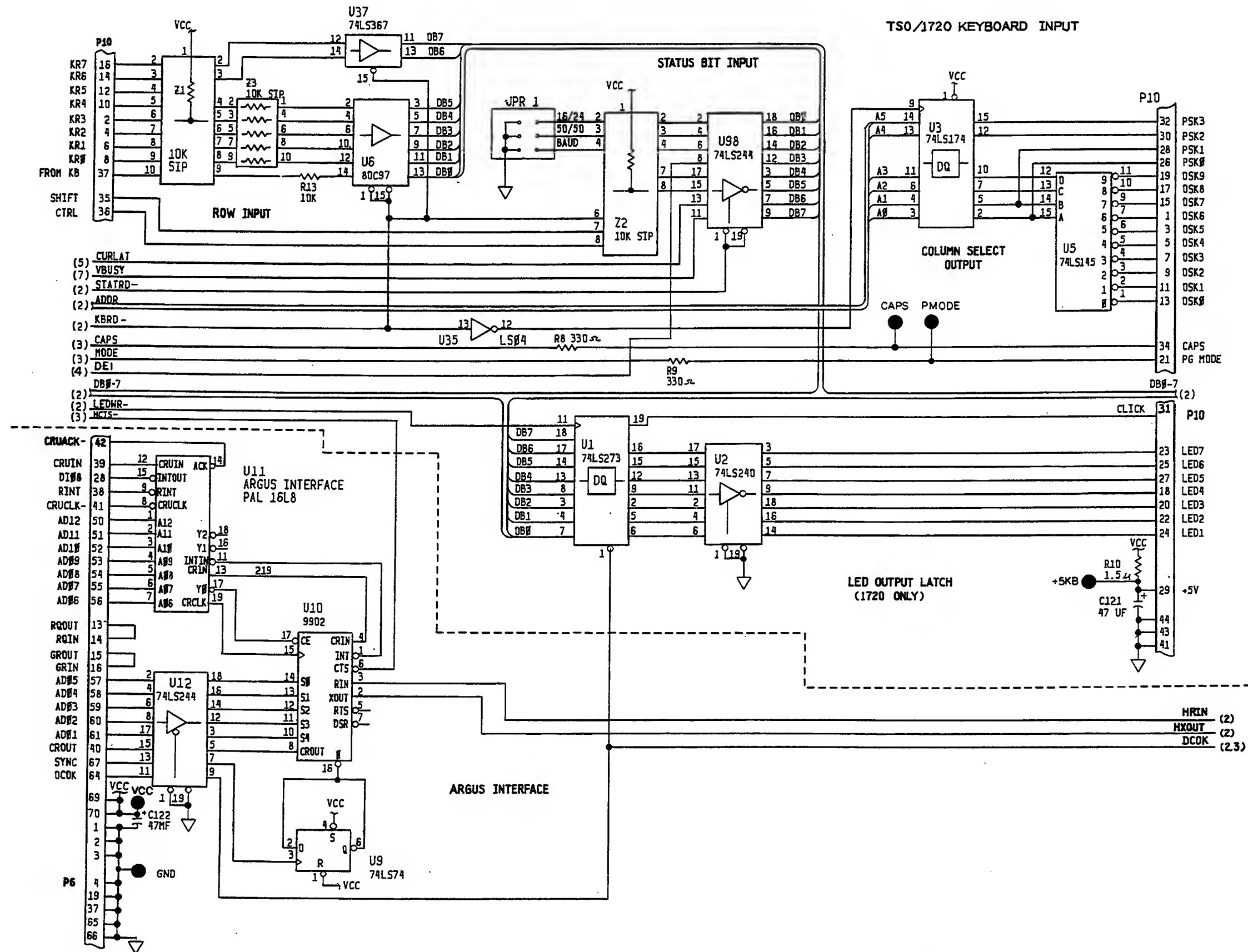
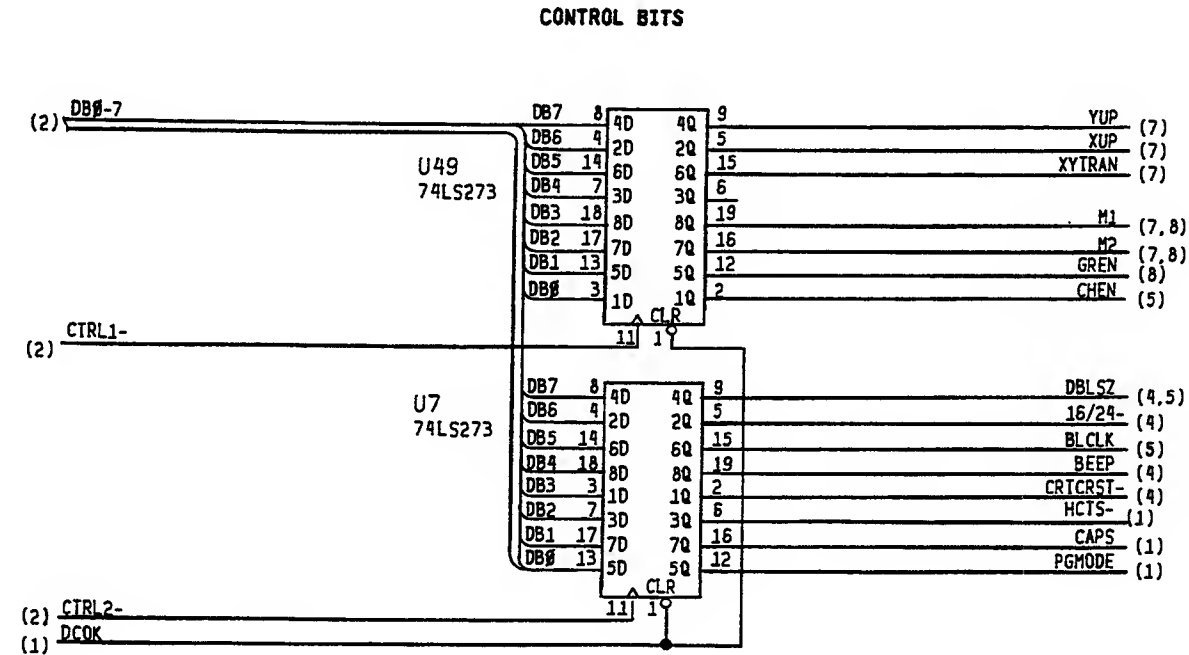


Figure 5-1. A1 Video/Graphics/Keyboard (VGK) Interface Module (cont)





- NOTES: UNLESS OTHERWISE SPECIFIED
1. +5V AND GND ARE NOT SHOWN EXPLICITLY FOR MOST CHIPS; UPPER LEFT HAND PIN (14,16,20...) IS ASSUMED TO BE +5V. LOWER RIGHT HAND PIN (7,8,9...) IS ASSUMED TO BE GROUND. OTHER SUPPLY VOLTAGES ARE SHOWN EXPLICITLY.
 2. ALL RESISTANCE IS IN OHMS.
 3. ALL CAPACITANCE IS IN MICROFARADS.
 4. NEGATIVE ASSERTION SIGNALS (SIGNAL) ARE LABELED AS SIGNAL-.

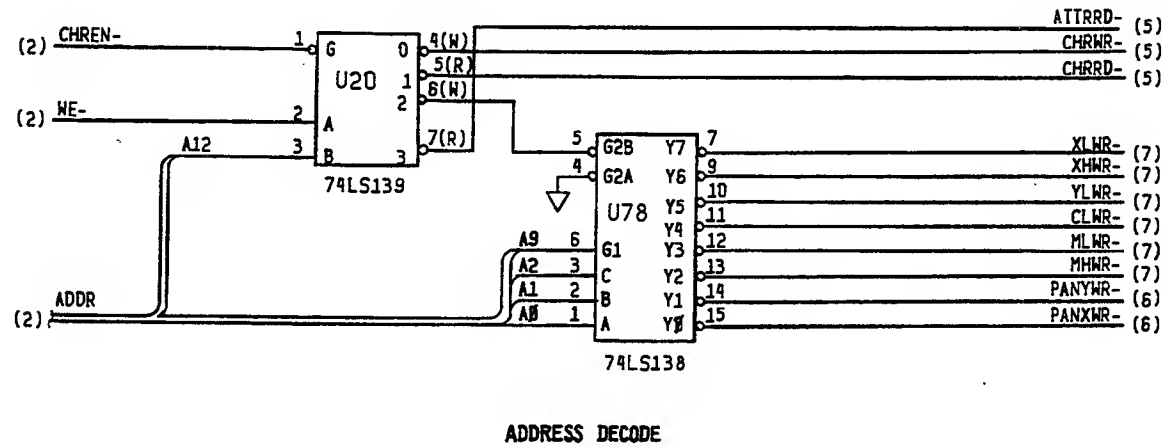
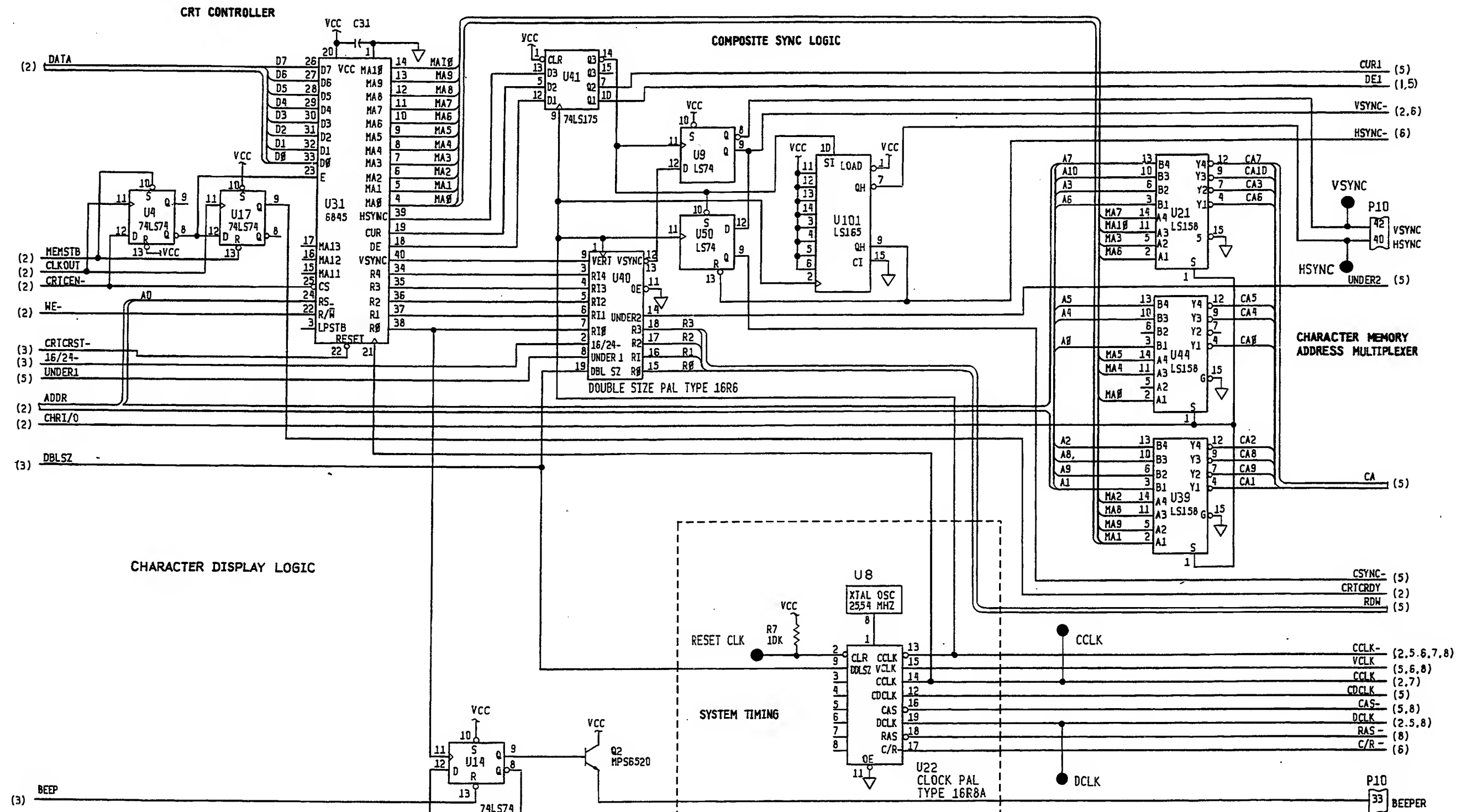


Figure 5-1. A1 Video/Graphics/Keyboard (VGK)
Interface Module (cont)



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Figure 5-1. A1 Video/Graphics/Keyboard (VGK)
Interface Module (cont)

Schematic Diagrams

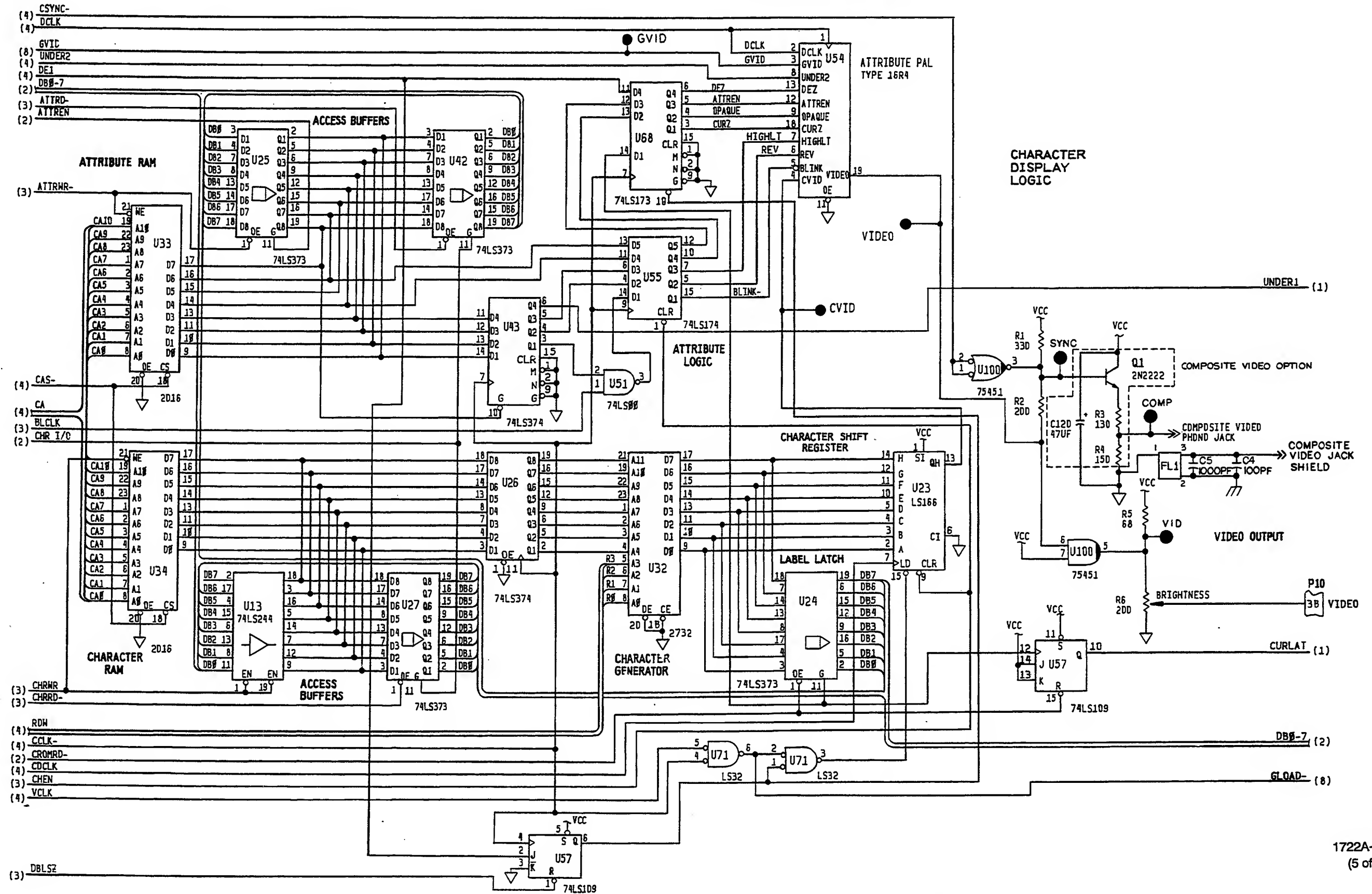


Figure 5-1. A1 Video/Graphics/Keyboard (VGK) Interface Module (cont)

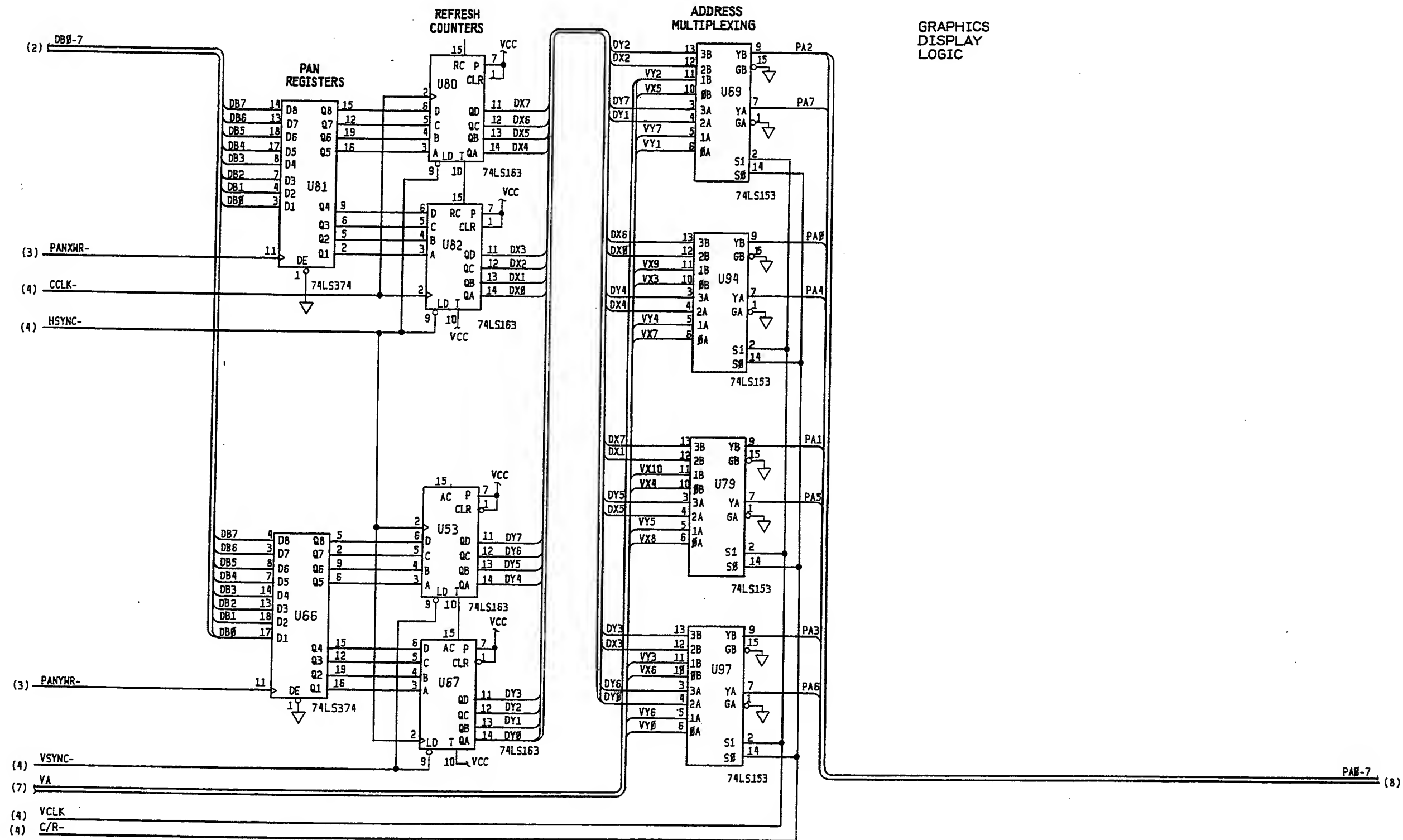
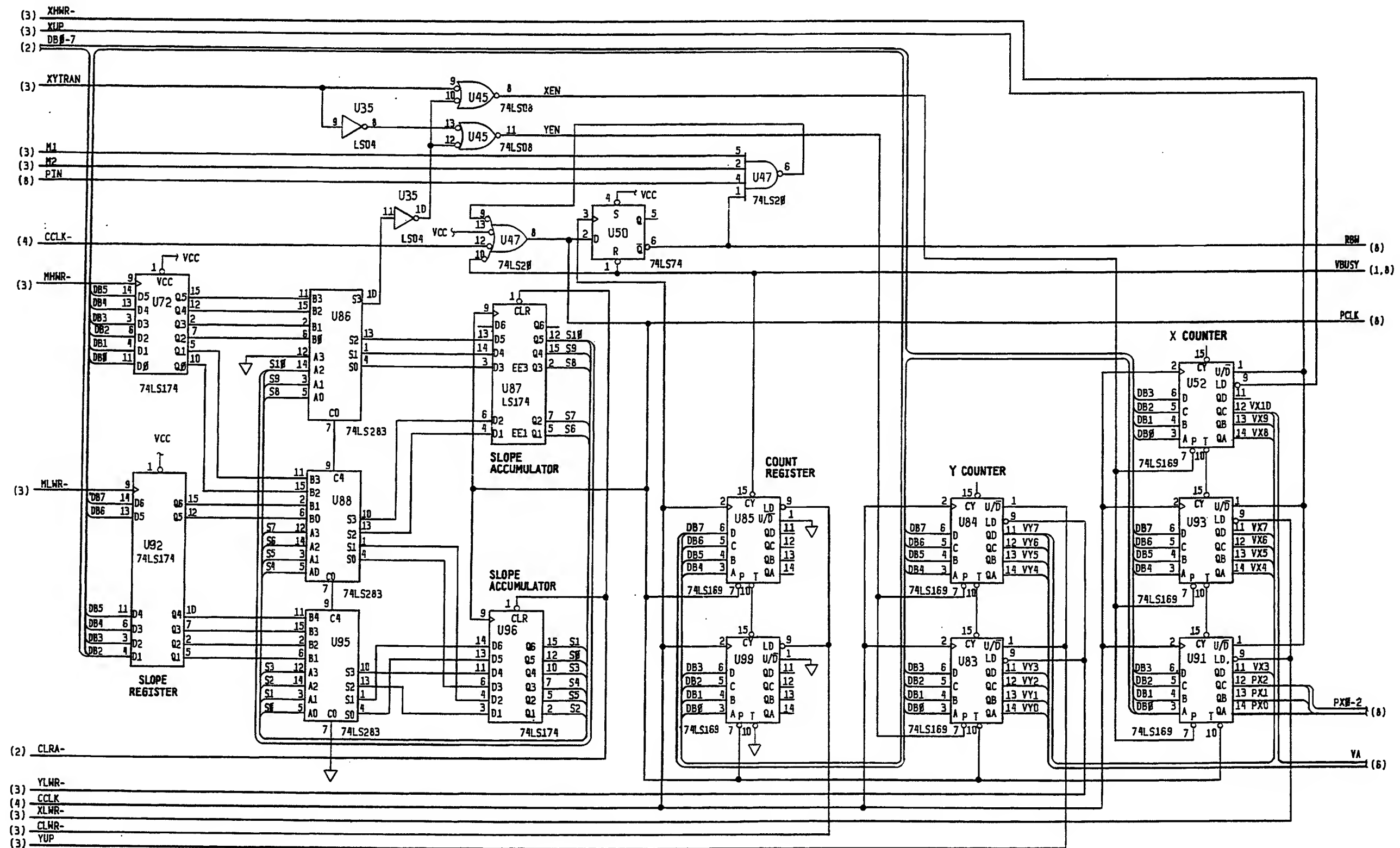


Figure 5-1. A1 Video/Graphics/Keyboard (VGK) Interface Module (cont)

Schematic Diagrams



VECTOR GENERATOR LOGIC

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(7 of 8)

Figure 5-1. A1 Video/Graphics/Keyboard (VGK)
Interface Module (cont)

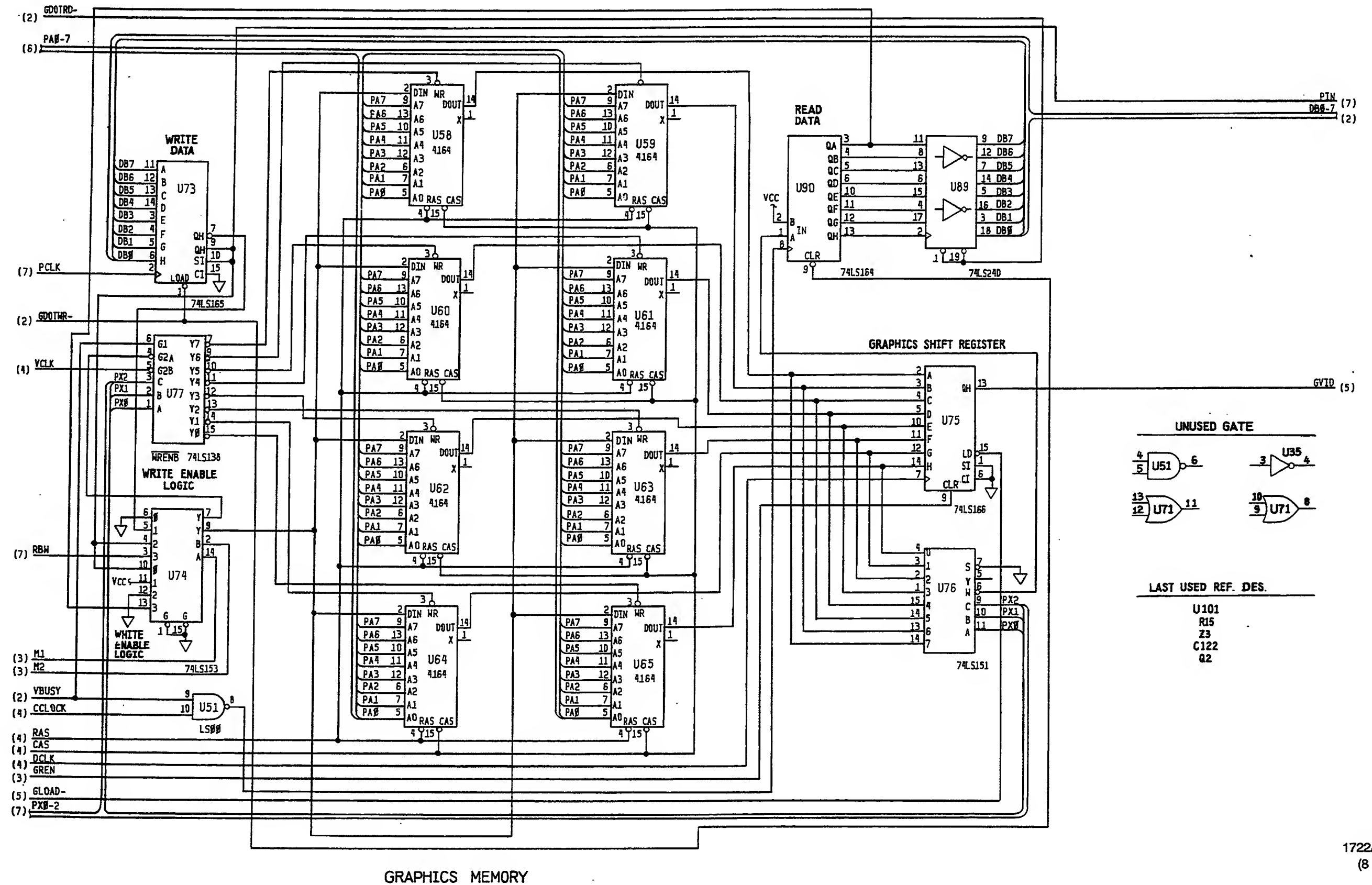
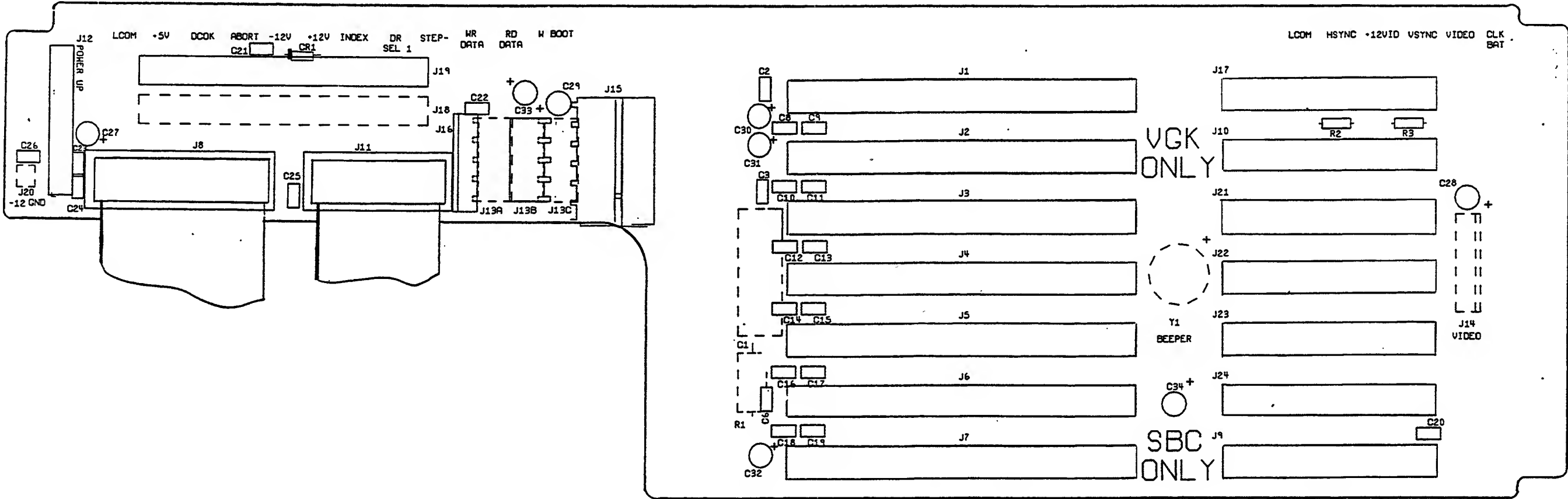


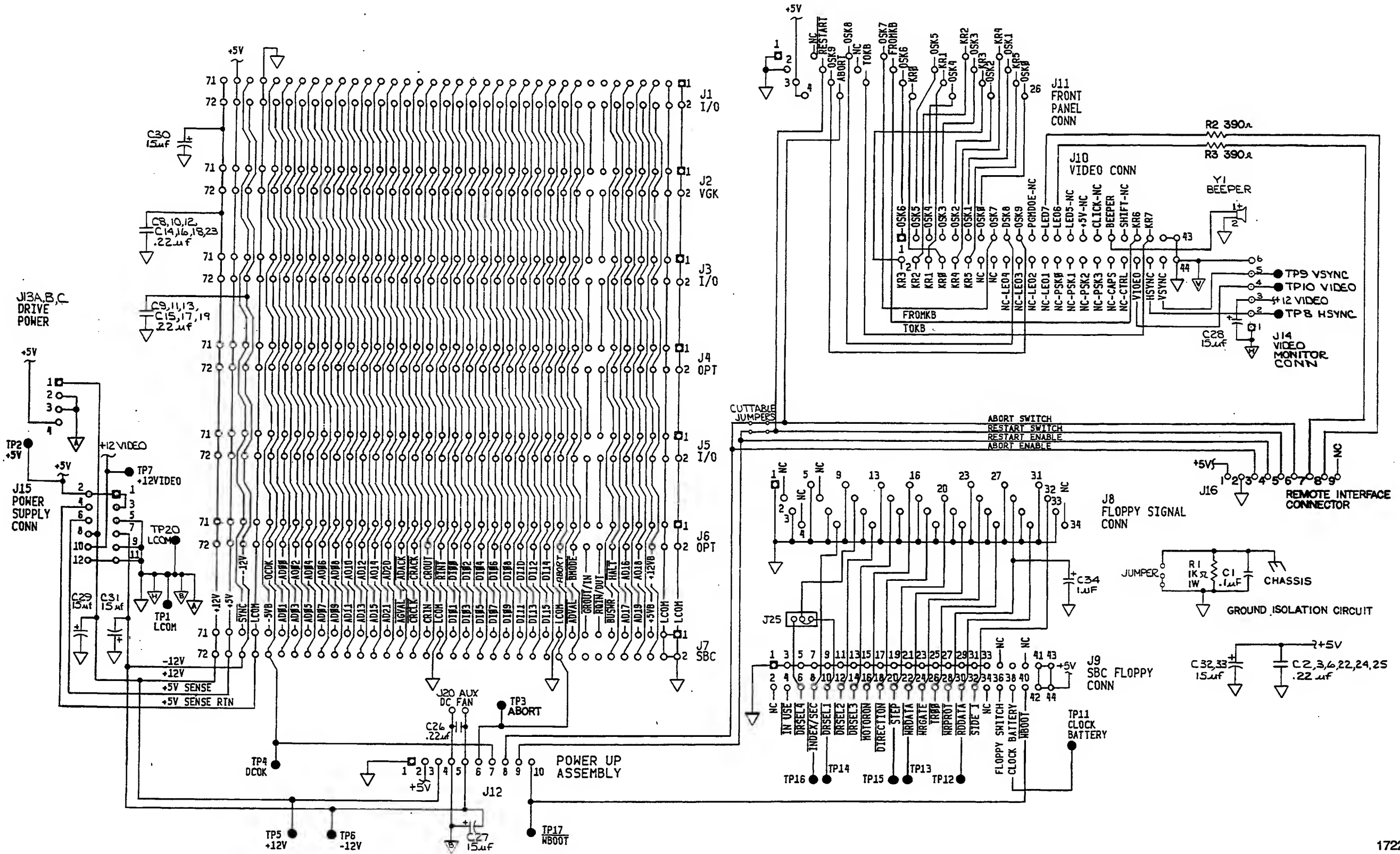
Figure 5-1. A1 Video/Graphics/Keyboard (VGK) Interface Module (cont)

Schematic Diagrams



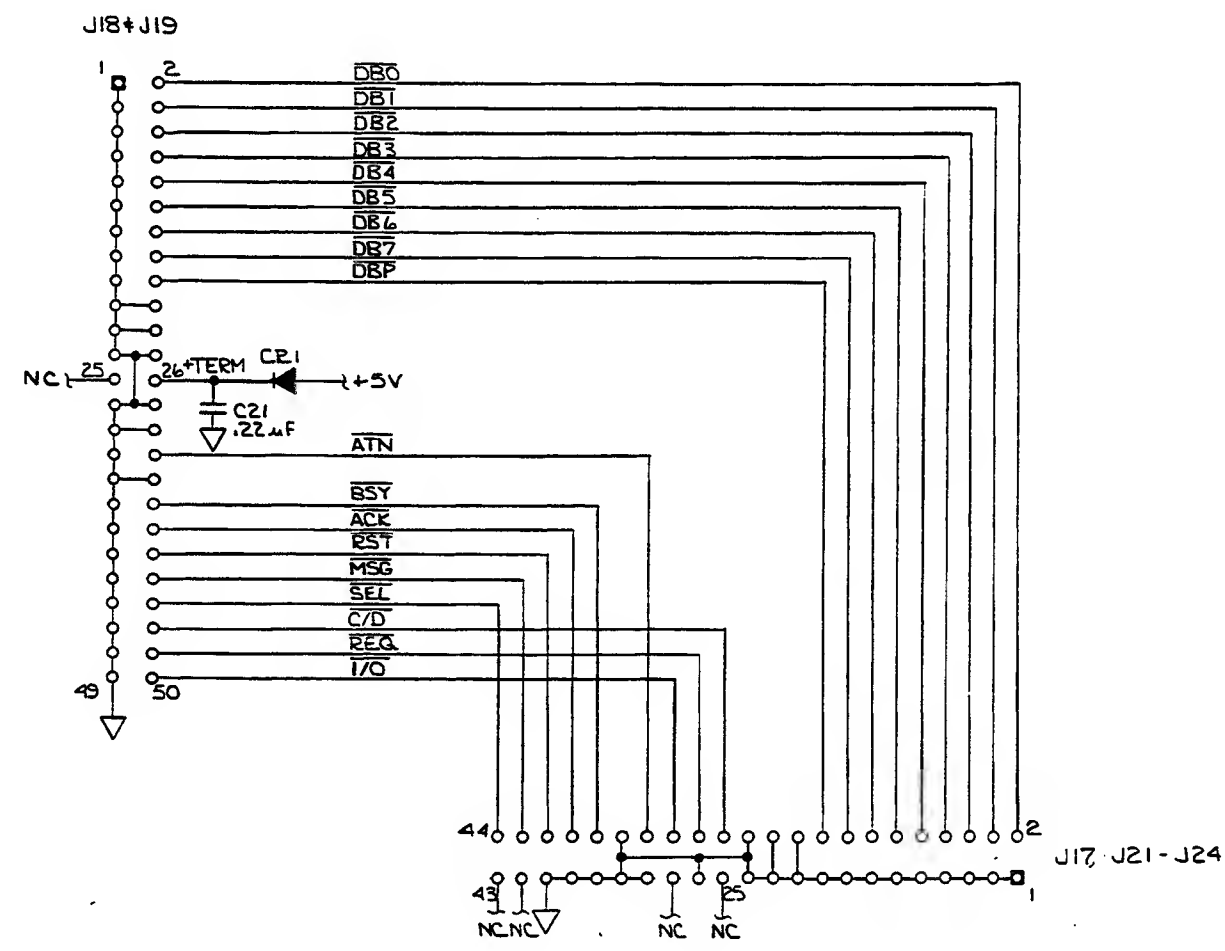
1722A-1602

Figure 5-2. A2 Motherboard PCA



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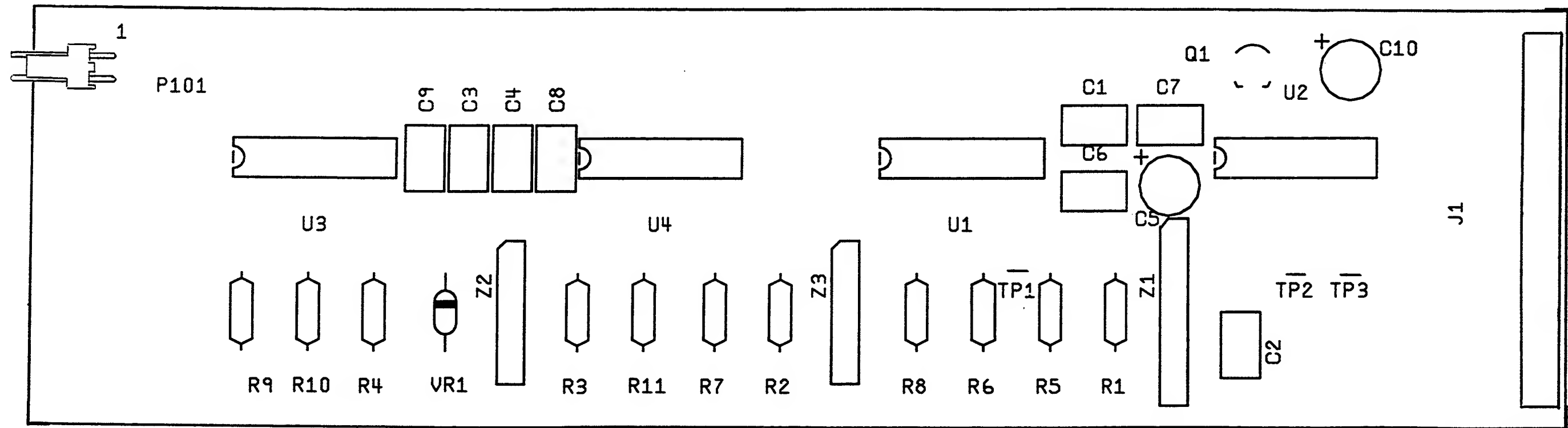
Figure 5-2. A2 Motherboard PCA (cont)



NOTES UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCES ARE IN OHMS
2 ALL CAPACITANCES ARE IN MICROFARADS
3
4

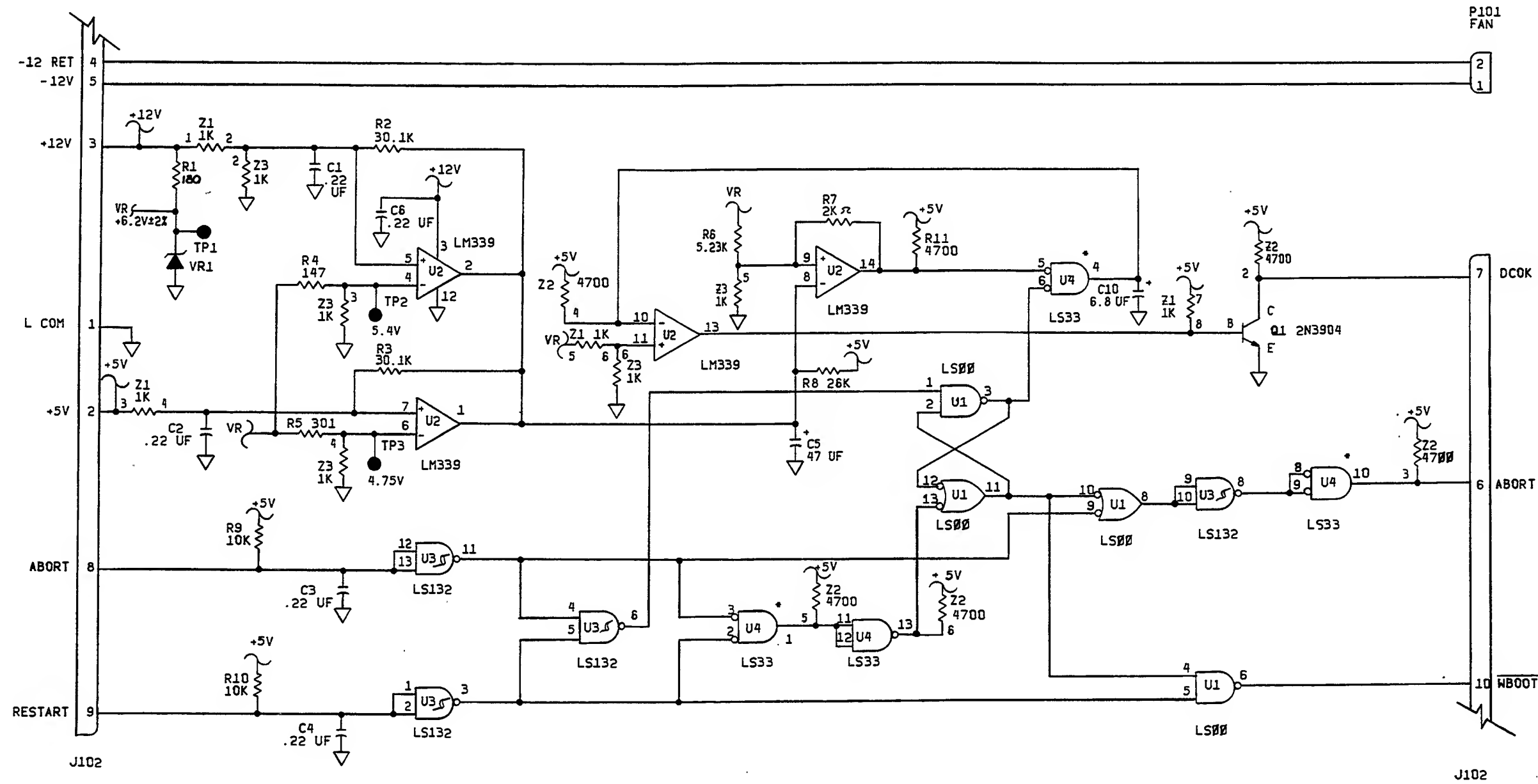
LAST USED	NOT USED
C34	C4, 5, 7
CR1	
J25	
R3	
TP20	TP18, 19
Y1	

Figure 5-2. A2 Motherboard PCA (cont)



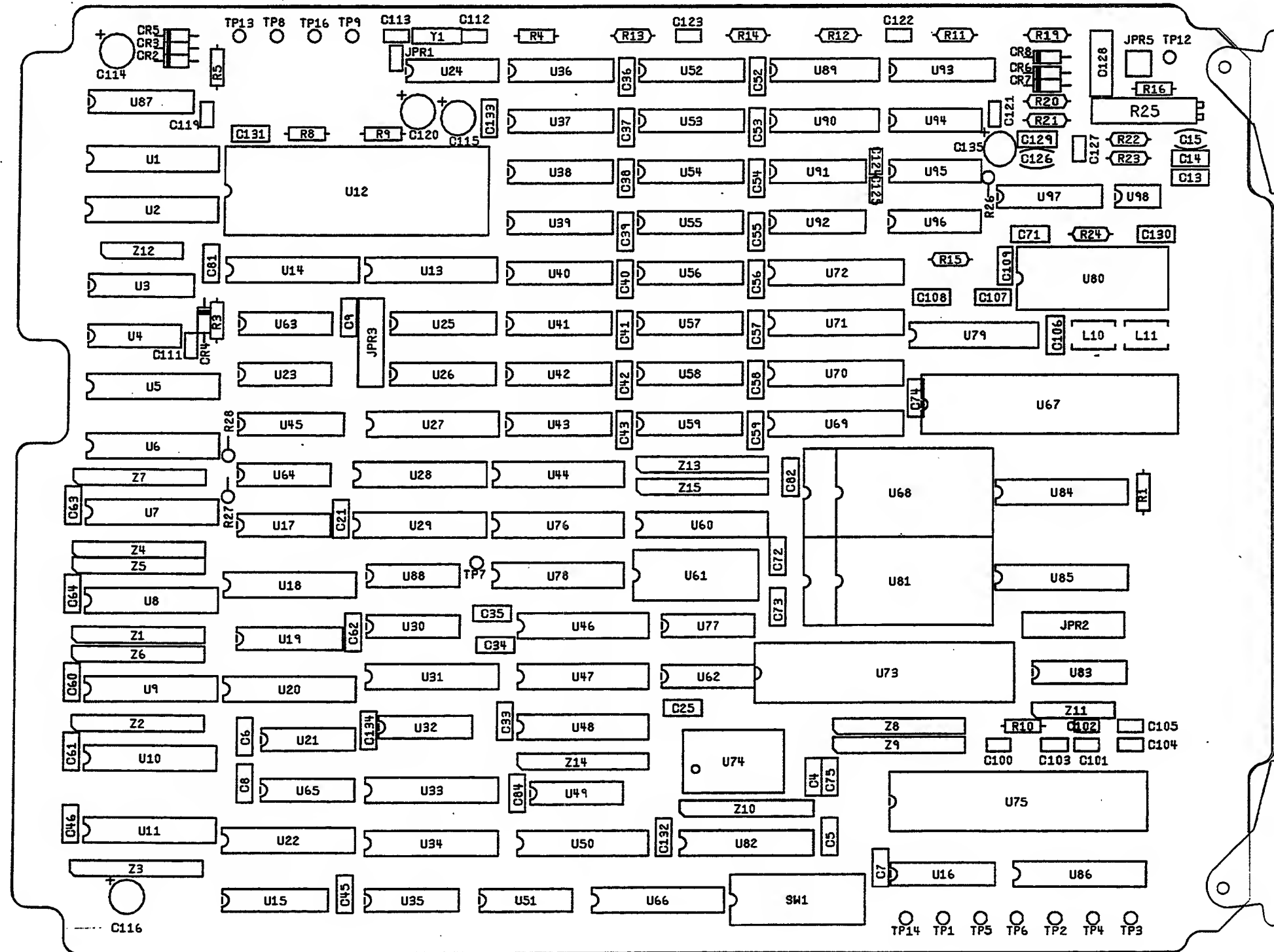
1722A-1603

Figure 5-3. A3 Power-up (PUP) PCA



1722A-1003

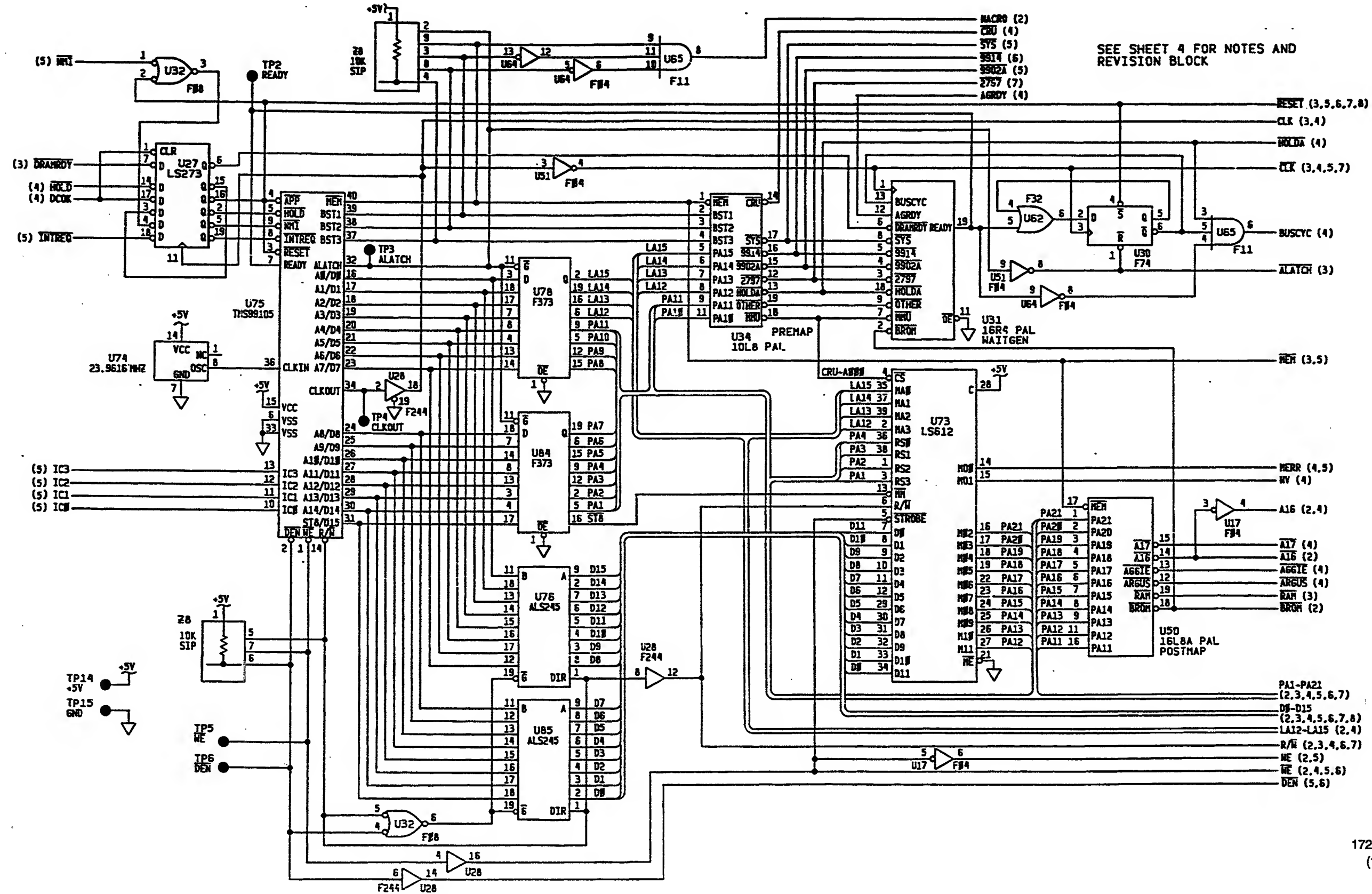
Figure 5-3. A3 Power-up (PUP) PCA (cont)



1722A-1604

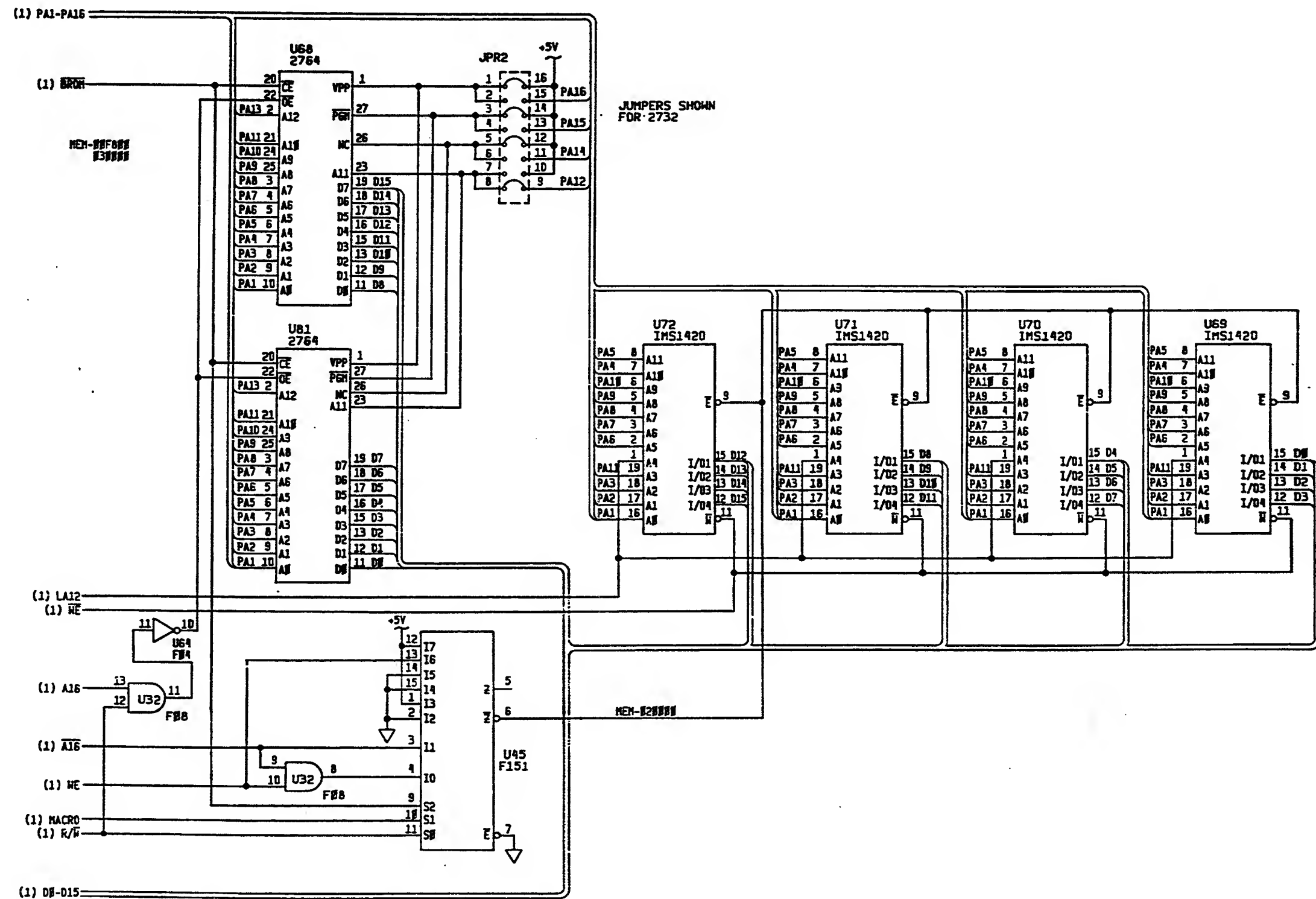
Figure 5-4. A4 Single-Board Computer (SBC)
Module (Rev.D)

Schematic Diagrams



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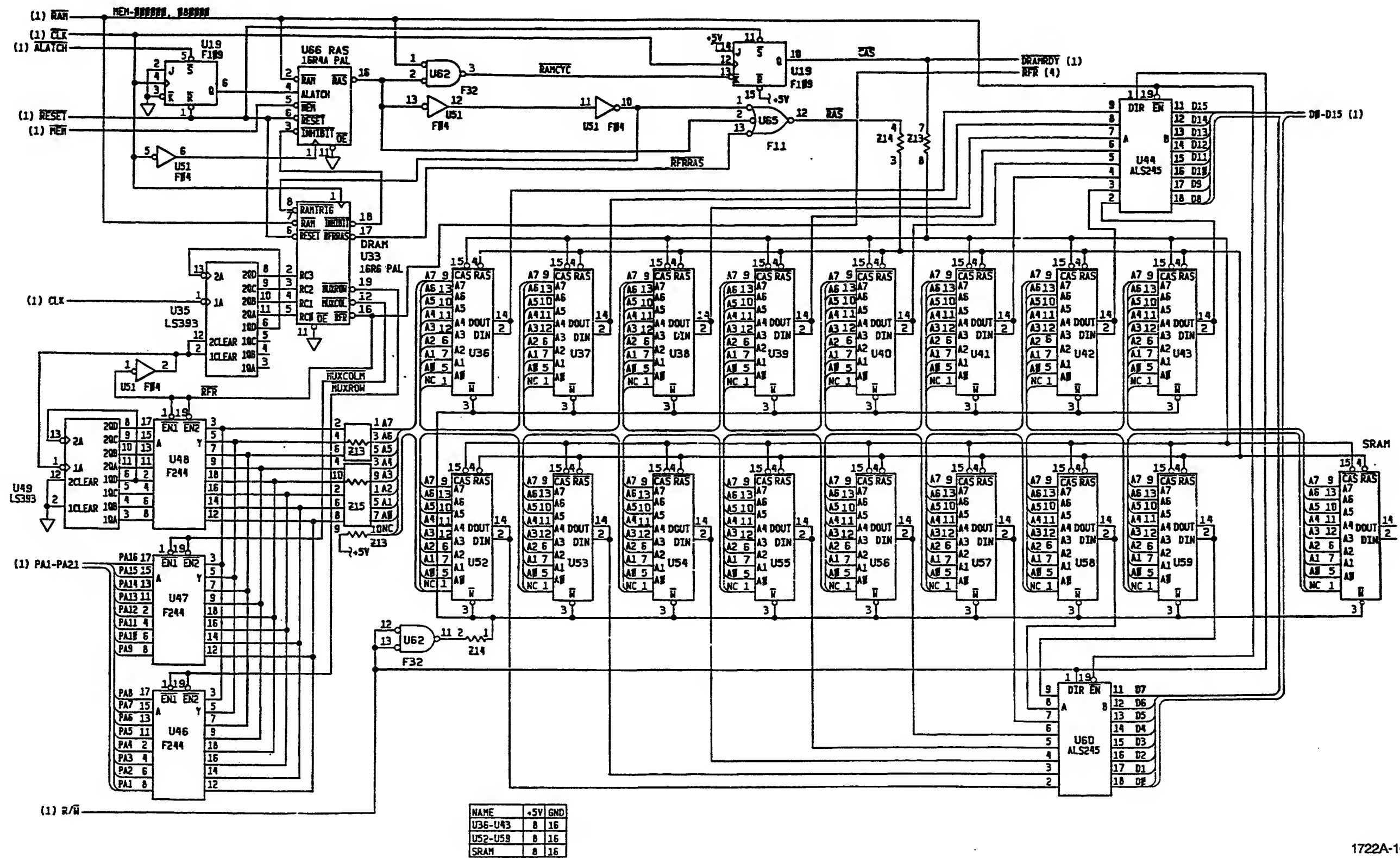
Figure 5-4. A4 Single-Board Computer (SBC)
Module (Rev.D) (cont)



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Figure 5-4. A4 Single-Board Computer (SBC)
Module (Rev.D) (cont)

Schematic Diagrams



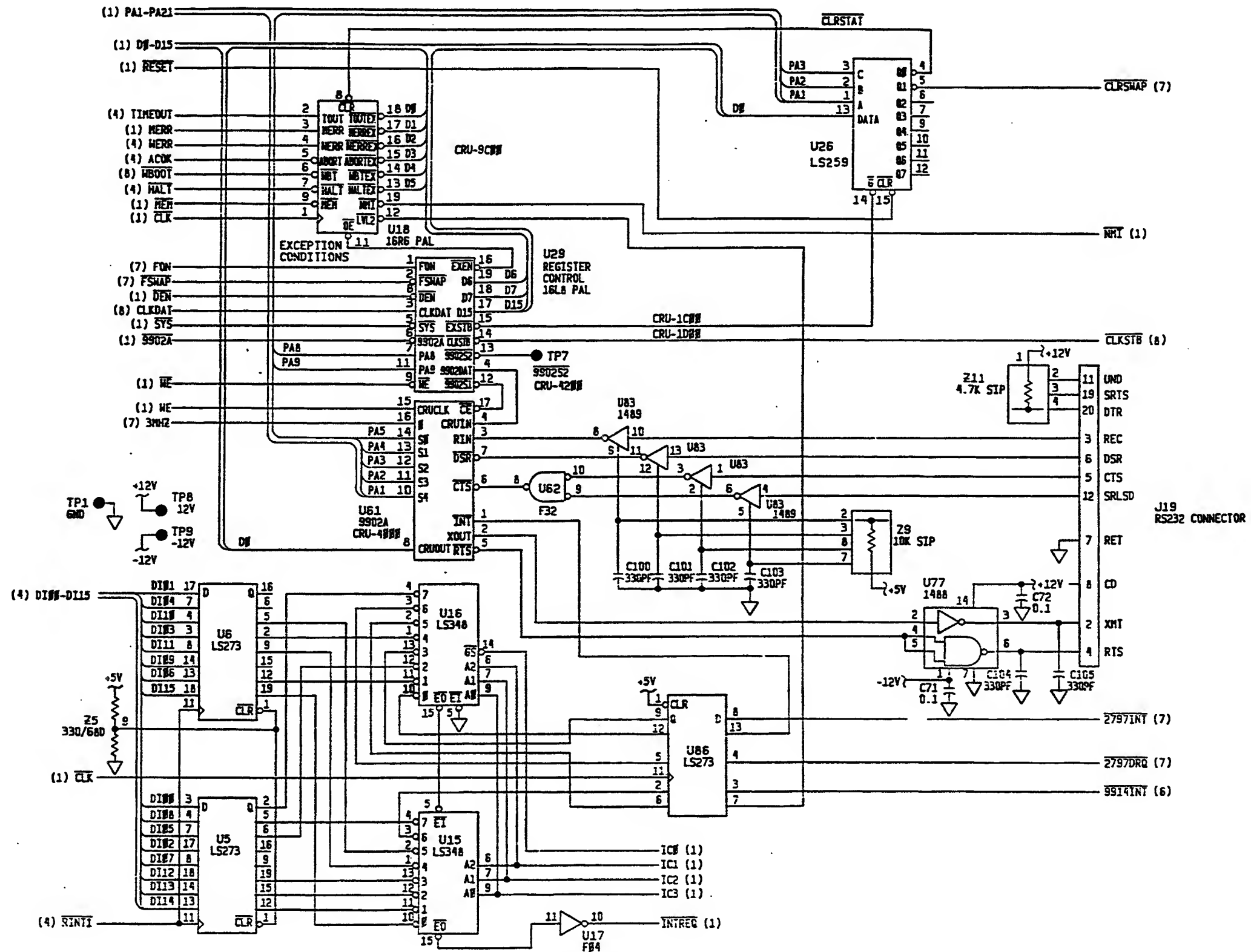
1722A-1004
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Figure 5-4. A4 Single-Board Computer (SBC) Module (Rev.D) (cont)



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Schematic Diagrams



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Figure 5-4. A4 Single-Board Computer (SBC) Module (Rev.D) (cont)

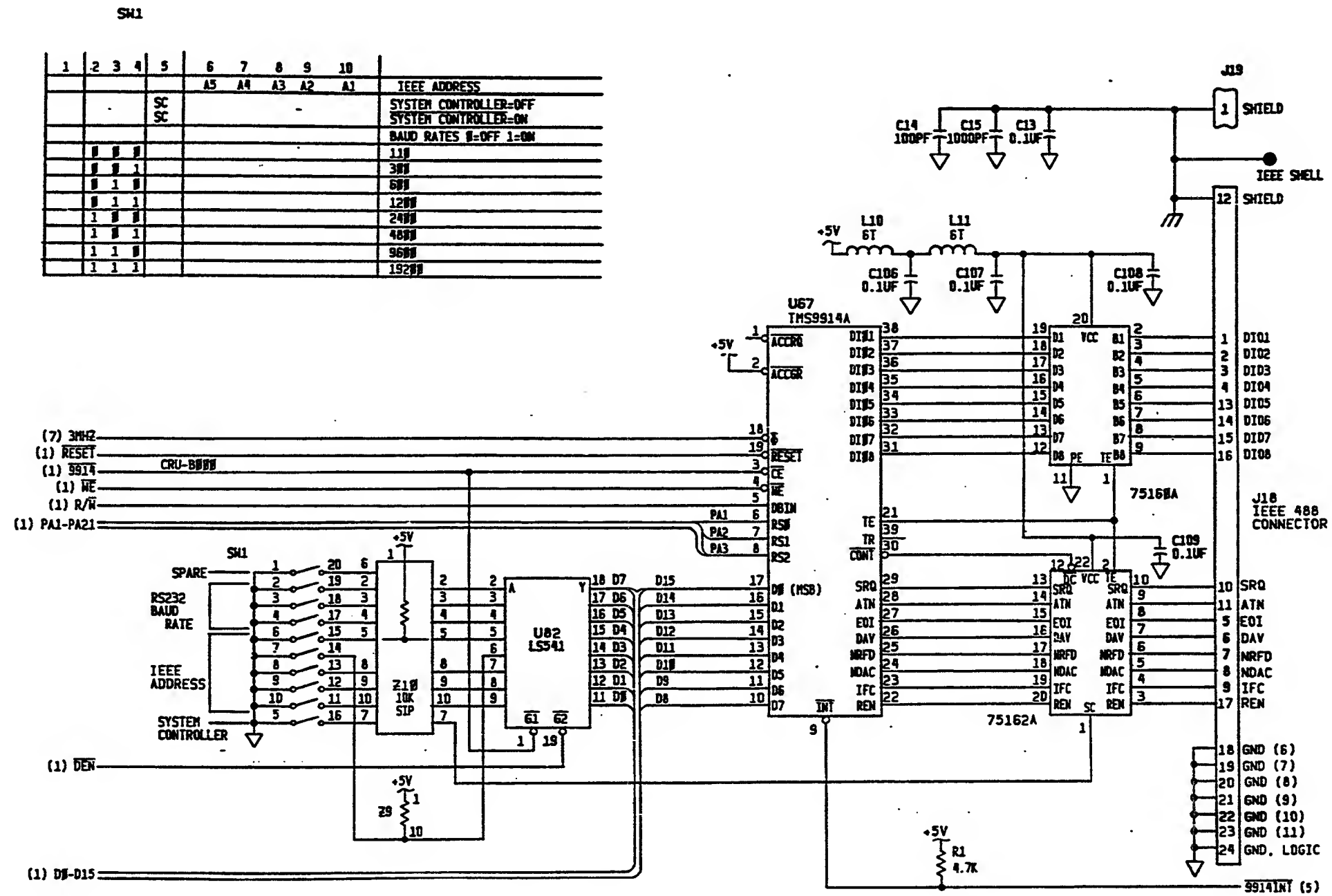
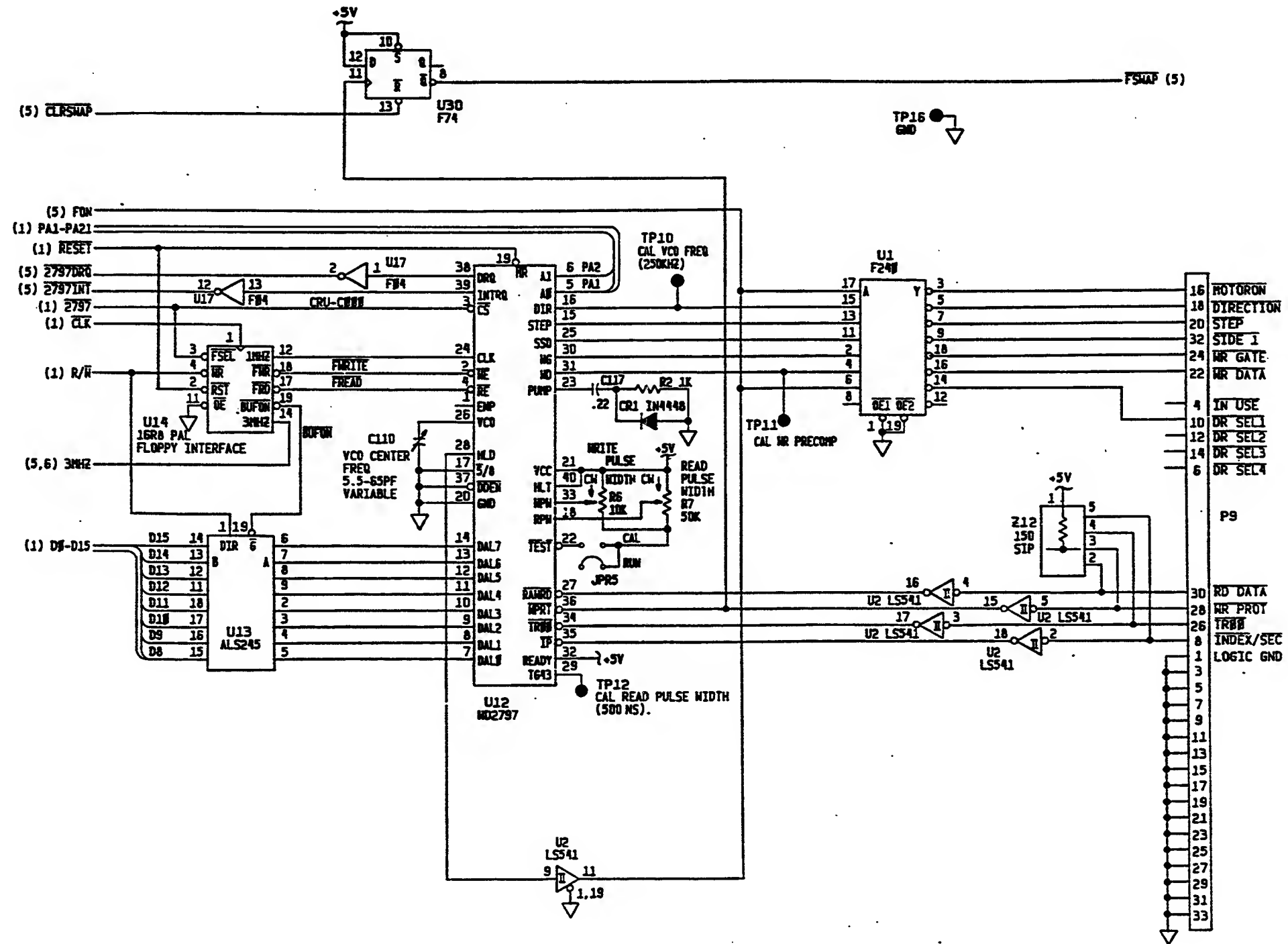


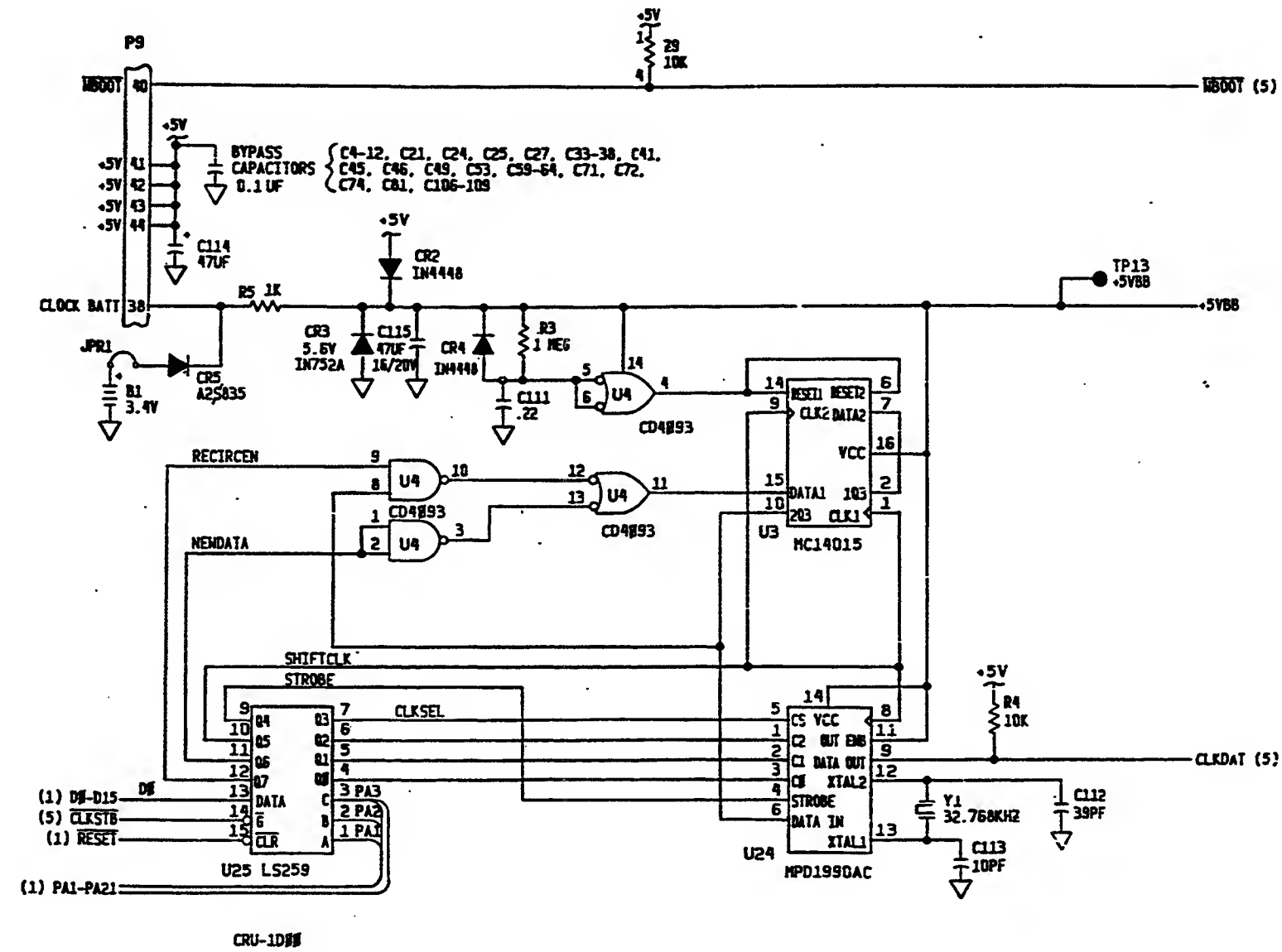
Figure 5-4. A4 Single-Board Computer (SBC) Module (Rev.D) (cont)

Schematic Diagrams



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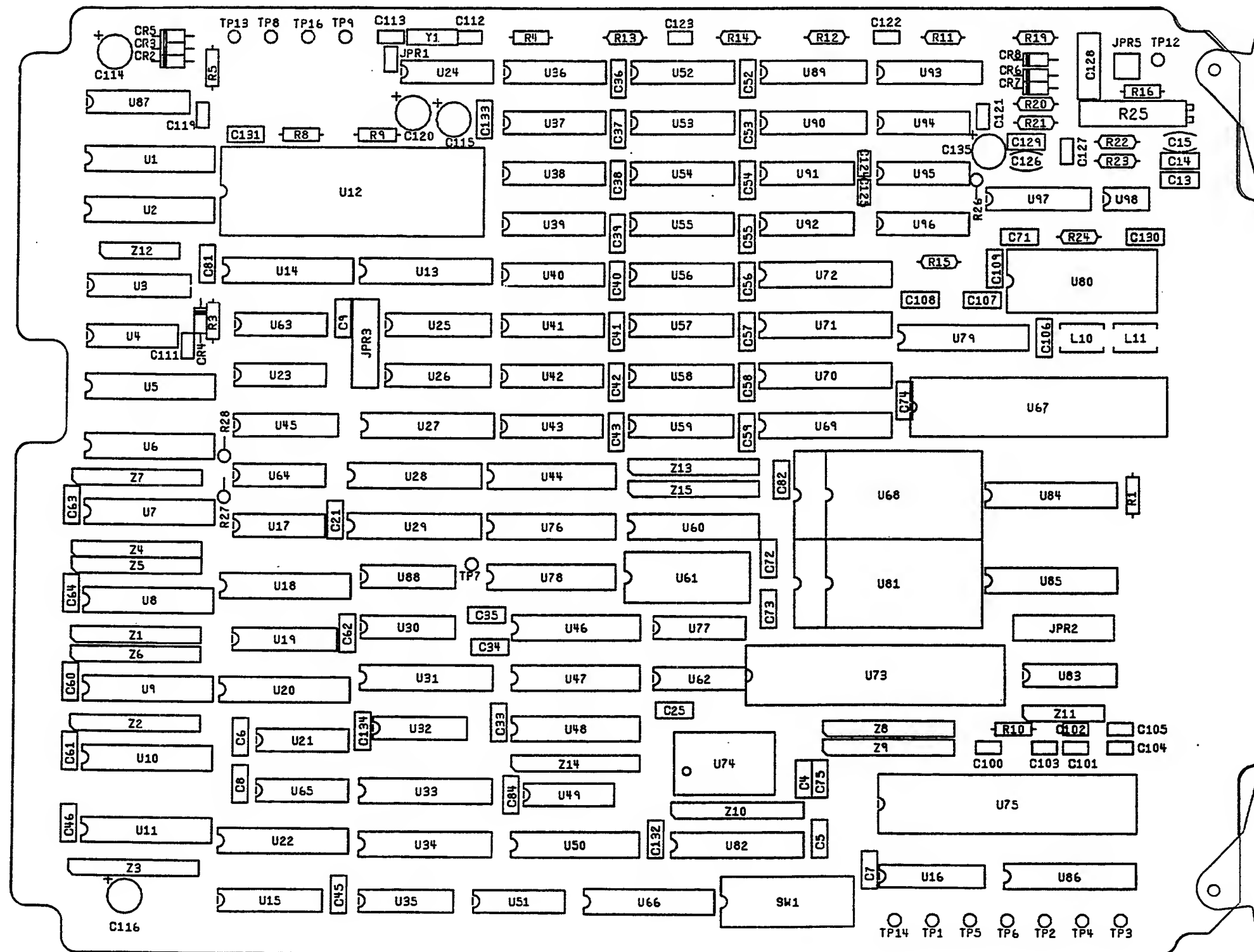
Figure 5-4. A4 Single-Board Computer (SBC)
Module (Rev.D) (cont)



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Figure 5-4. A4 Single-Board Computer (SBC) Module (Rev.D) (cont)

Schematic Diagrams

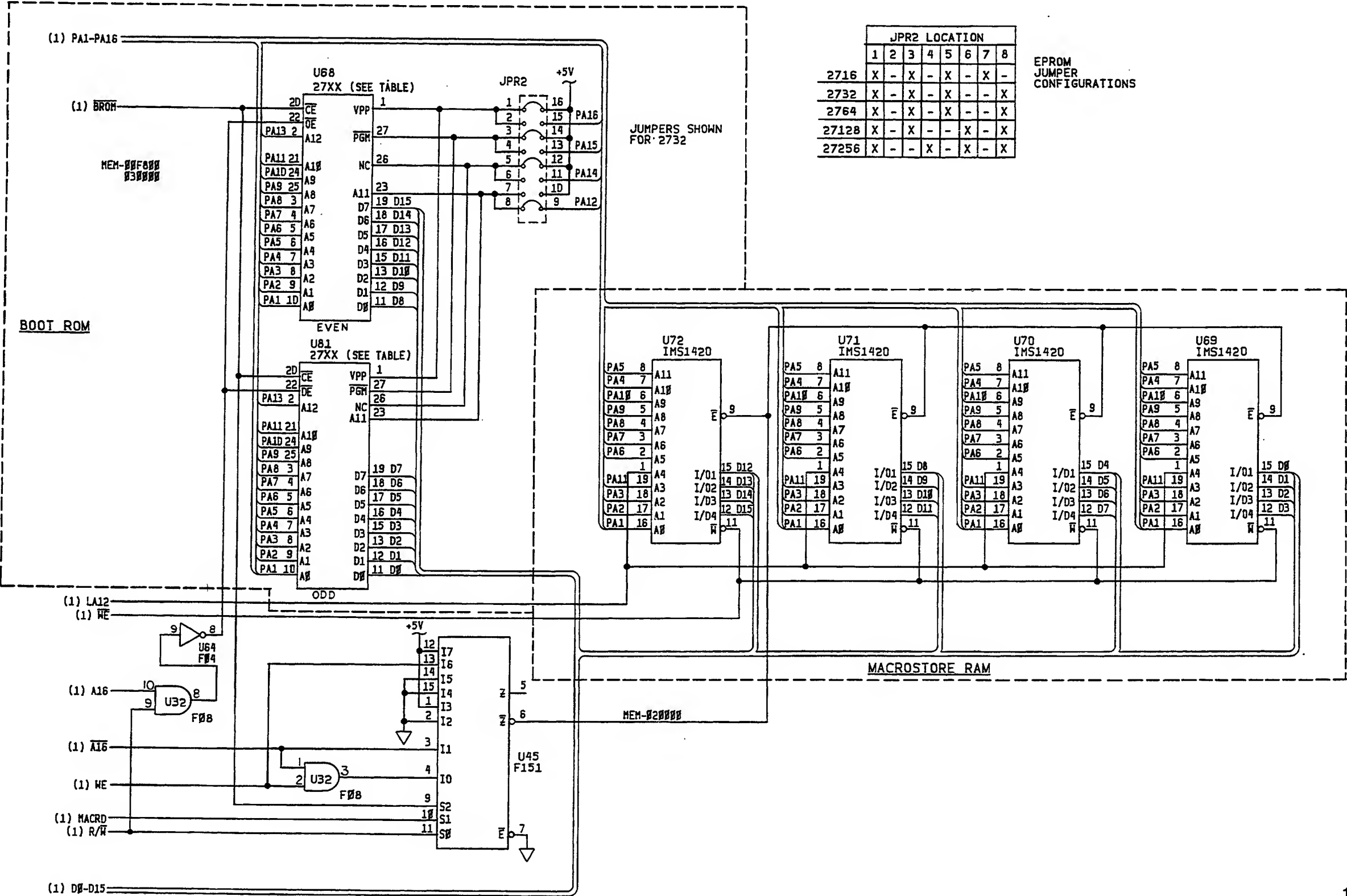


1722A-1604

Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K)



Schematic Diagrams



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Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K) (cont)

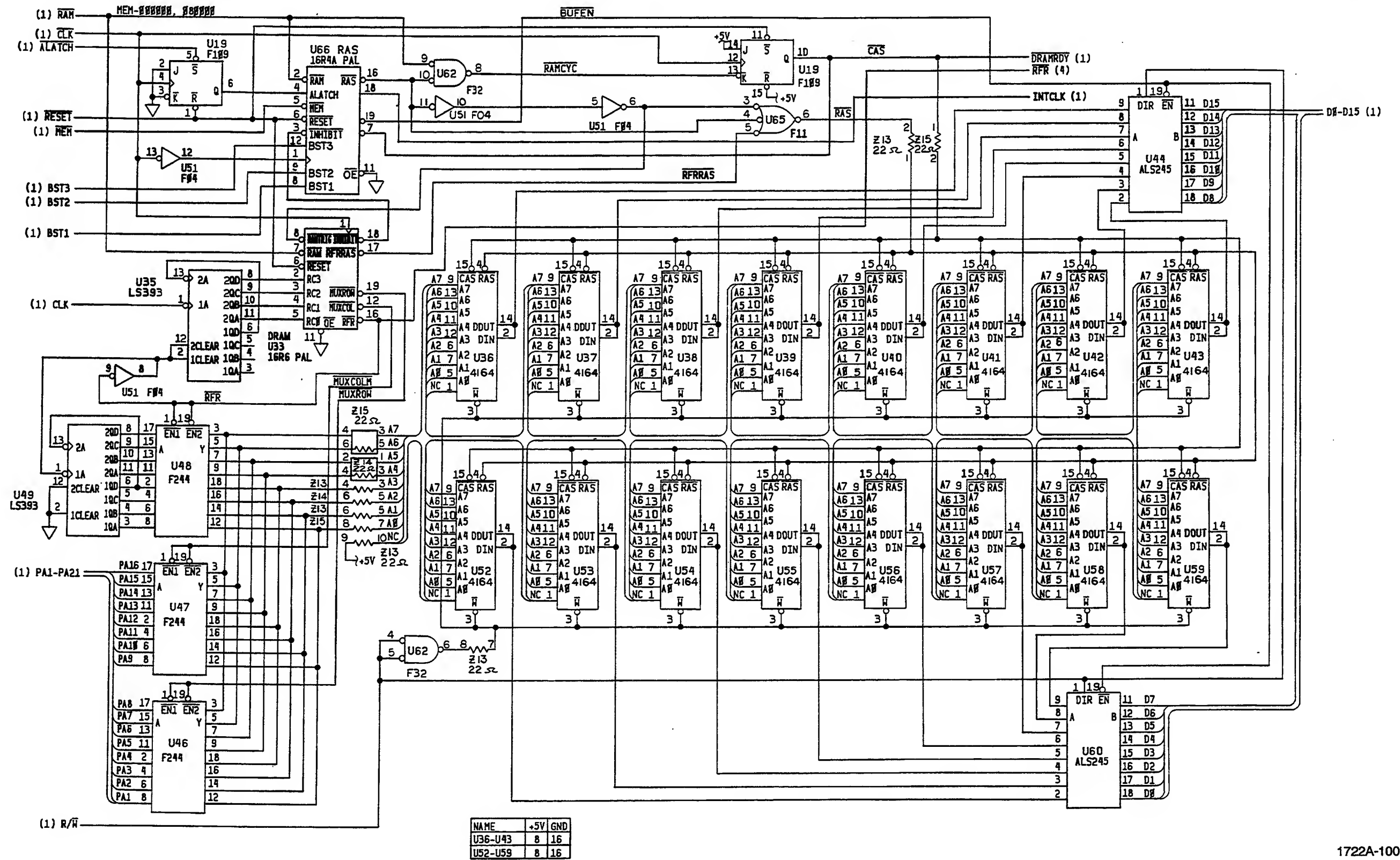
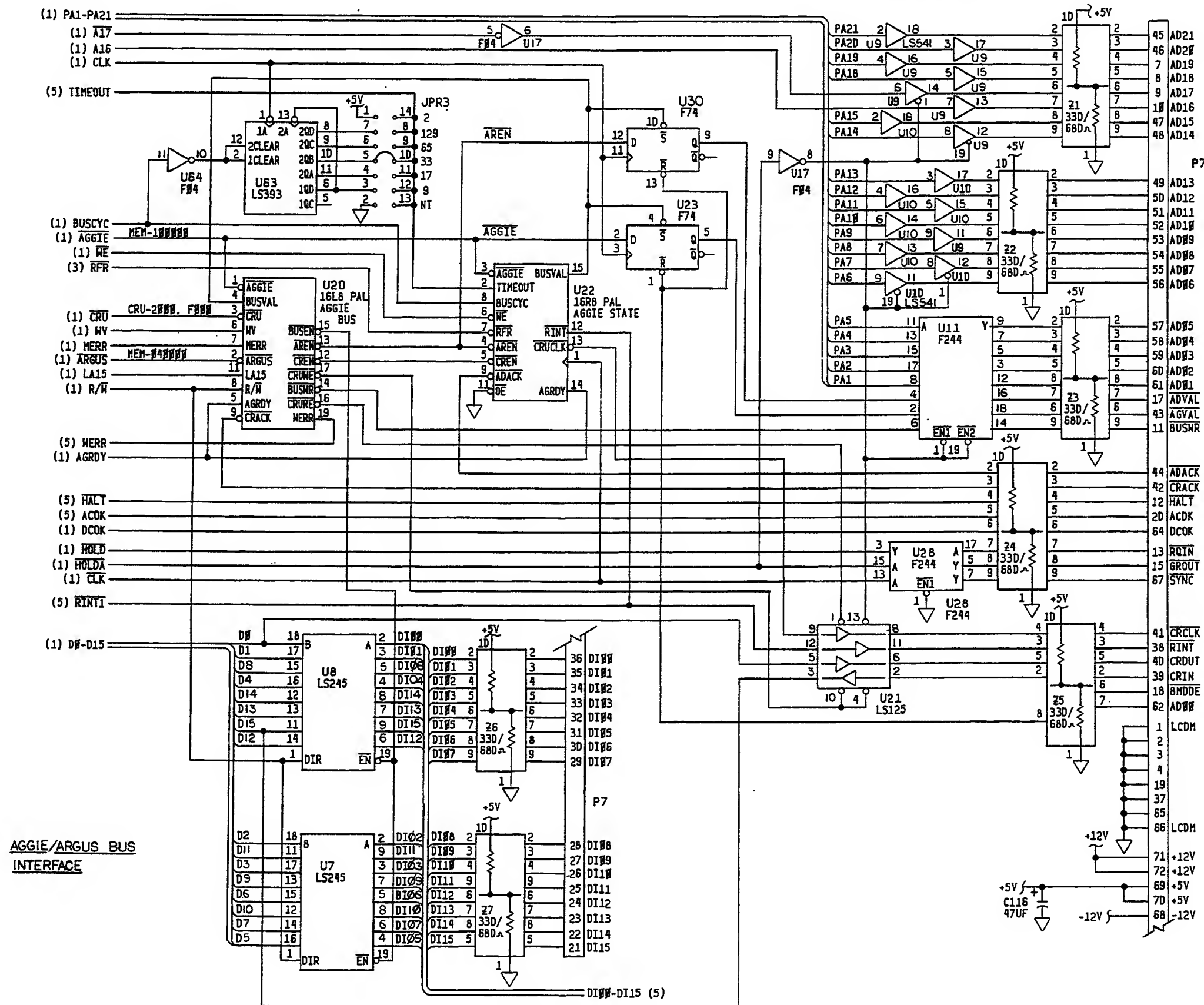


Figure 5-5. A4 Single-Board Computer (SBC) Module (Rev.K) (cont)

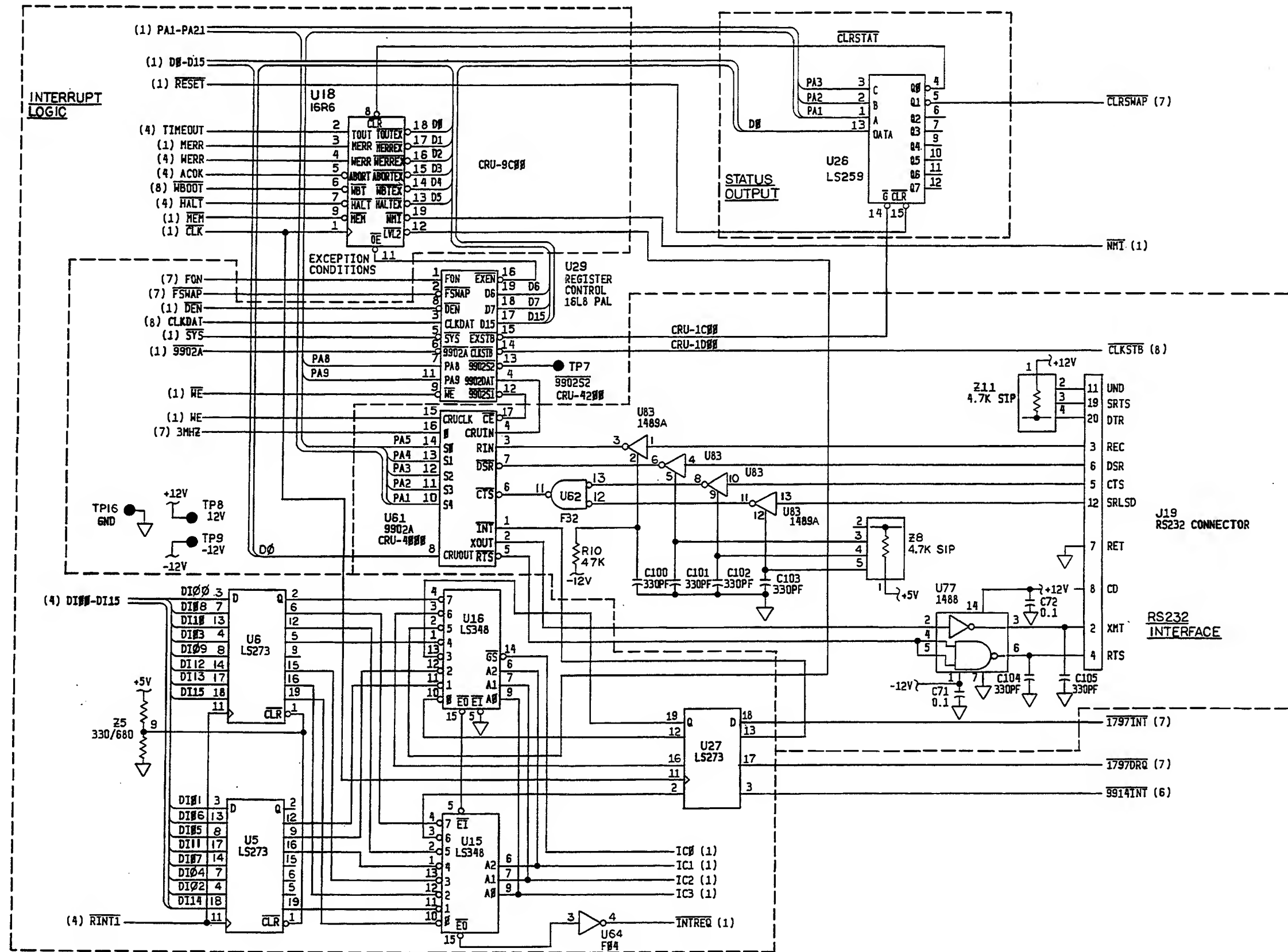
Schematic Diagrams



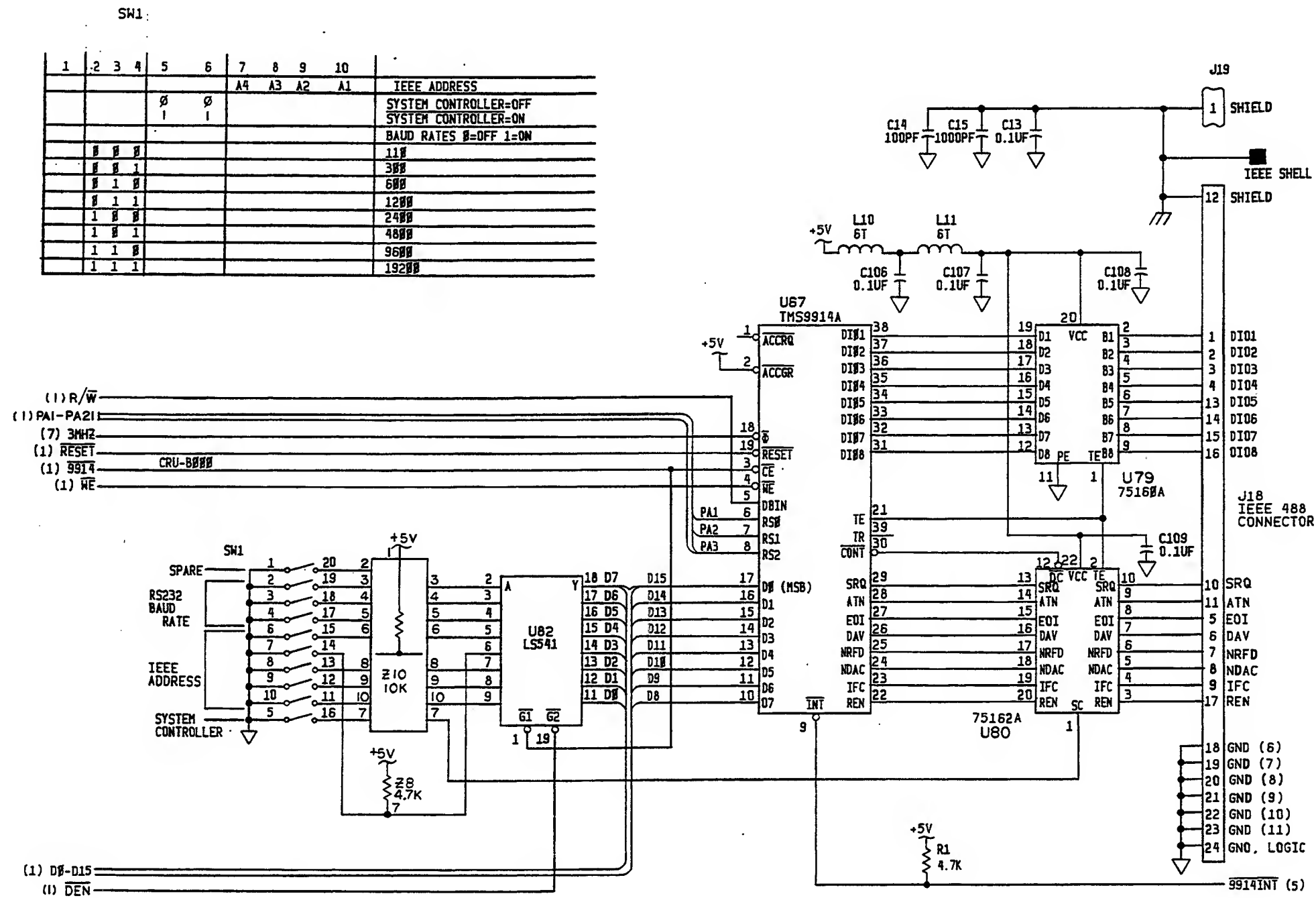
NOTES: UNLESS OTHERWISE SPECIFIED

1. +5 AND GND ARE NOT SHOWN EXPLICITLY FOR MOST CHIPS. FOR CHIPS WITHOUT +5 AND GND, PINS 14, 16, 20... ARE ASSUMED TO BE +5 AND PINS 7, 8, 10... ARE ASSUMED TO BE GROUND. OTHER SUPPLY VOLTAGES ARE SHOWN EXPLICITLY.
2. ALL RESISTANCE IS IN OHMS.
3. ALL CAPACITANCE IS IN MICROFARADS.
4. UNUSED GATES AND PAL INPUTS ARE TIED TO GROUND.
5. ⚠ WARNING: THIS ASSEMBLY CONTAINS DEVICES WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.D.P. 19.1.

Figure 5-5. A4 Single-Board Computer (SBC) Module (Rev.K) (cont)



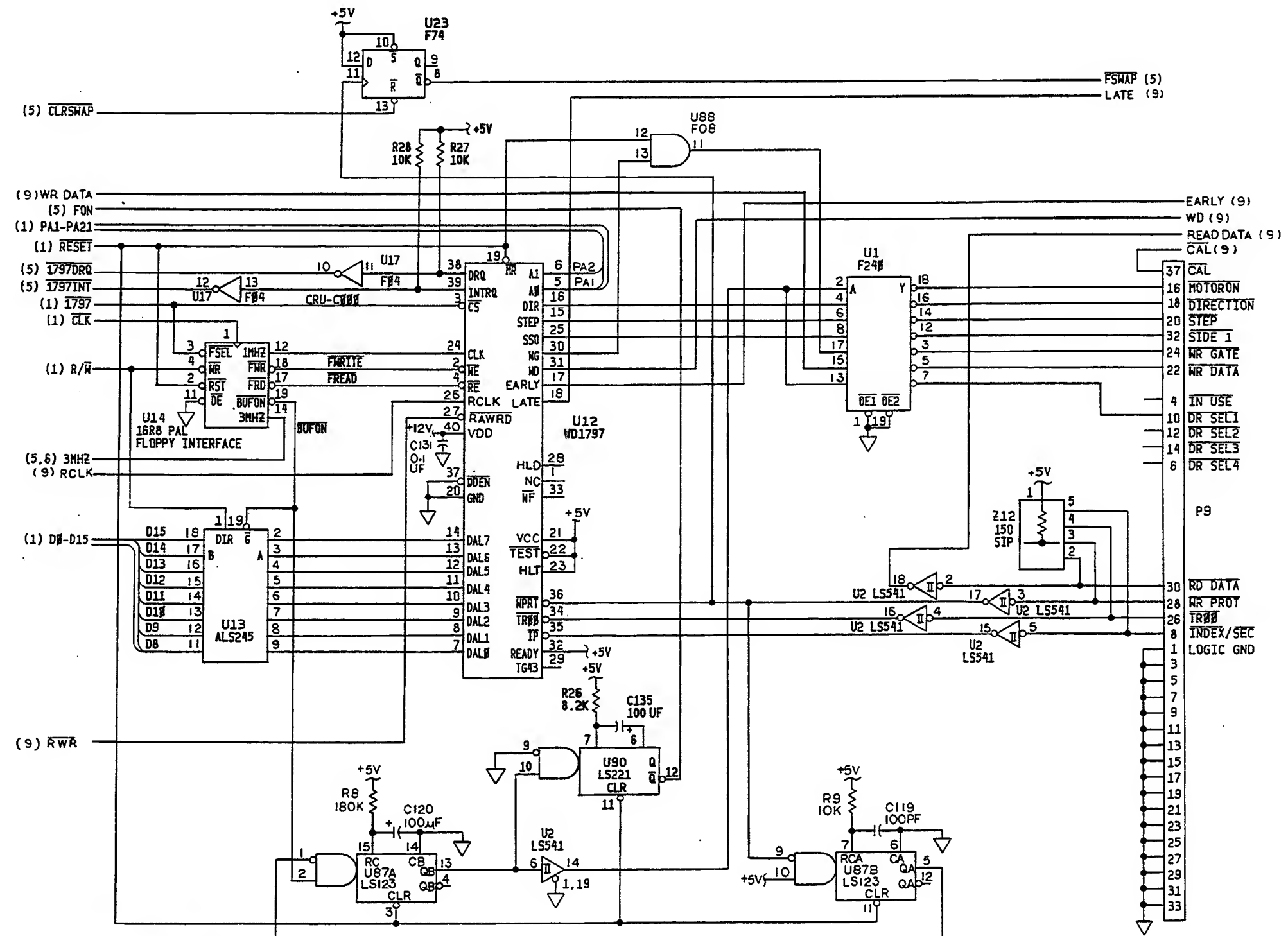
Schematic Diagrams



IEEE 488 INTERFACE

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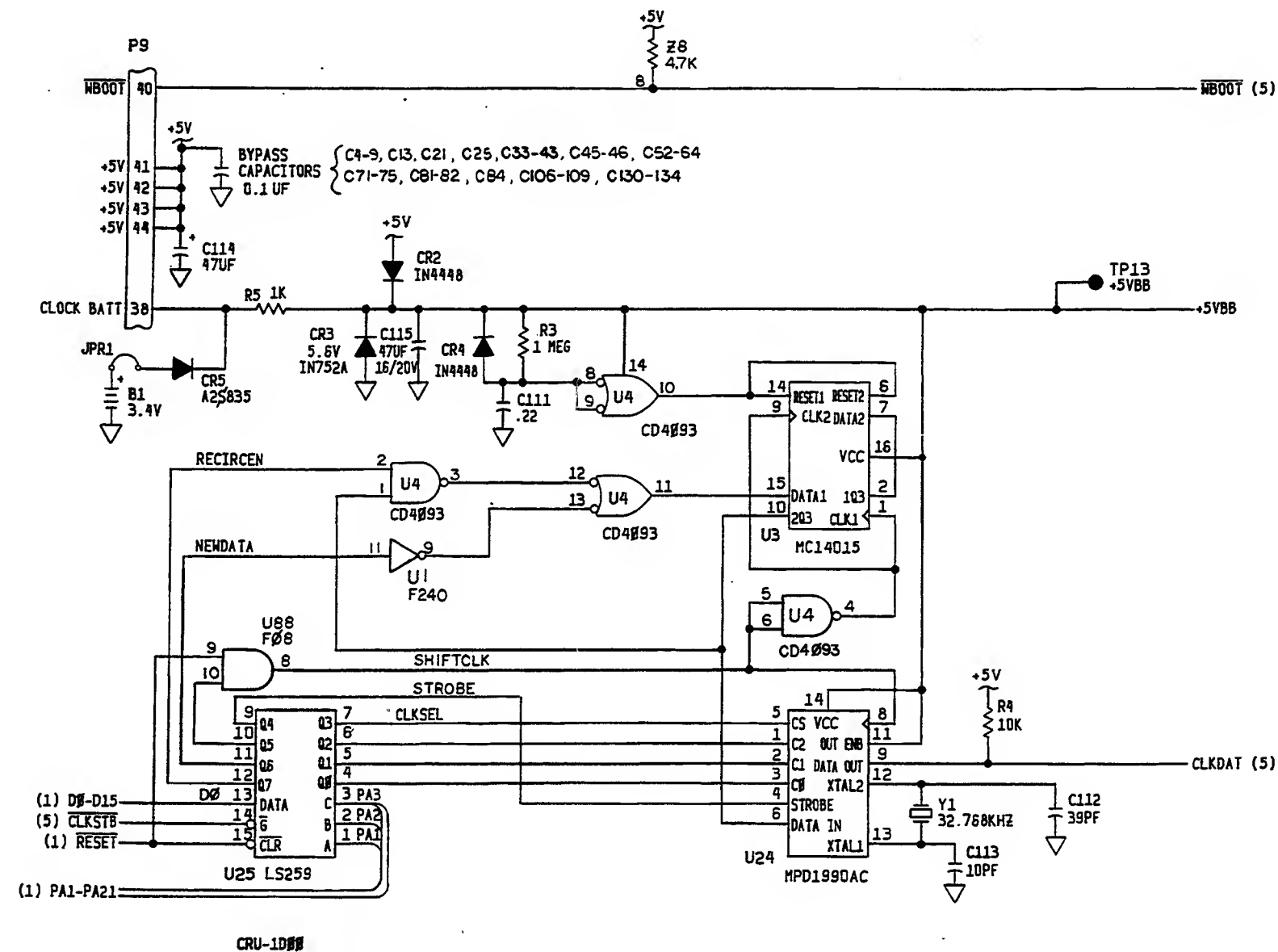
Figure 5-5. A4 Single-Board Computer (SBC) Module (Rev.K) (cont)



FLOPPY DISK INTERFACE

1722A-1004
(7 of 10)Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K) (cont)

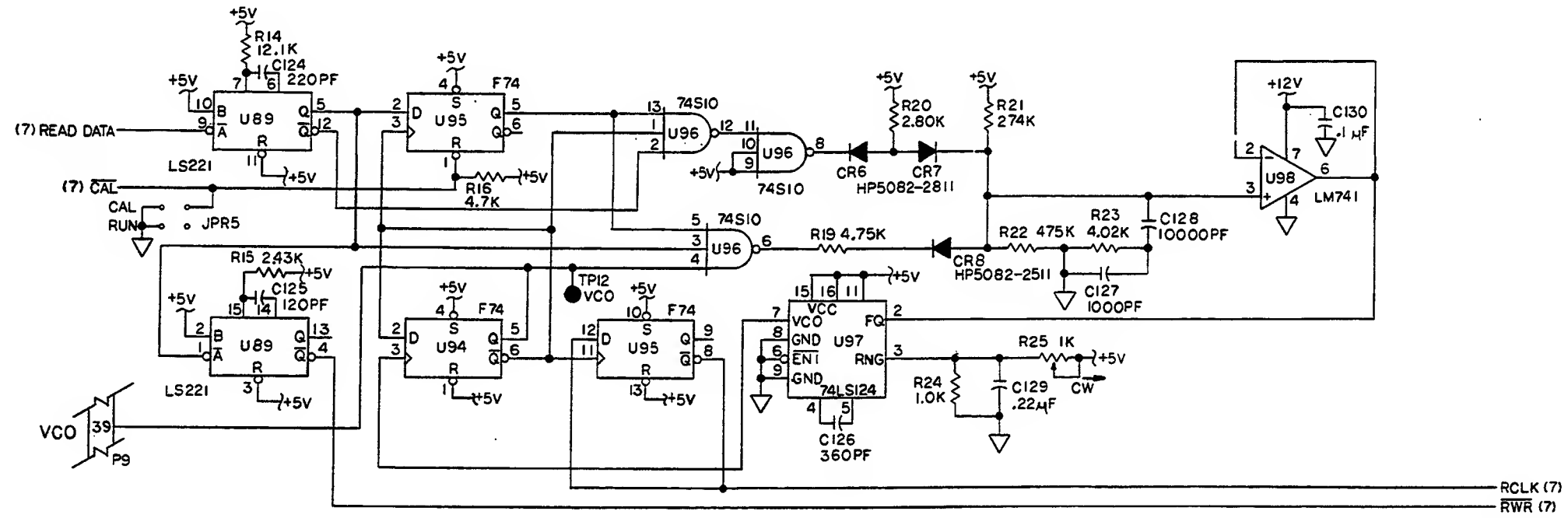
Schematic Diagrams



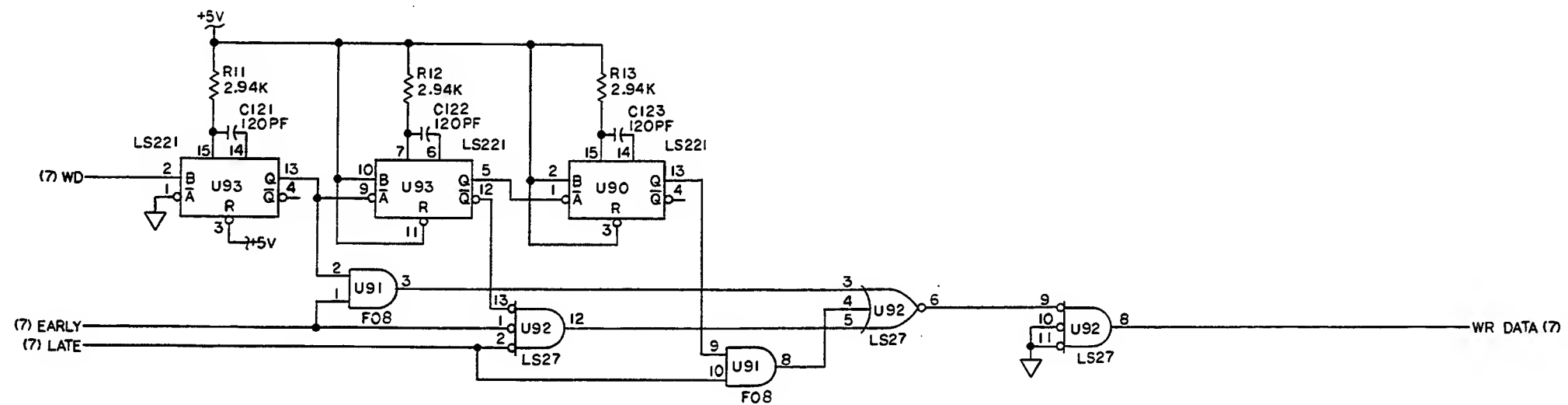
NON-VOLATILE CLOCK CIRCUIT

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Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K) (cont)



WRITE PRECOMPENSATION CIRCUIT



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Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K) (cont)

LAST USED, UNUSED REF DES CHART		
COMPONENT TYPE	LAST USED	UNUSED
I.C.	U98	—
DIODE	CR8	CR1
RES NETWORK	Z15	—
RESISTORS	R28	R2, R6, R7, R17, R18
CAPACITORS	C135	C1-C3, C10-C12, C16-C20, C22-C24, C26-C32, C44, C47-C51, C65-C70, C76-C80, C83, C85-C99, C110, C117, C118,
TEST POINTS	TP16	TP10, TP11, TP15
JUMPERS	JPR5	JPR4
BATTERY	B1	—
CRYSTAL	Y1	—
CHOKE	L11	L1-L9

SBC SPARE GATES:

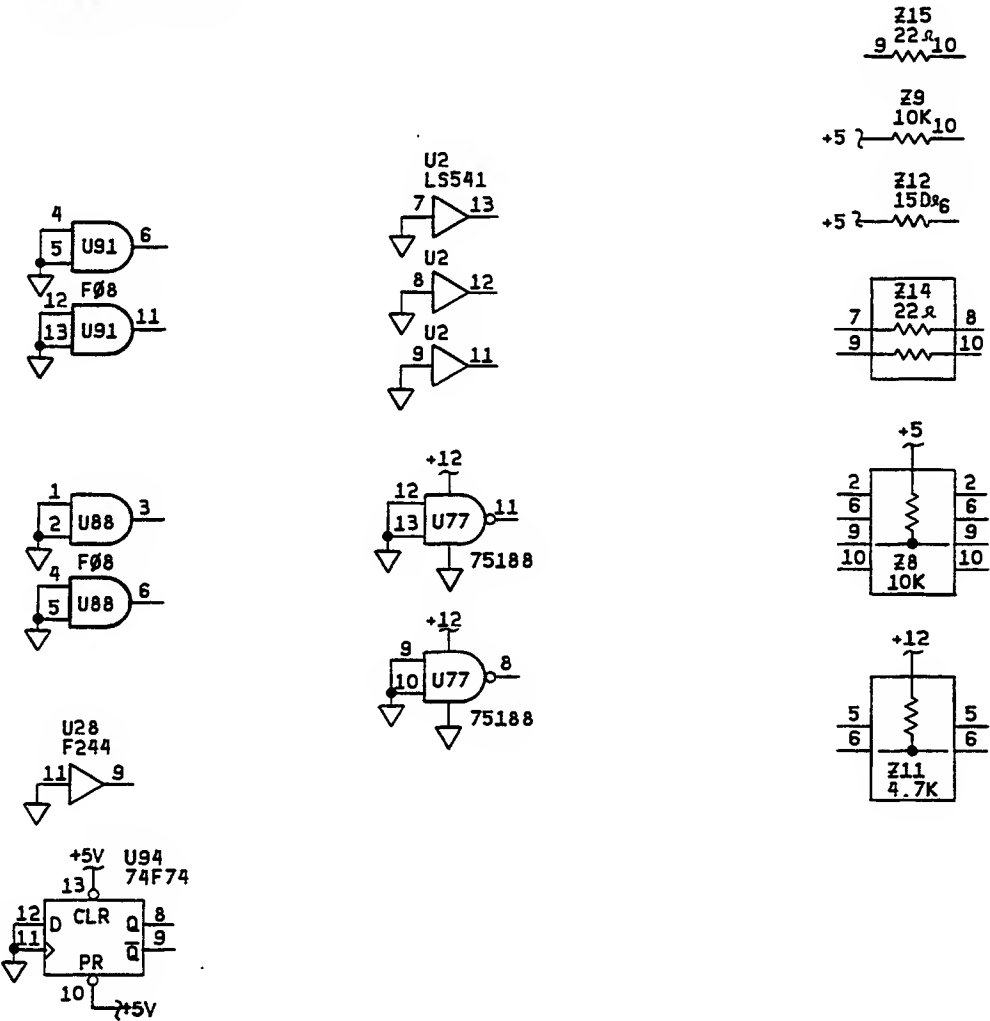
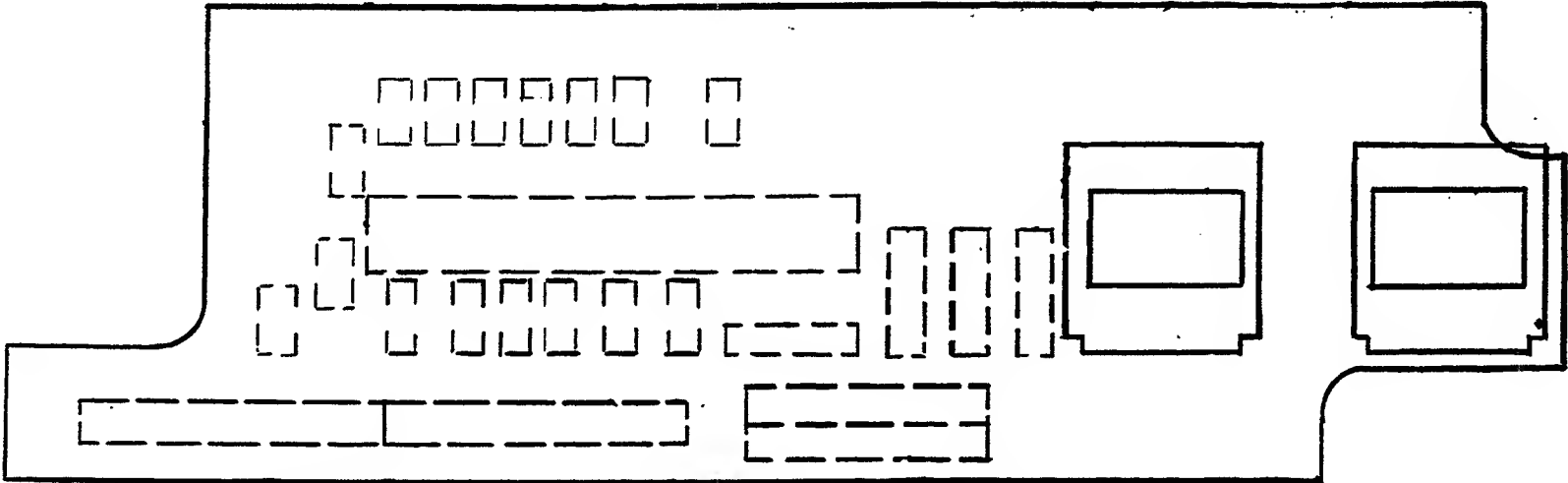


Figure 5-5. A4 Single-Board Computer (SBC)
Module (Rev.K) (cont)



1722A-4005

Figure 5-6. A5 Front Panel Assembly

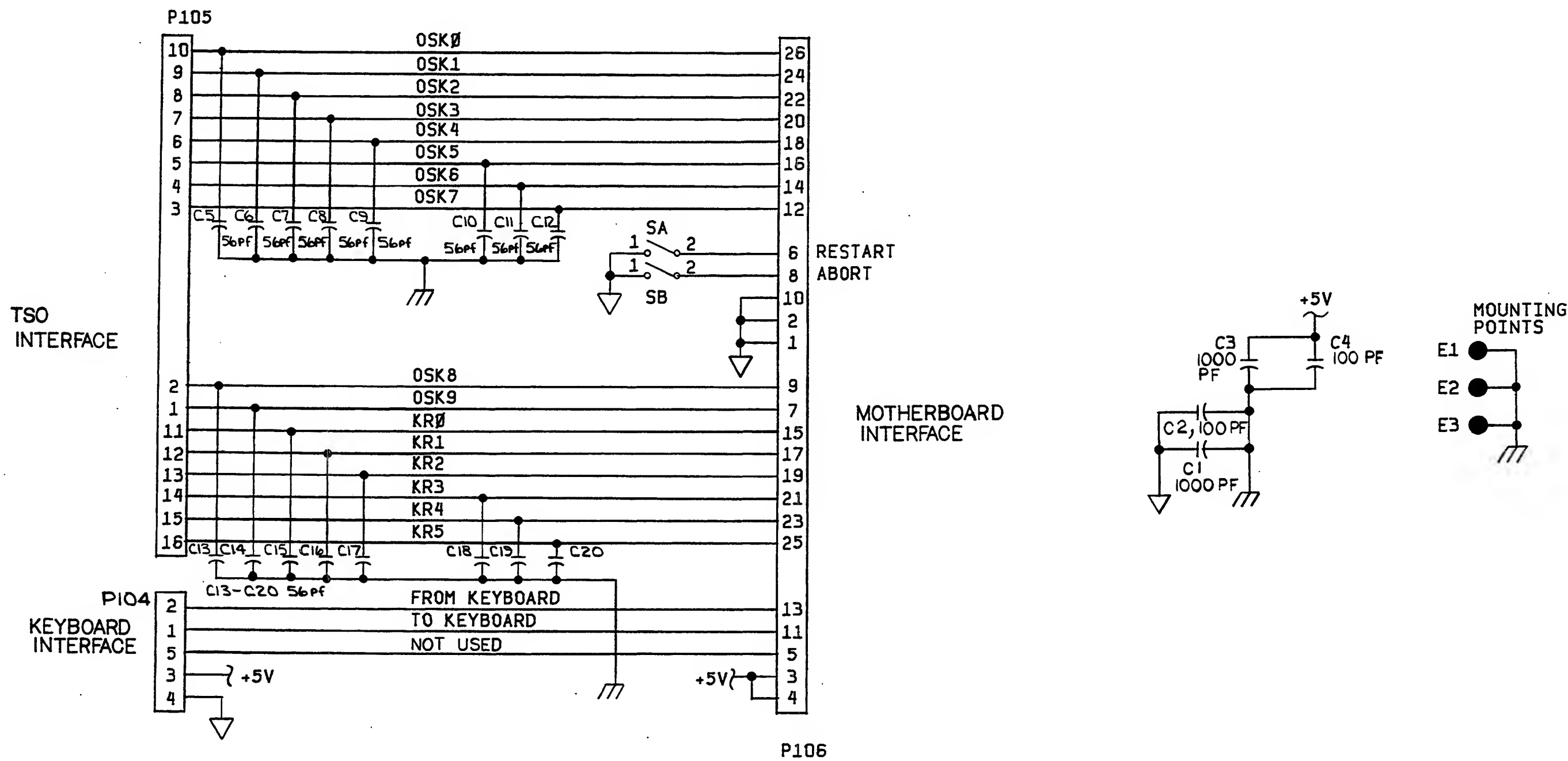
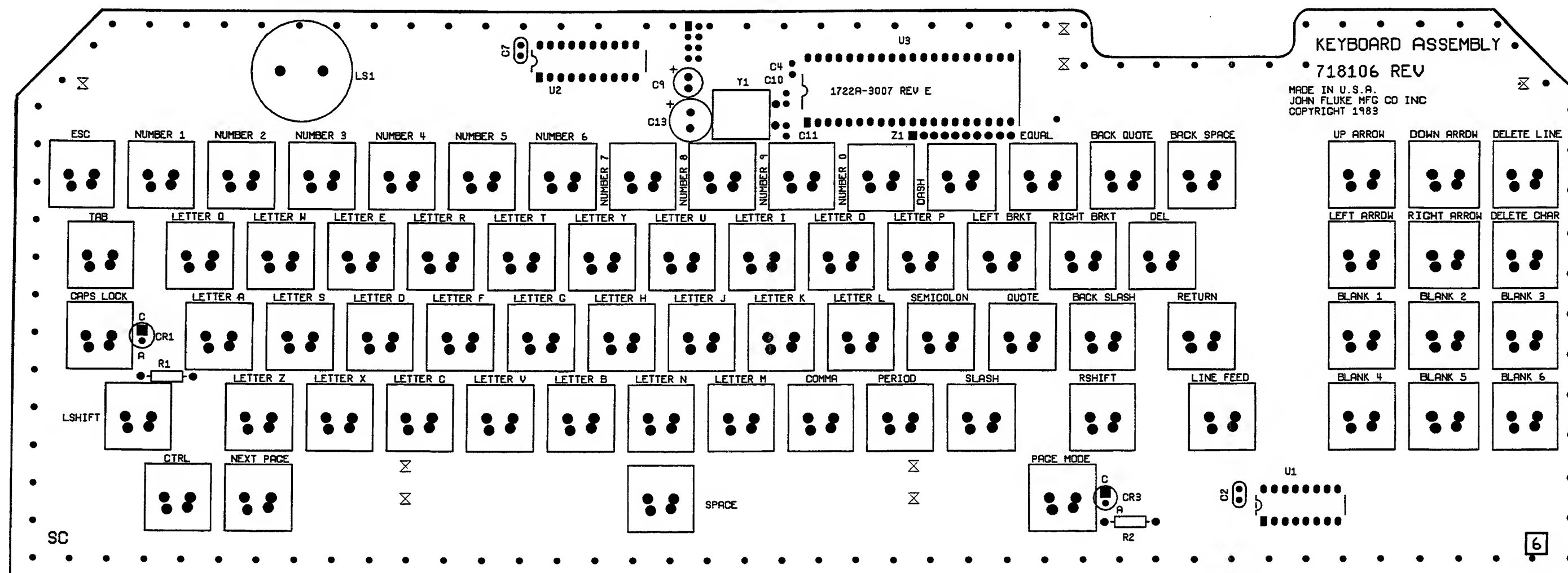
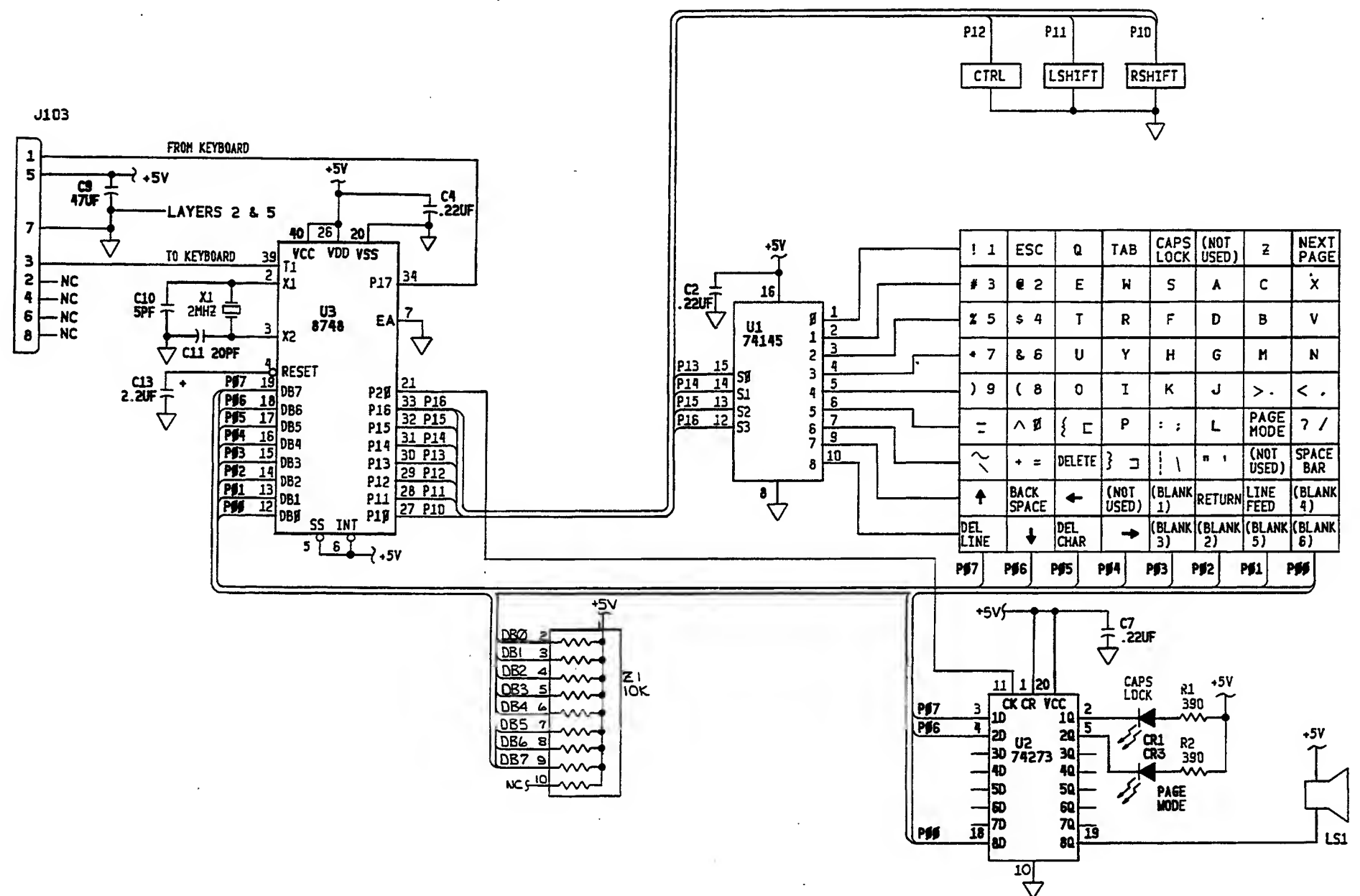


Figure 5-6. A5 Front Panel Assembly (cont)



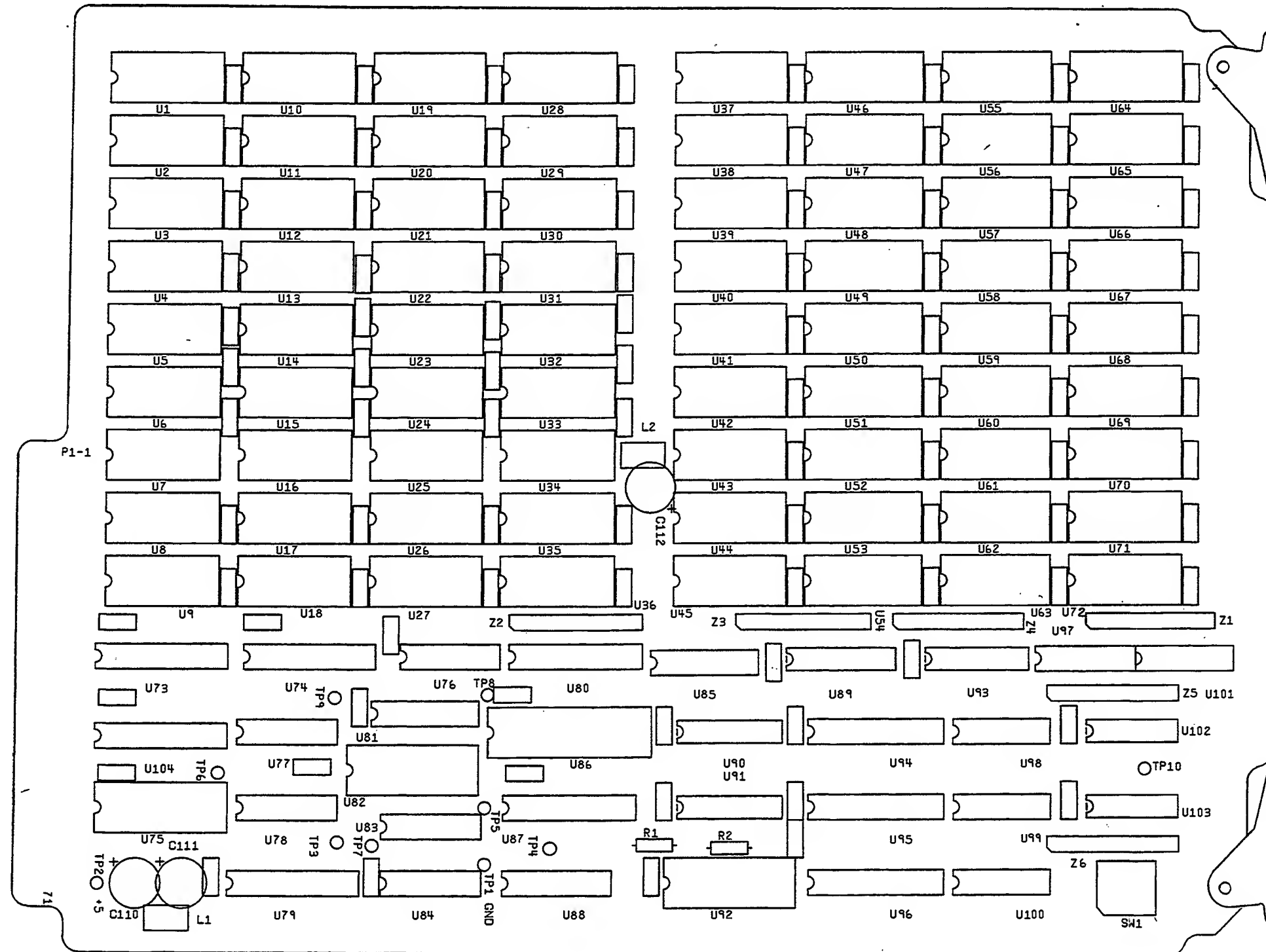
1722A-1607

Figure 5-7. A6A1 Programmer's Keyboard



1722A-1007

Figure 5-7. A6A1 Programmer's Keyboard (cont)



1722A-1608

Figure 5-8. 006, 007, 016, 017 Expansion Modules

Schematic Diagrams

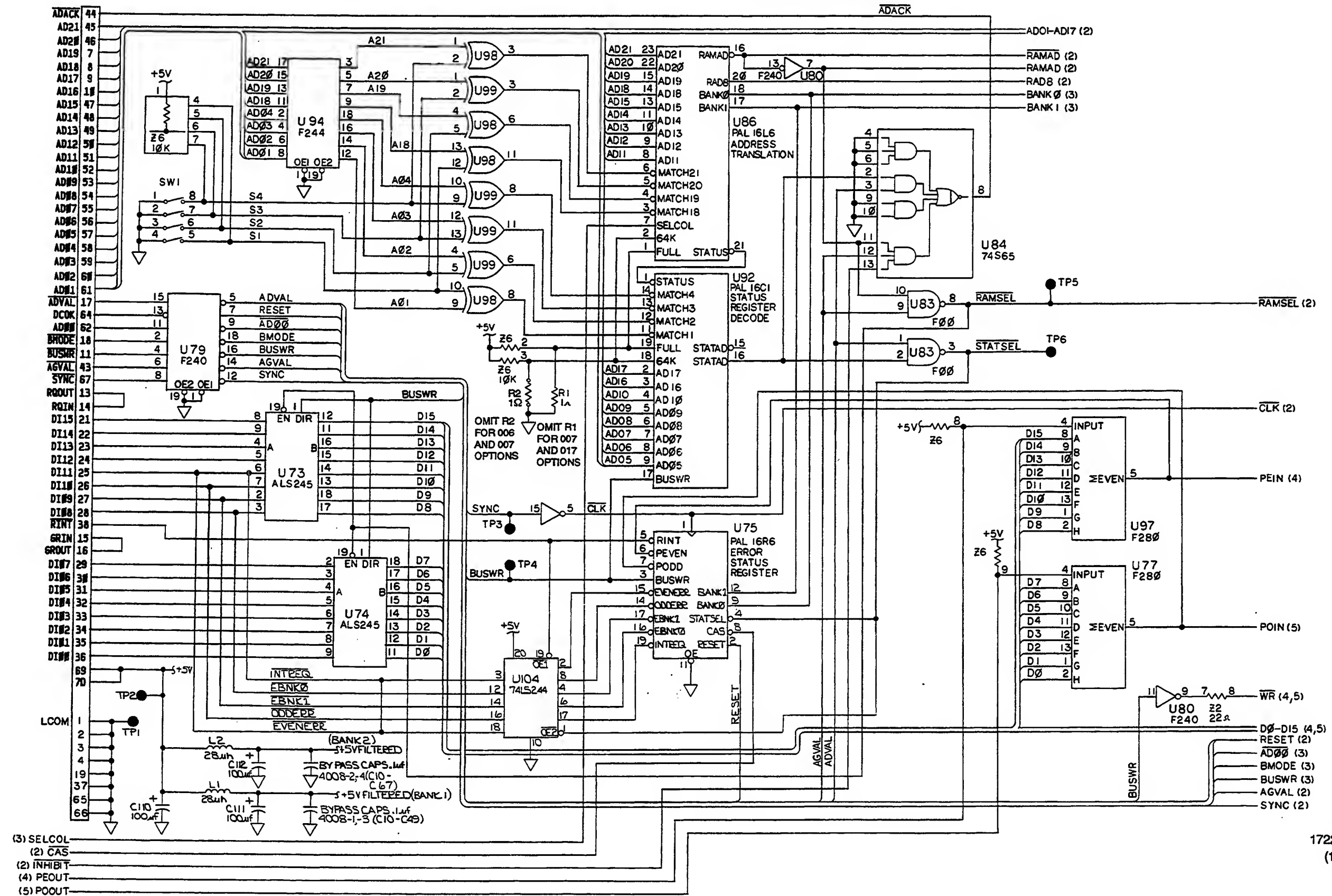
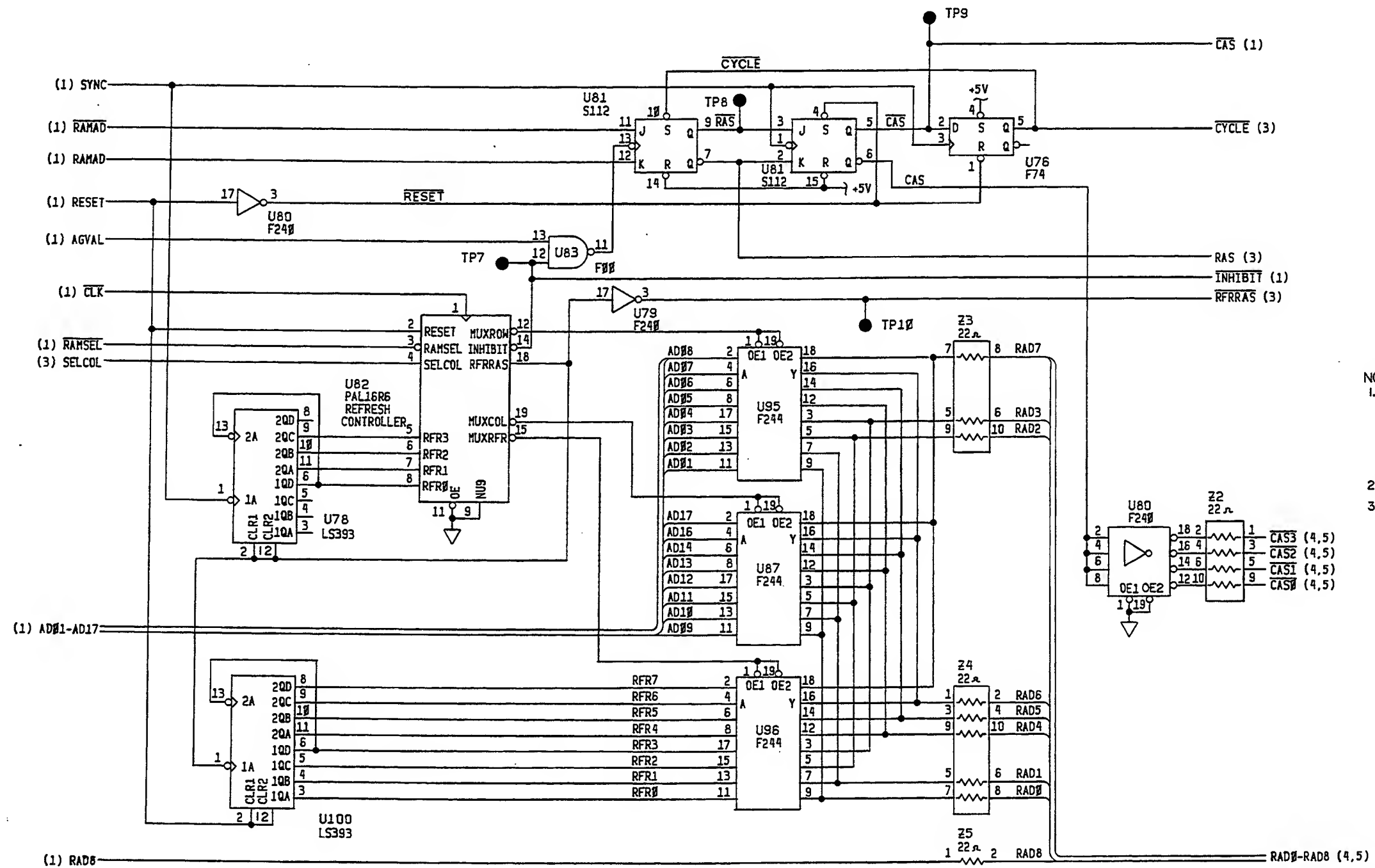


Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)



- NOTES: UNLESS OTHERWISE SPECIFIED
1. +5V AND GND ARE NOT SHOWN EXPLICITLY FOR MOST CHIPS; PIN 14, 16, 20, OR 24 ARE ASSUMED TO BE +5V. PIN 7, 8, 10, OR 12 ARE ASSUMED TO BE GND. OTHER SUPPLY VOLTAGES ARE SHOWN EXPLICITLY.
 2. ALL RESISTANCE IS IN OHMS.
 3. ALL CAPACITANCE IS IN MICROFARADS.

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Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)

Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)

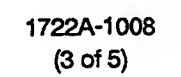
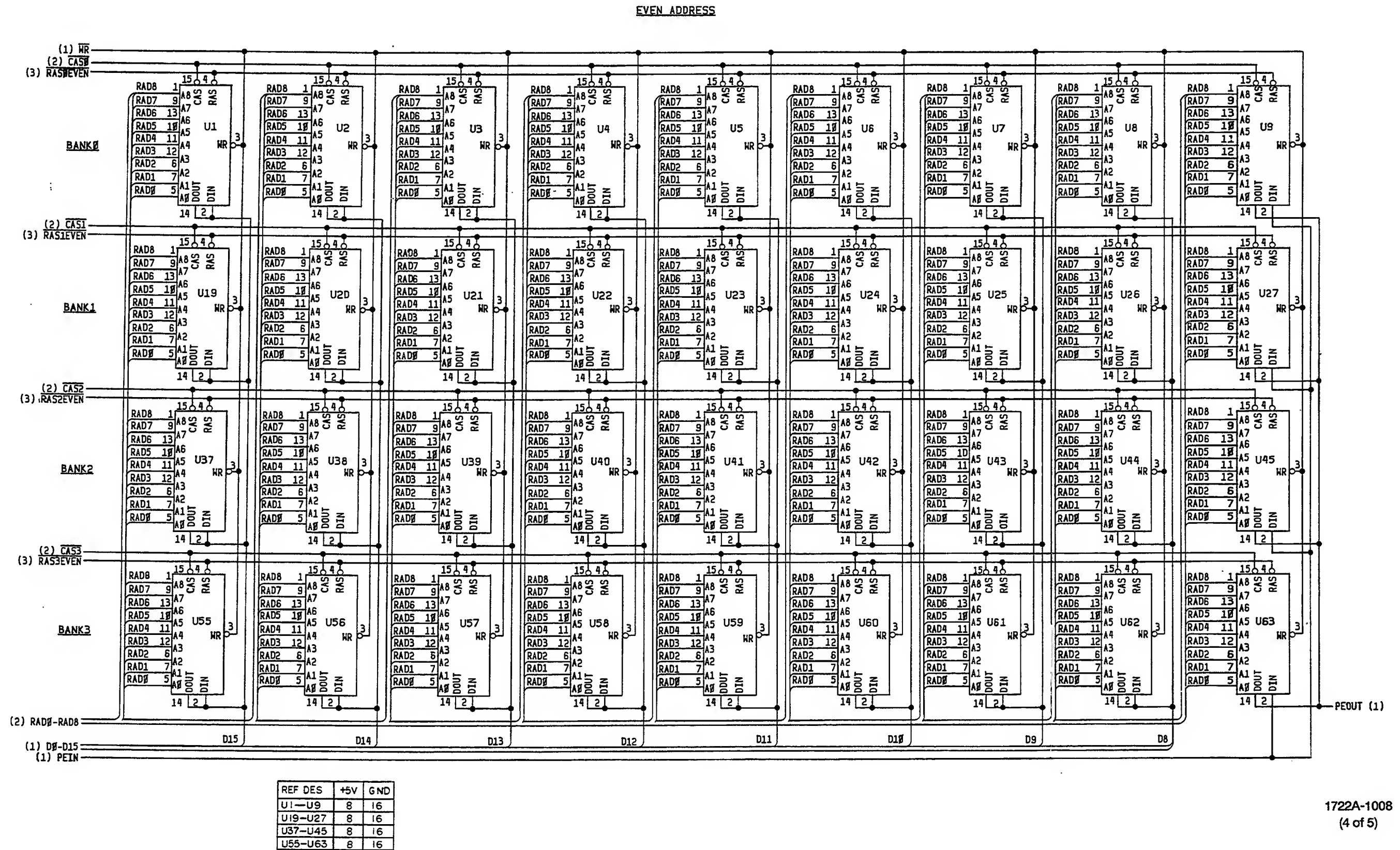


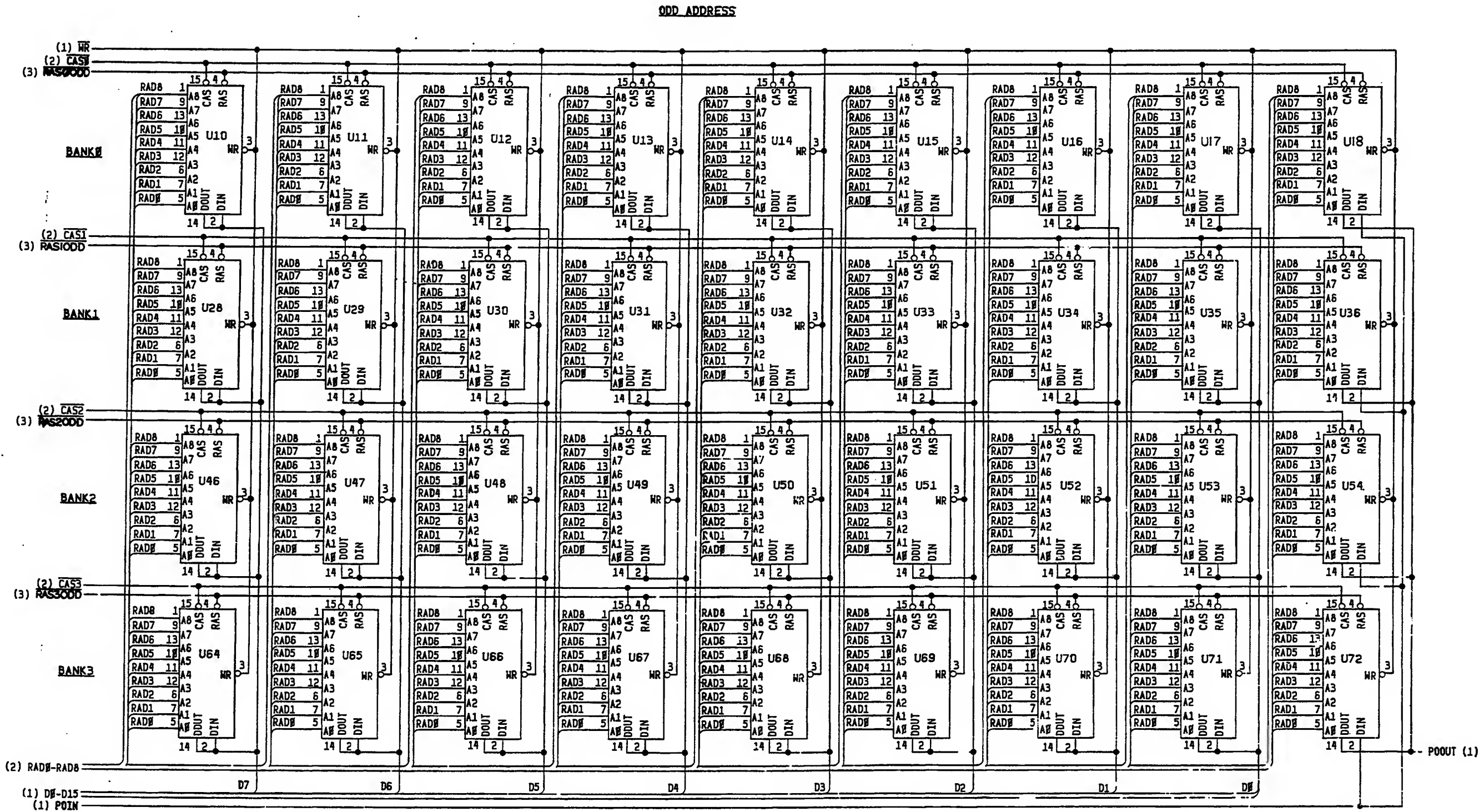
Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)



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Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)

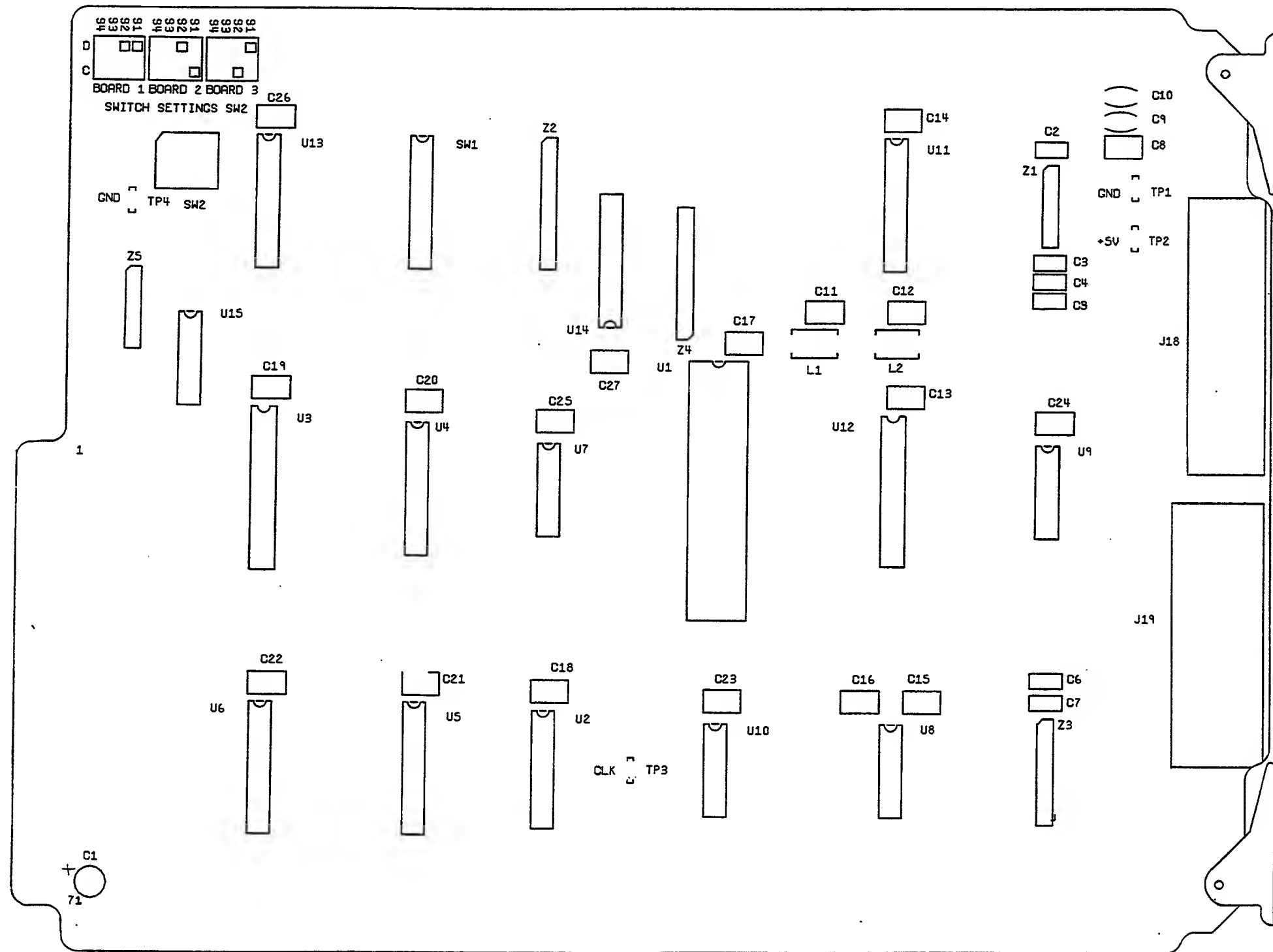
Schematic Diagrams



REF DES	+5V	GND
U10-U18	8	16
U28-U36	8	16
U46-U54	8	16
U64-U72	8	16

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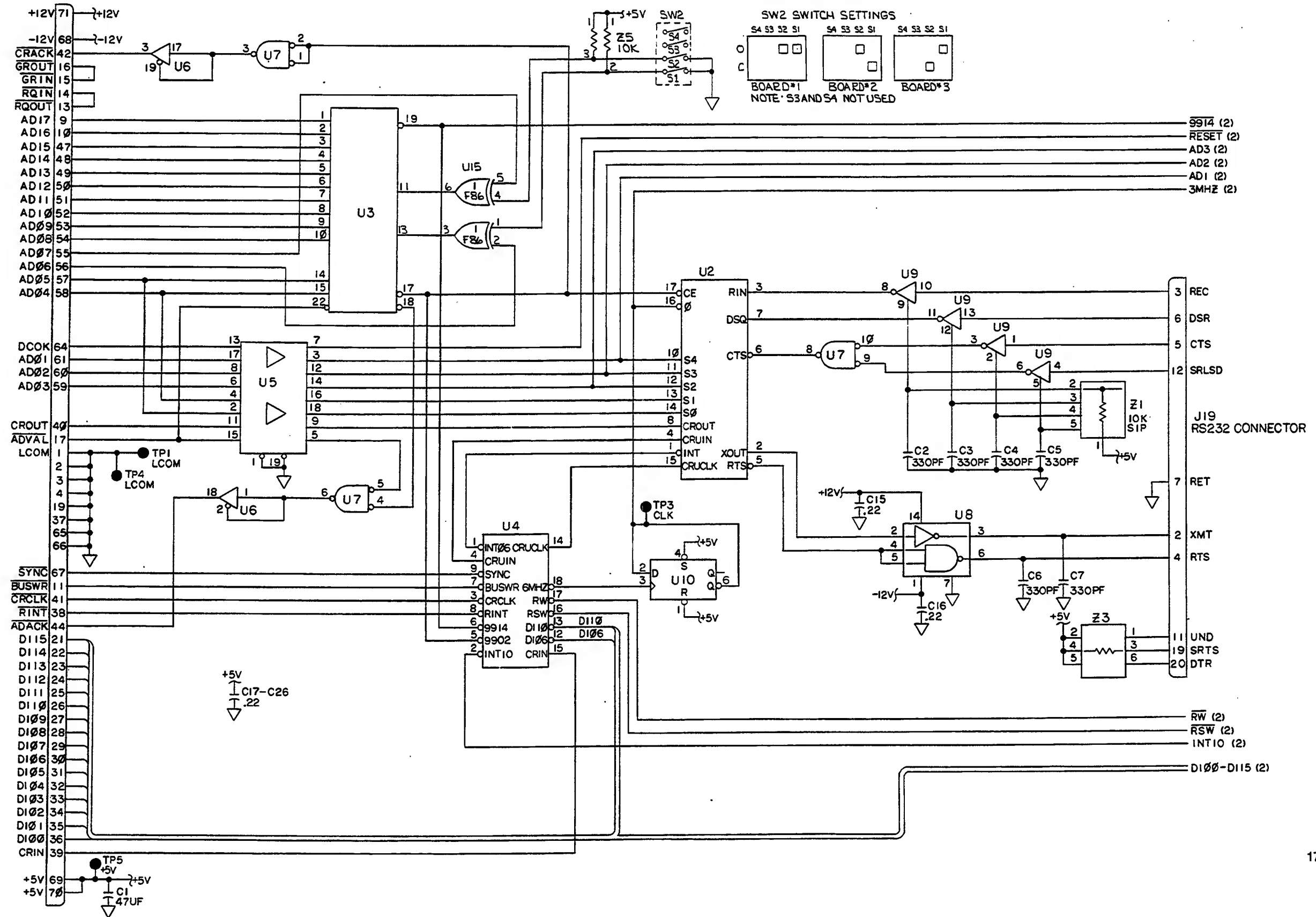
Figure 5-8. 006, 007, 016, 017 Expansion Modules (cont)



1722A-1609

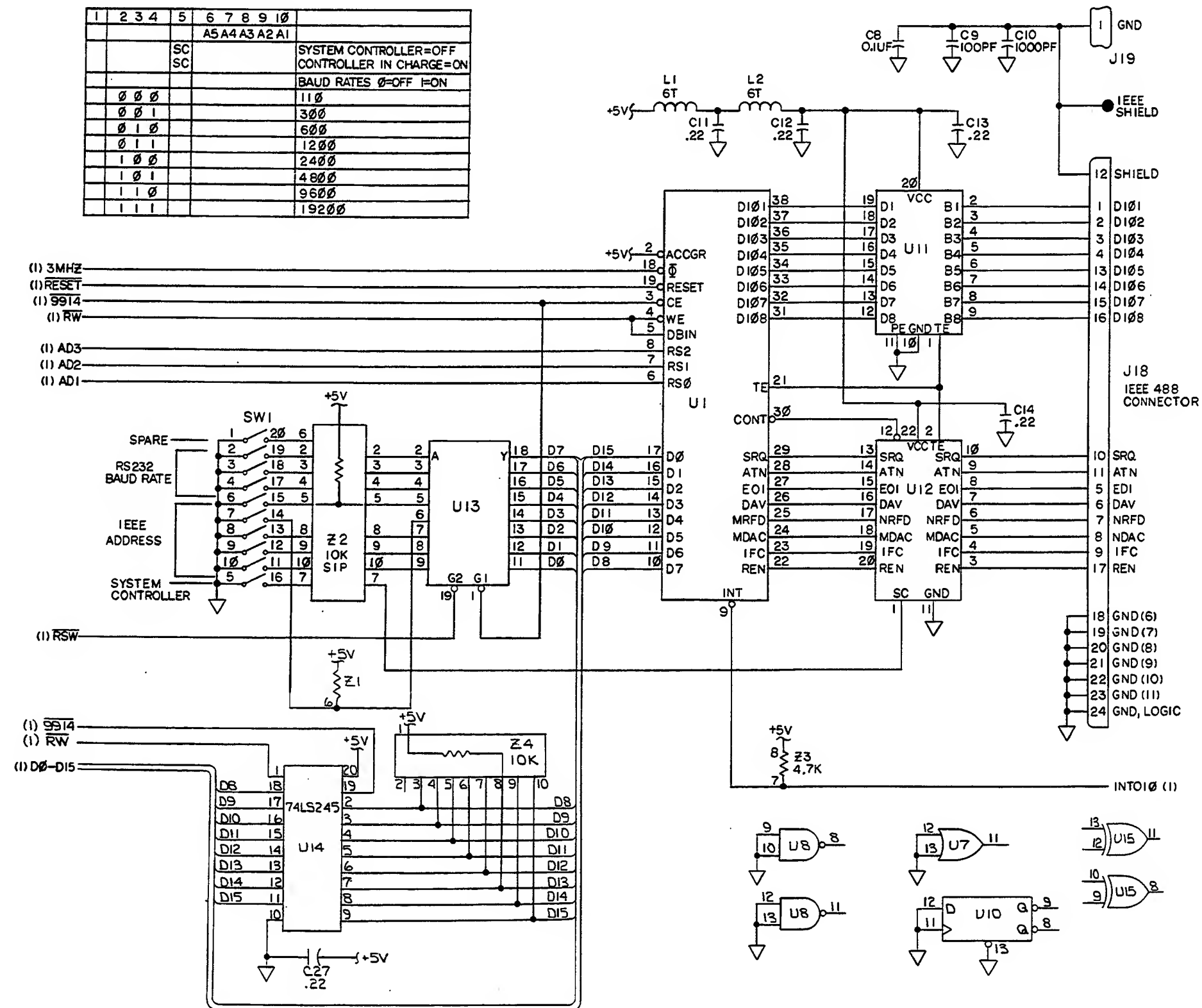
Figure 5-9. 008 IEEE-488/RS-232-C Interface Module

Schematic Diagrams



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Figure 5-9. 008 IEEE-488/RS-232-C Interface Module (cont)



NOTES: UNLESS OTHERWISE SPECIFIED

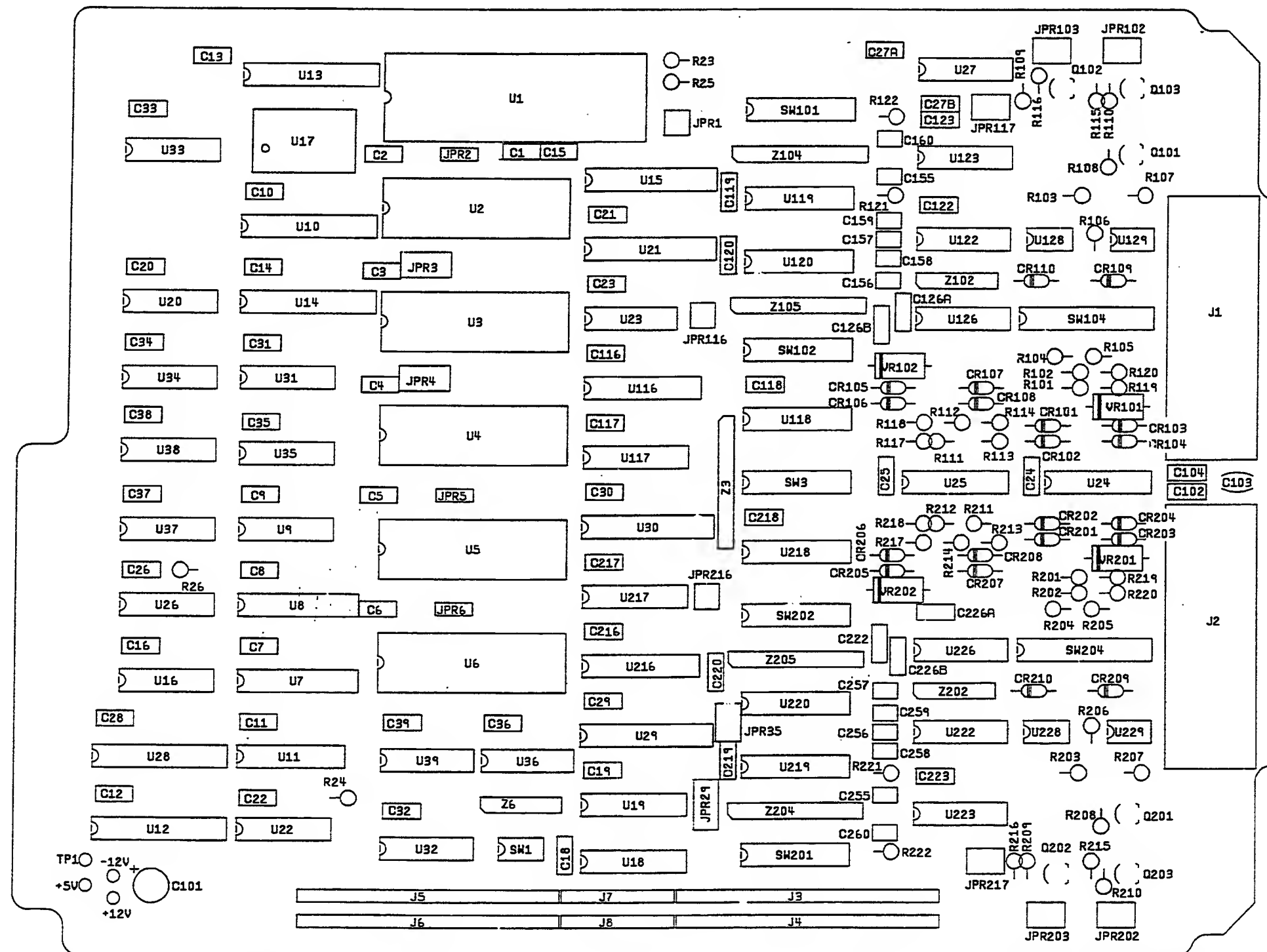
1. ALL RESISTANCE IS IN OHMS.
2. ALL CAPACITANCE IS IN MICROFARADS.

REF DES	+5V	GND	TYPE
U1	40	20	TMS9914A
U2	18	9	9902A
U3	24	12	16L6
U4	20	10	16L8
U5	20	10	F244
U6	20	10	F244
U7	14	7	F32
U9	14	7	1489
U10	14	7	LS74
U11	20	10	75160A
U12	22	11	75162A
U13	20	10	LS541
U14	20	10	LS245
U15	14	7	F86

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Figure 5-9. 008 IEEE-488/RS-232-C Interface Module (cont)

Schematic Diagrams



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Figure 5-10. 009 Dual Serial Interface Module

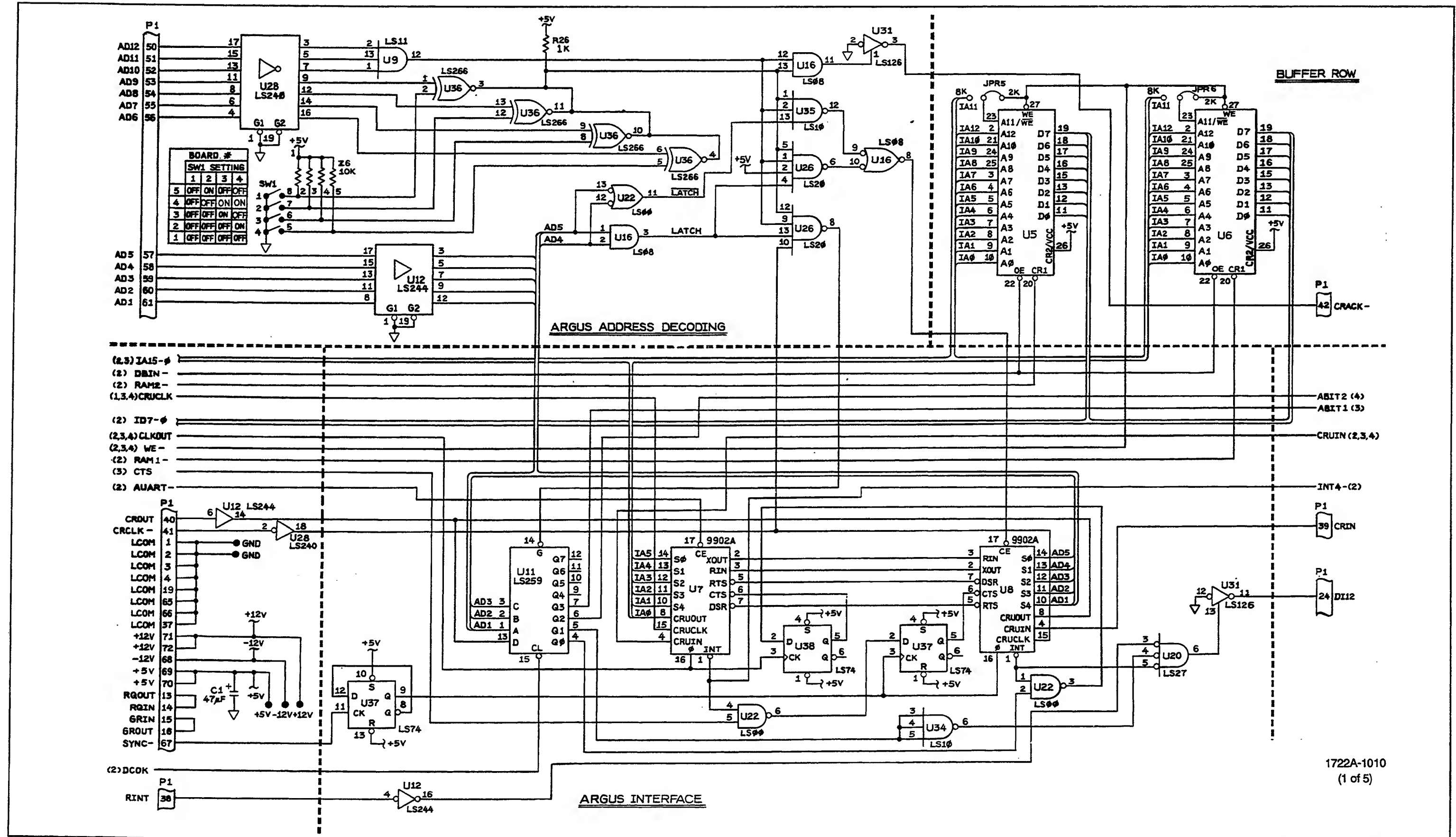


Figure 5-10. 009 Dual Serial Interface Module (cont)

Schematic Diagrams

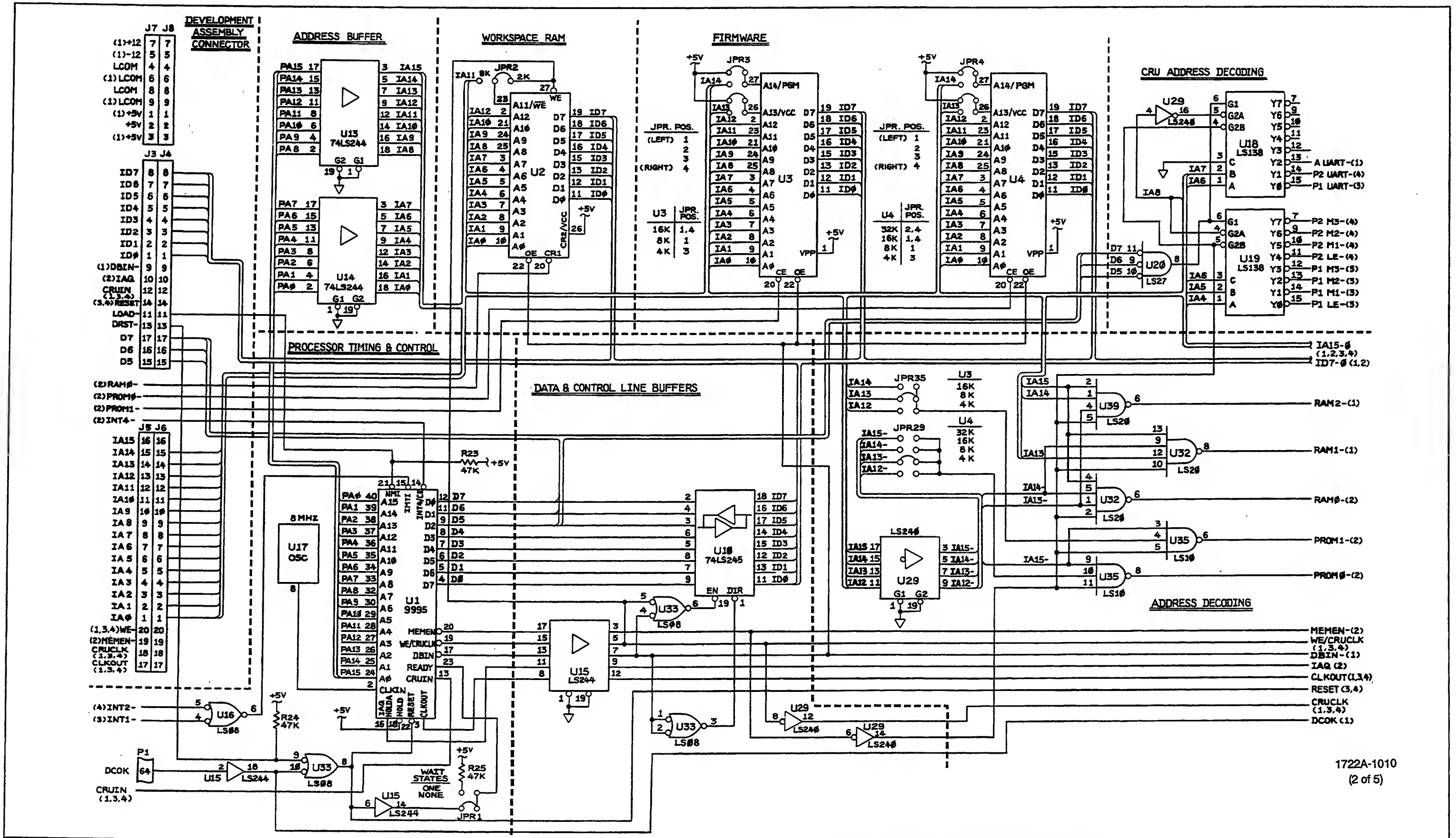


Figure 5-10. 009 Dual Serial Interface Module (cont)

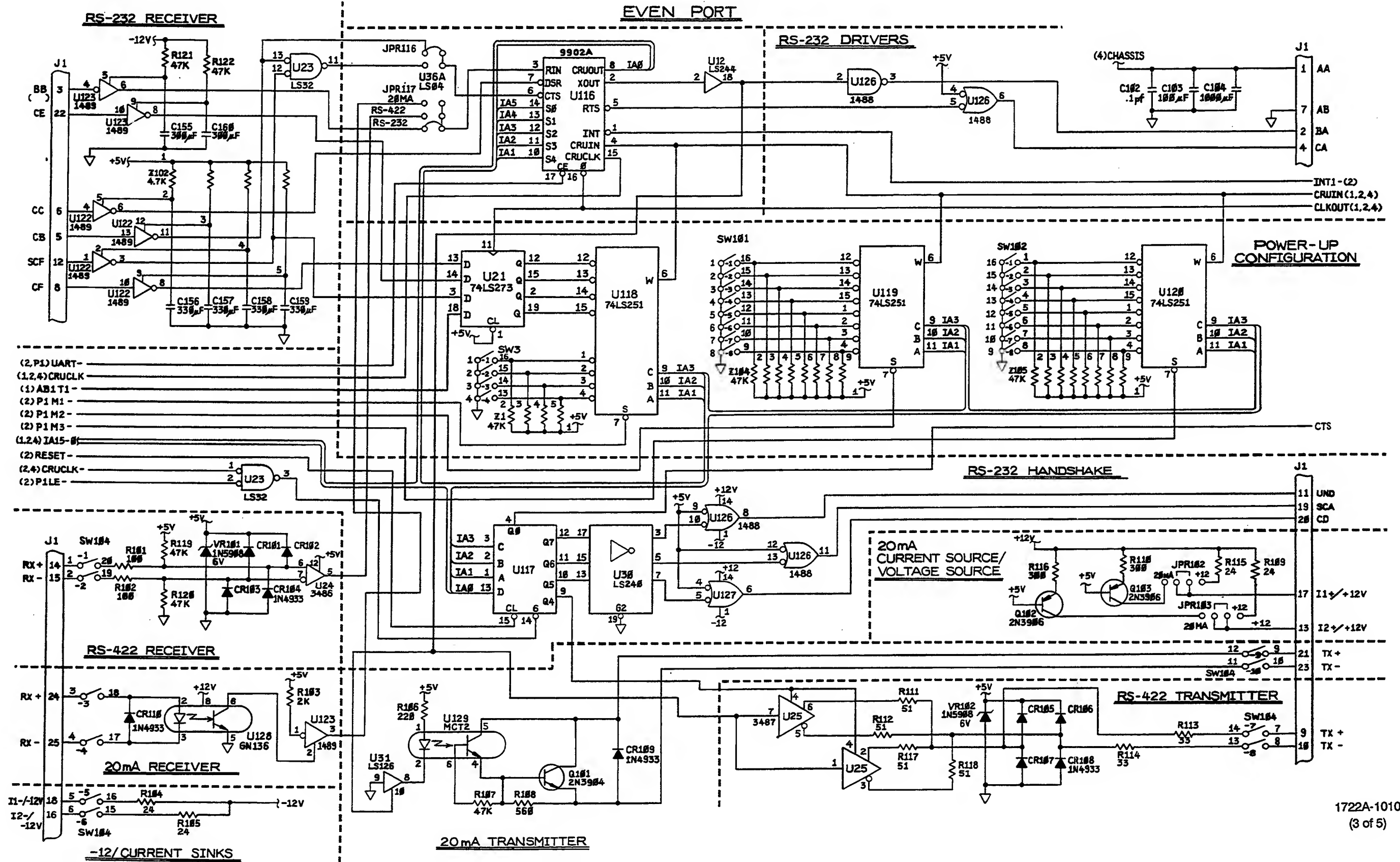
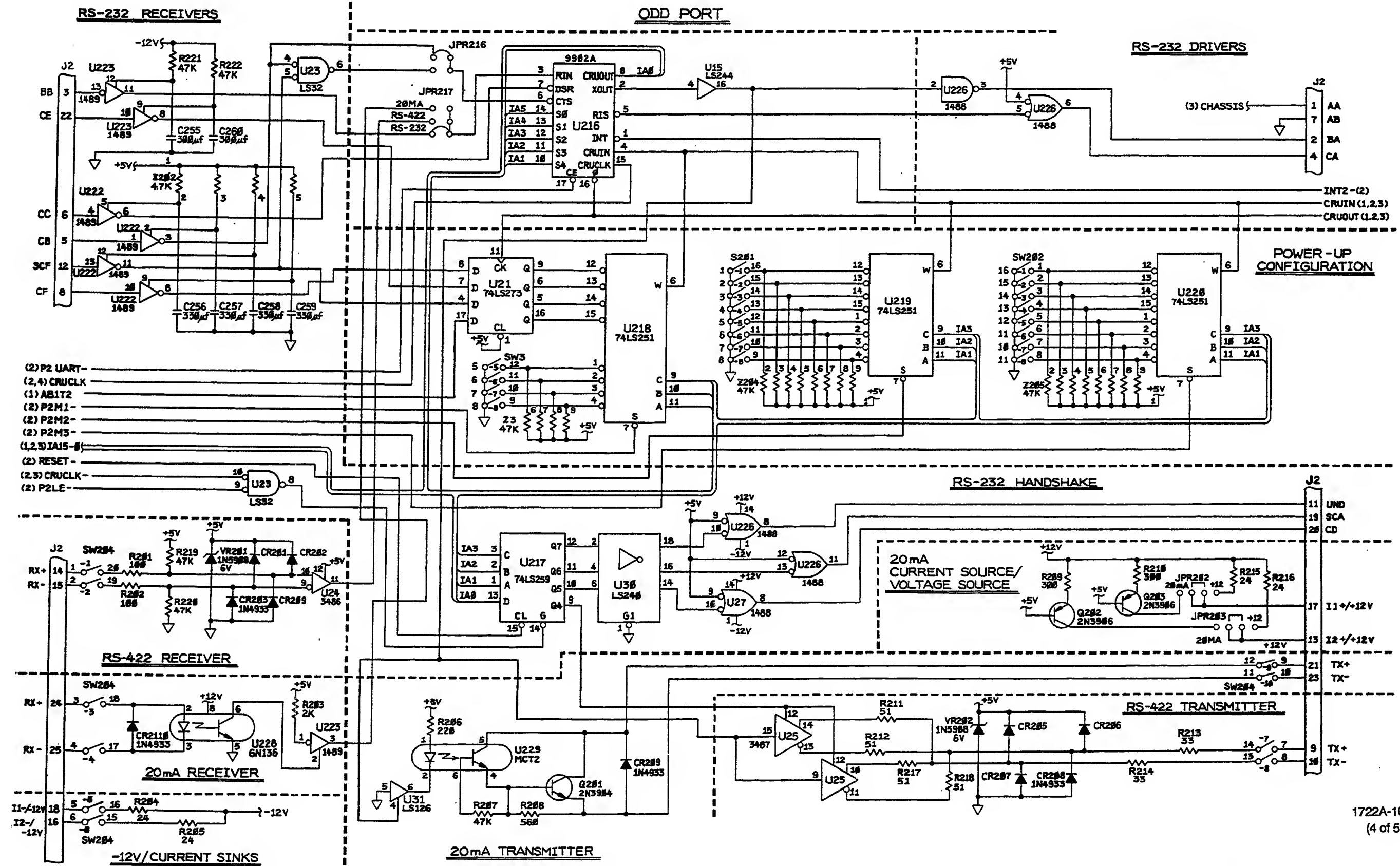


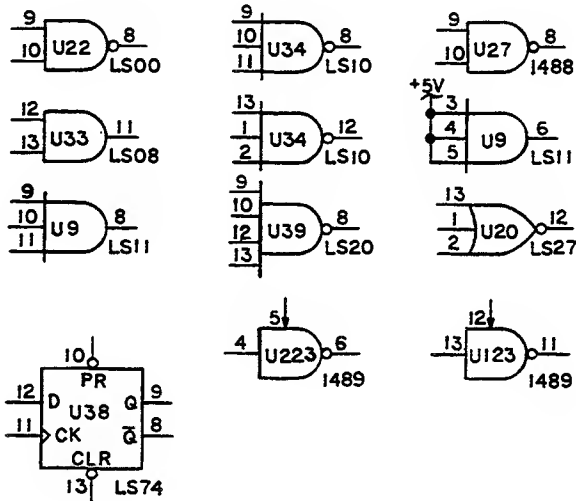
Figure 5-10. 009 Dual Serial Interface Module (cont)

Schematic Diagrams



NOTES: UNLESS OTHERWISE SPECIFIED

- 1. ALL CAPACITANCES ARE IN MICROFARADS.
- 2. ALL RESISTANCES ARE IN OHMS.
- 3. ALL RESISTORS ARE 1/4W, 5%.
- 4.
- 5.
- 6.
- 7. +S AND GND ARE NOT SHOWN EXPLICITLY FOR MOST CHIPS. FOR CHIPS WITHOUT +S AND GND, PINS 14,16,20... ARE ASSUMED TO BE +S, AND PINS 7,8,10... ARE ASSUMED TO BE GROUND. OTHER SUPPLY VOLTAGES ARE SHOWN EXPLICITLY.
- 8.



REFERENCE DESIGNATORS USED

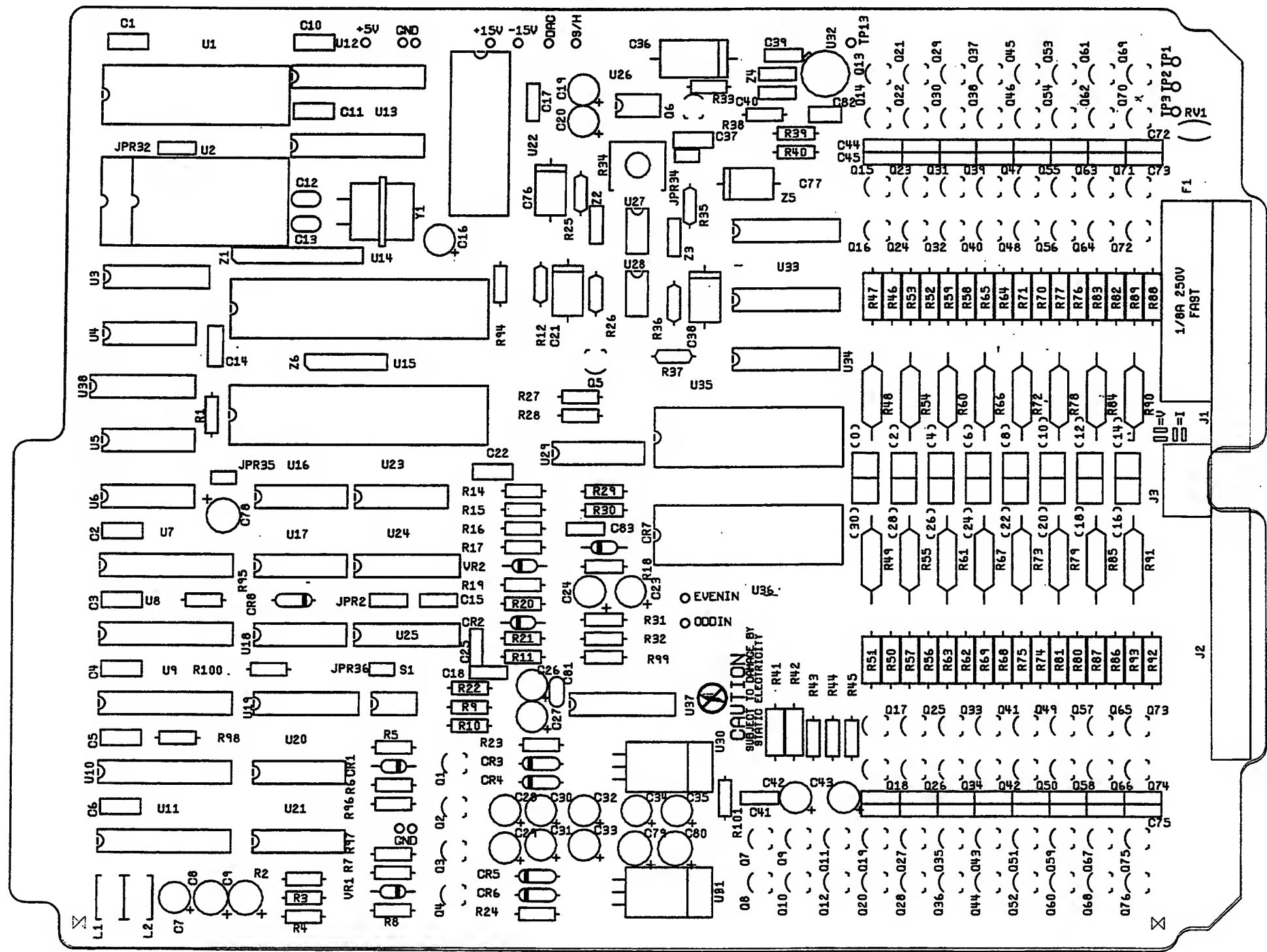
FIRST USED	LAST USED	UNUSED
U1	U229	U40-U115 U121, U124, U125, U127, U130-U215, U221, U224, U225, U227
Q1	Q203	Q1-Q100, Q104-Q200
CR1	CR210	CR1-CR100 CR111-CR200
VR1	VR202	VR1-VR100 VR103-VR200
R1	R222	R1-R22 R27-R100 R123-R200
C1	C260	C17, C40-C100 C105-C115, C121, C124, C125 C127-C154, C161-C215, C221, C224, C225, C227-C254
Z1	Z205	Z1, Z2, Z4, Z5, Z7-Z101, Z103, Z106-Z201, Z203
SW1	SW204	SW2, SW4-SW100, SW103, SW105- SW200, SW203
JPR1	JPR217	JPR30-JPR34, JPR36-JPR101, JPR104-JPR115, JPR118-JPR201, JPR204-JPR215, JPR7-JPR28
J1	J8	
P1	P1	
TP1	TP4	

POWER-GROUND CONNECTIONS

REF. DES.	TYPE	-12V	+12V	GND
U27, U126, U226	LM1488	1	14	7
U128, U228	6N136	—	8	S

REF. DES.	TYPE	+5V	GND
U1	TMS9995	10	31
U2, U5, U6	2064P	28	14
U3, U4	2764D	28	14
U7, U8 U116, U216	9902A	18	9
U9	74LS11	14	7
U10	74LS245	20	10
U11, U117 U217	74LS259	16	8
U12, U13, U14, U15	74LS244	20	10
U16, U33	74LS08	14	7
U17	OSC	4	2
U18, U19	74LS138	16	8
U20	74LS27	14	7
U21	74LS273	20	10
U22	74LS00	14	7
U23	74LS32	14	7
U24	MC3486	16	8
U25	MC3487	16	8
U26, U32, U39	74LS20	14	7
U28, U29, U30	74LS240	20	10
U31	74LS126	14	7
U34, U35	74LS10	14	7
U36	74LS266	14	7
U37, U38	74LS74	14	7
U118, U119, U120, U218, U219, U220	74LS251	16	8
U122, U222, U123, U223	MC1489	14	7

Figure 5-10. 009 Dual Serial Interface Module (cont)



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Figure 5-11. 010 A/D Converter Module

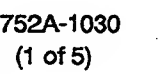
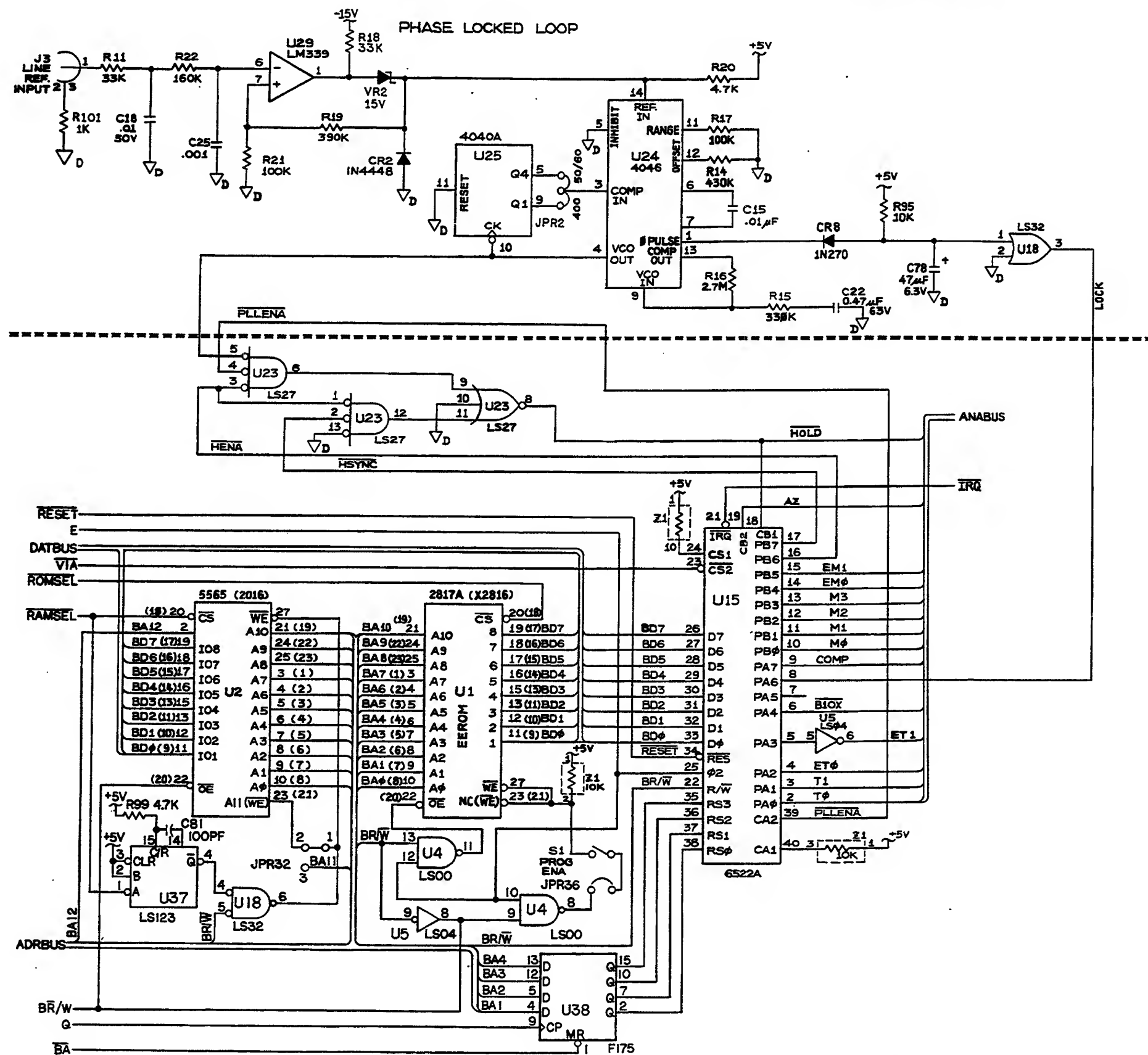


Figure 5-11. 010 A/D Converter Module (cont)

Schematic Diagrams

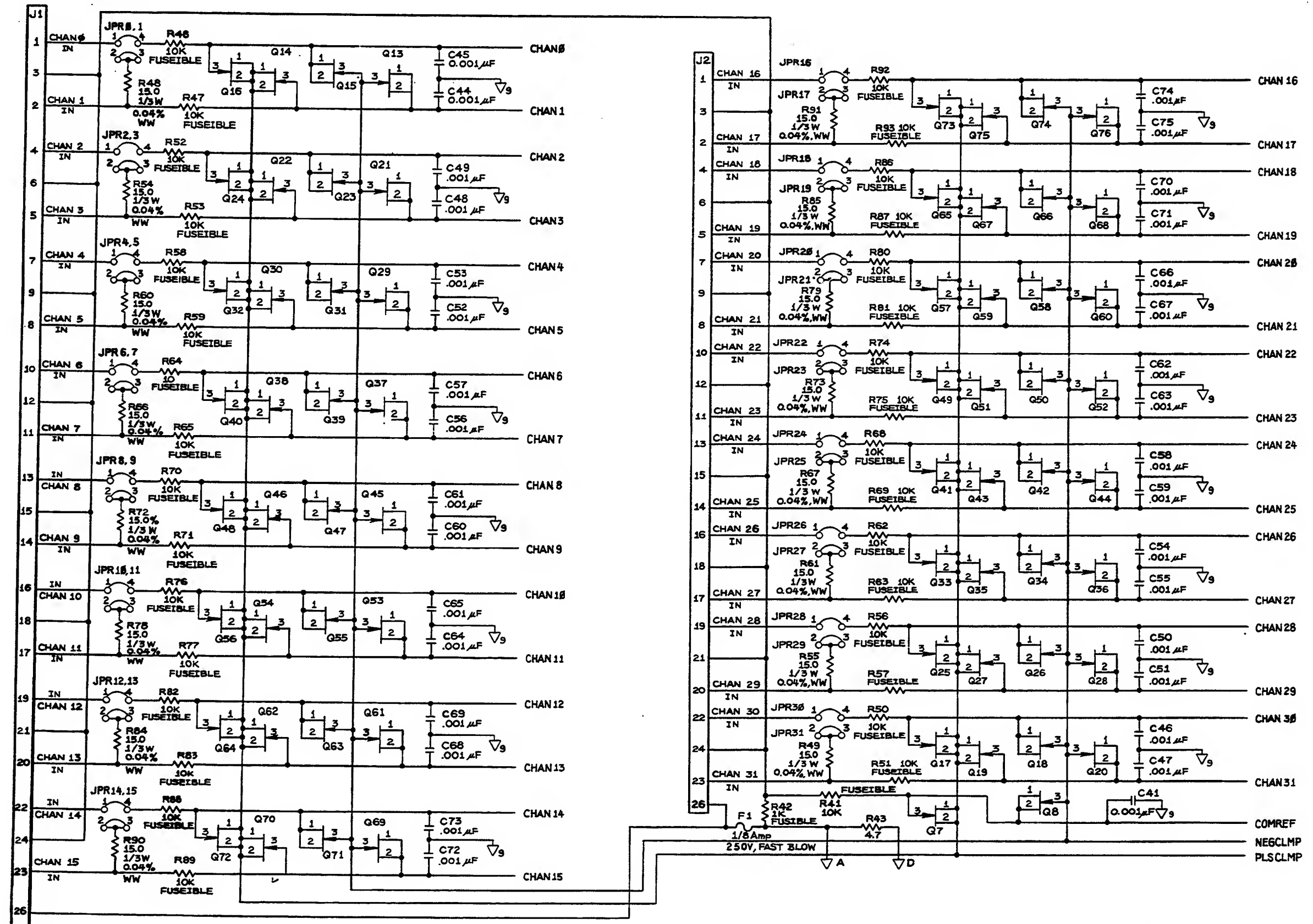


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTANCES ARE IN OHMS.
3. ALL RESISTORS ARE 1/4W, 5%.
- 4.
- 5.
- 6.
7. +5 AND GND ARE NOT SHOWN EXPLICITLY FOR MOST CHIPS. OTHER SUPPLY VOLTAGES ARE SHOWN EXPLICITLY.
8. FOR LAST USED REF DES AND POWER/GROUND TABLE SEE SHEET 5 OF 5.
9. FOR SPARES SEE SHEET 4 OF 5.

1752A-1030
(2 of 5)

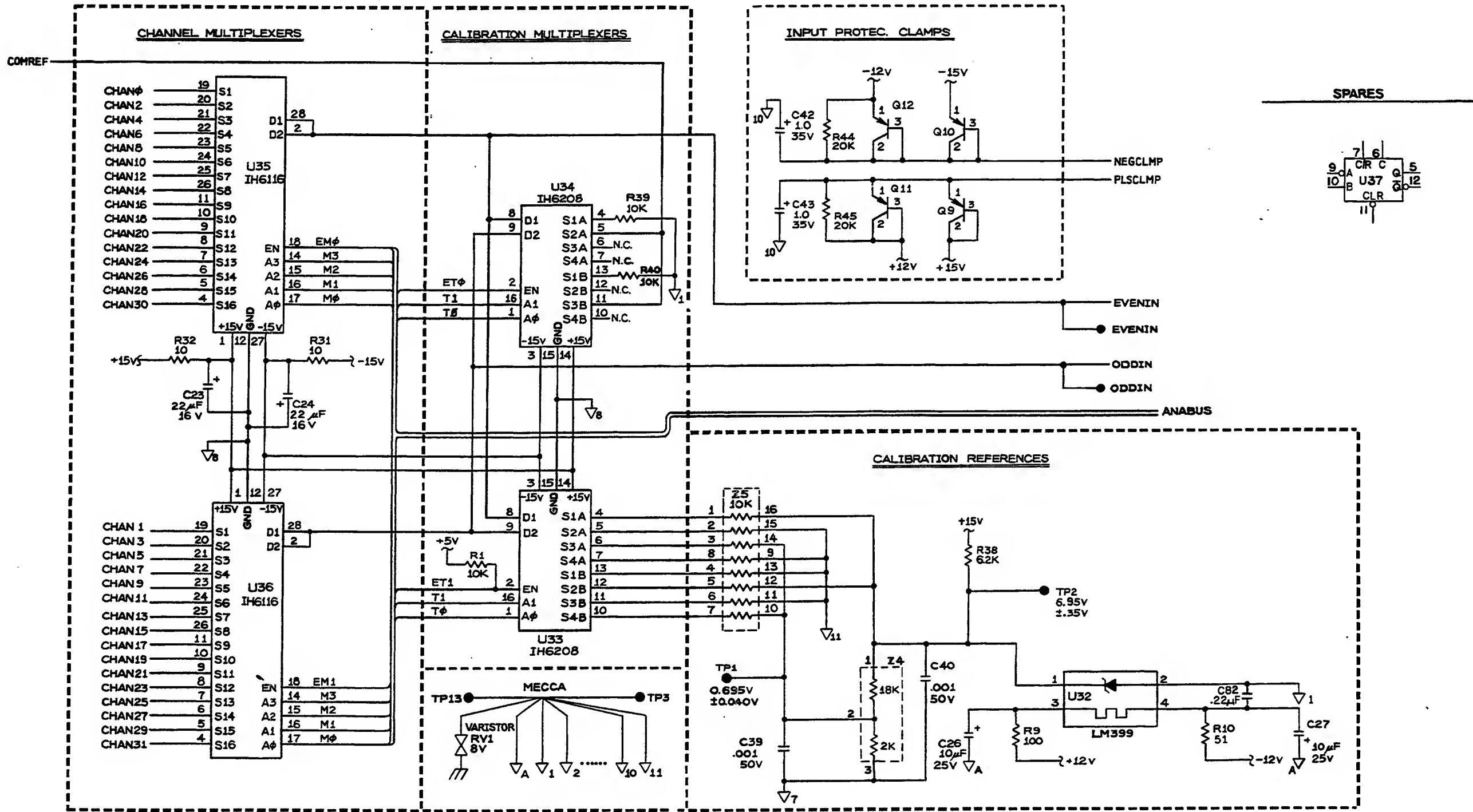
Figure 5-11. 010 A/D Converter Module (cont)



1752A-1030
(3 of 5)

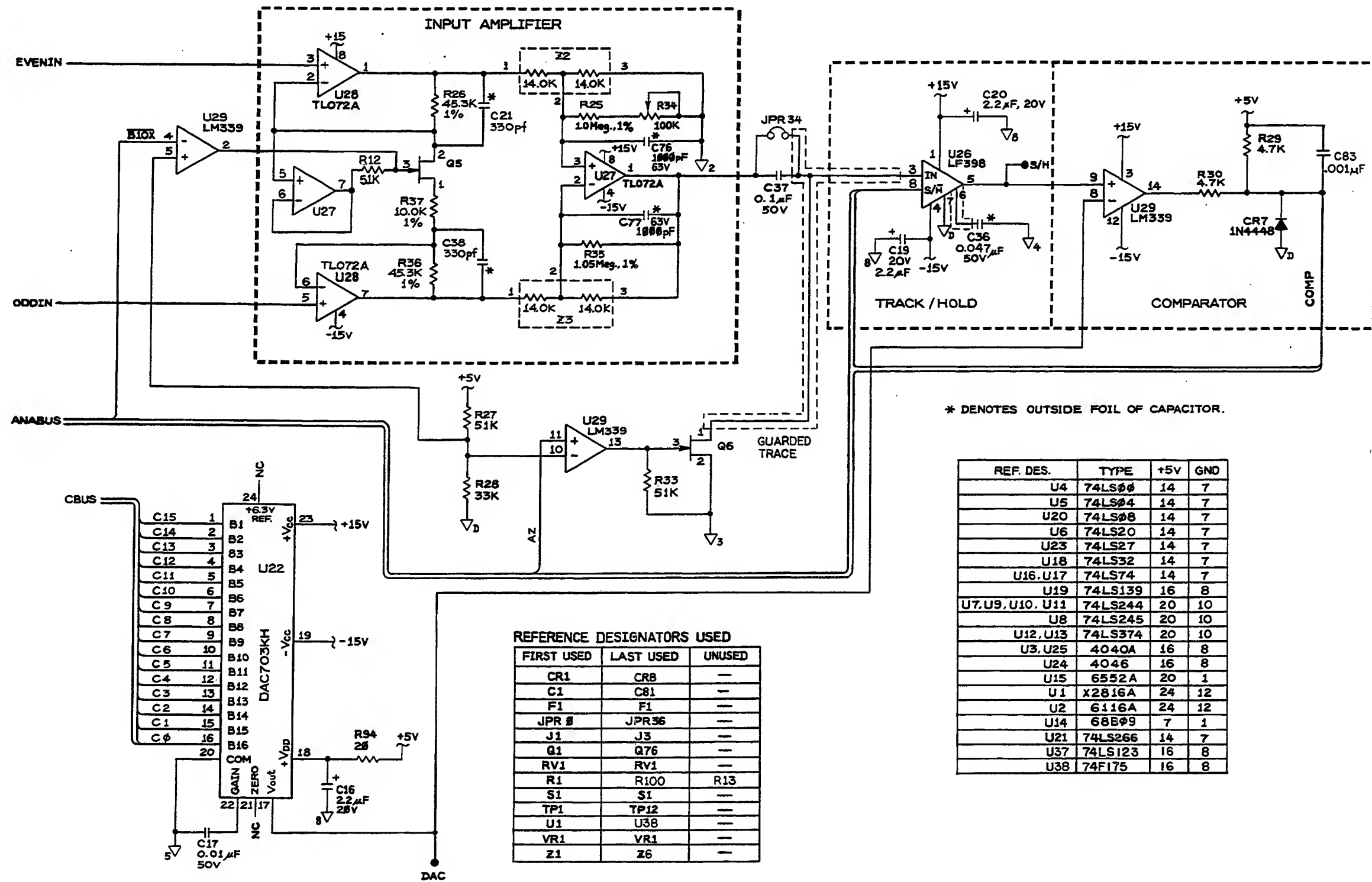
Figure 5-11. 010 A/D Converter Module (cont)

Schematic Diagrams



1752A-1030
(4 of 5)

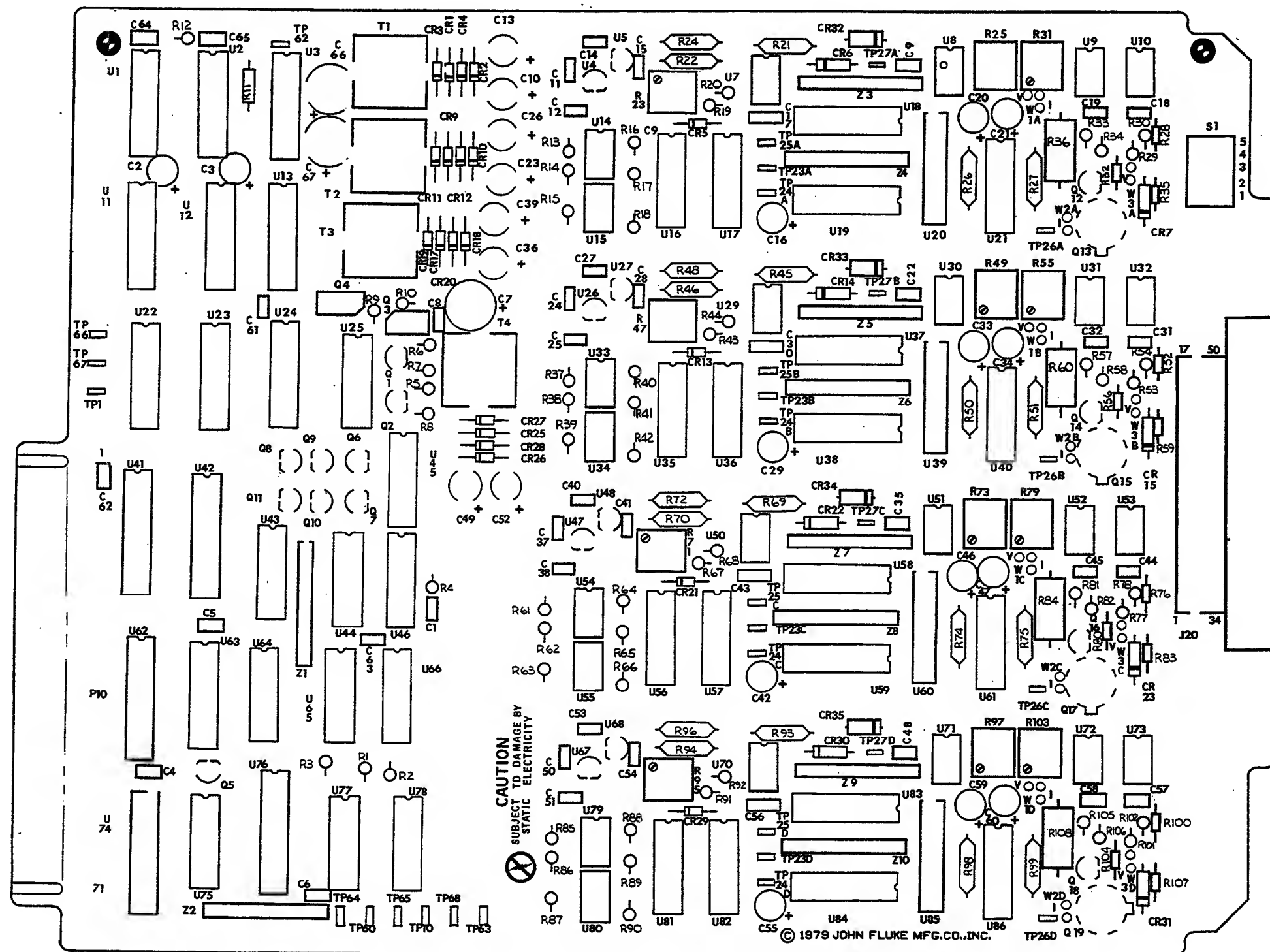
Figure 5-11. 010 A/D Converter Module (cont)



1752A-1030
(5 of 5)

Figure 5-11. 010 A/D Converter Module (cont)

Schematic Diagrams



2400A-1609

Figure 5-12. 011 Analog Output Module

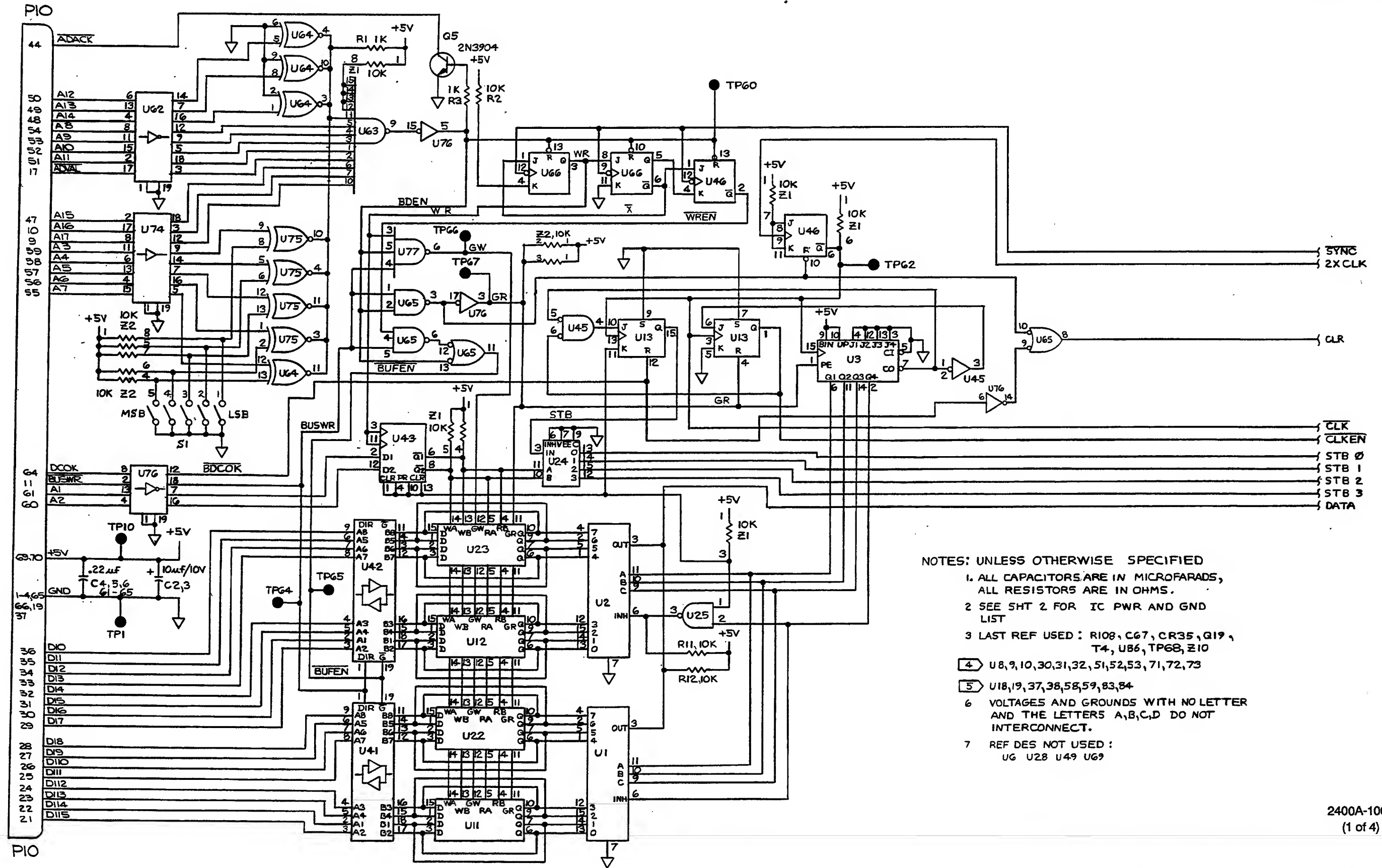
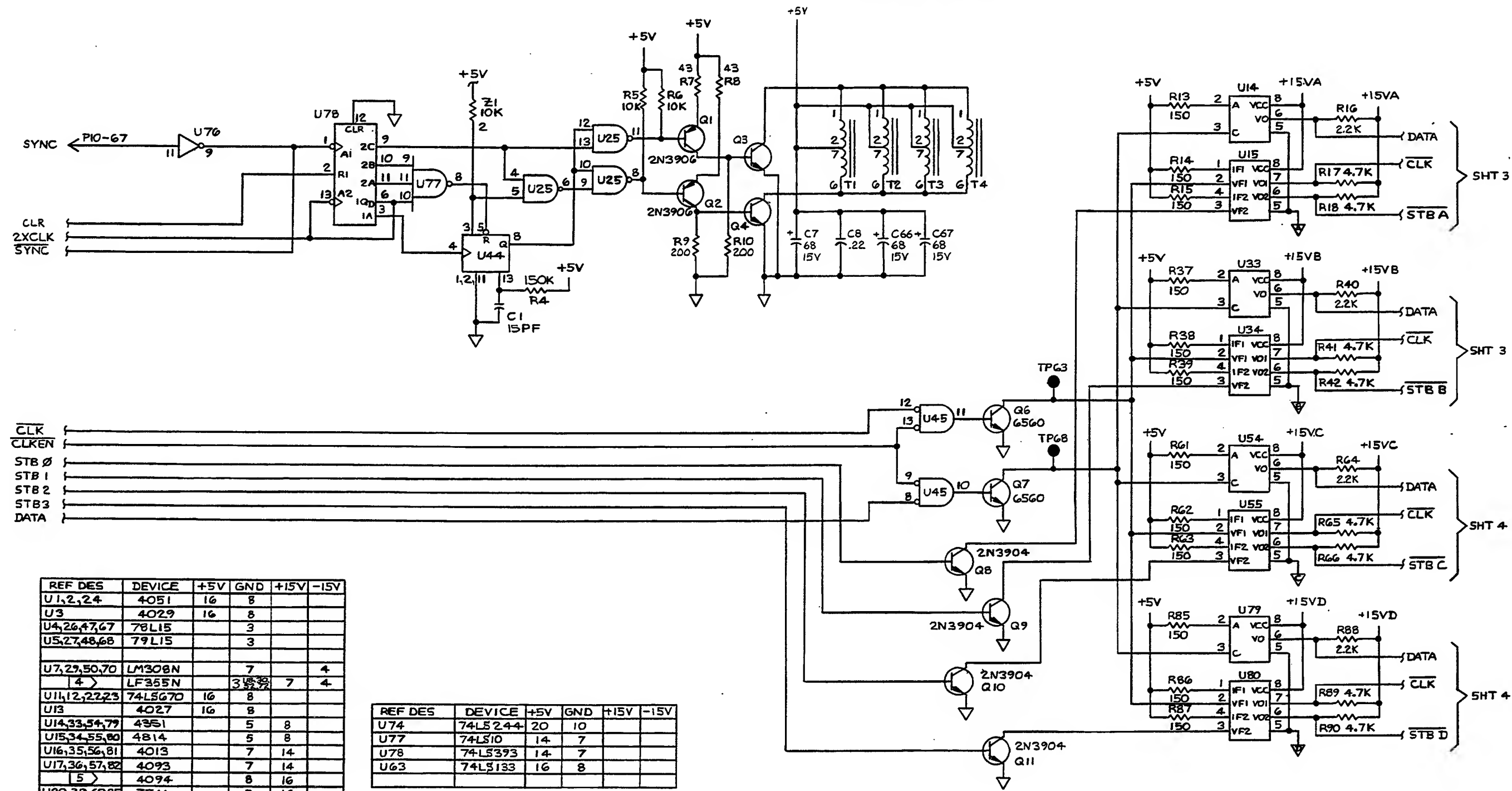


Figure 5-12. 011 Analog Output Module (cont)

Schematic Diagrams



2400A-1009
(2 of 4)

Figure 5-12. 011 Analog Output Module (cont)

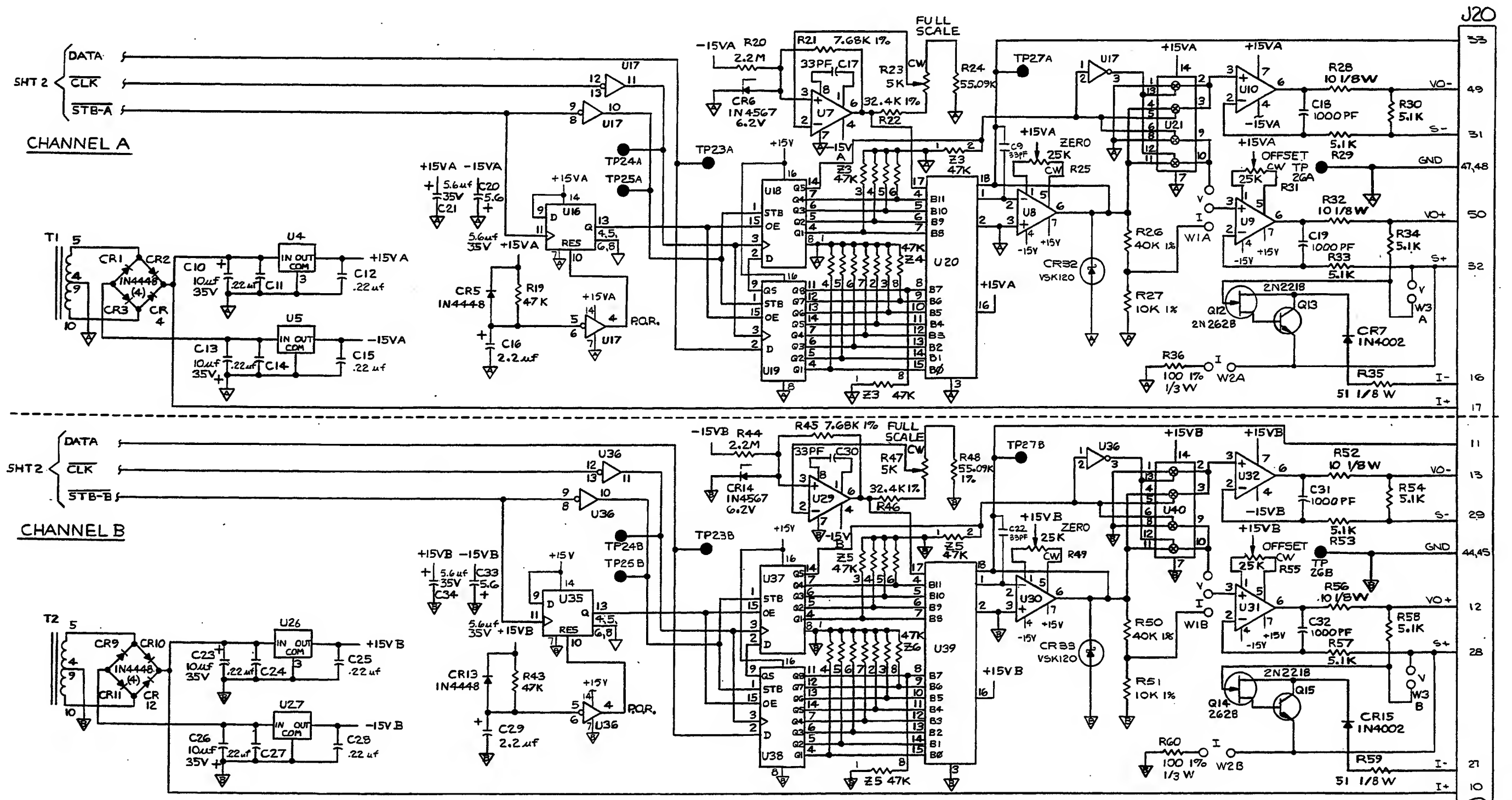
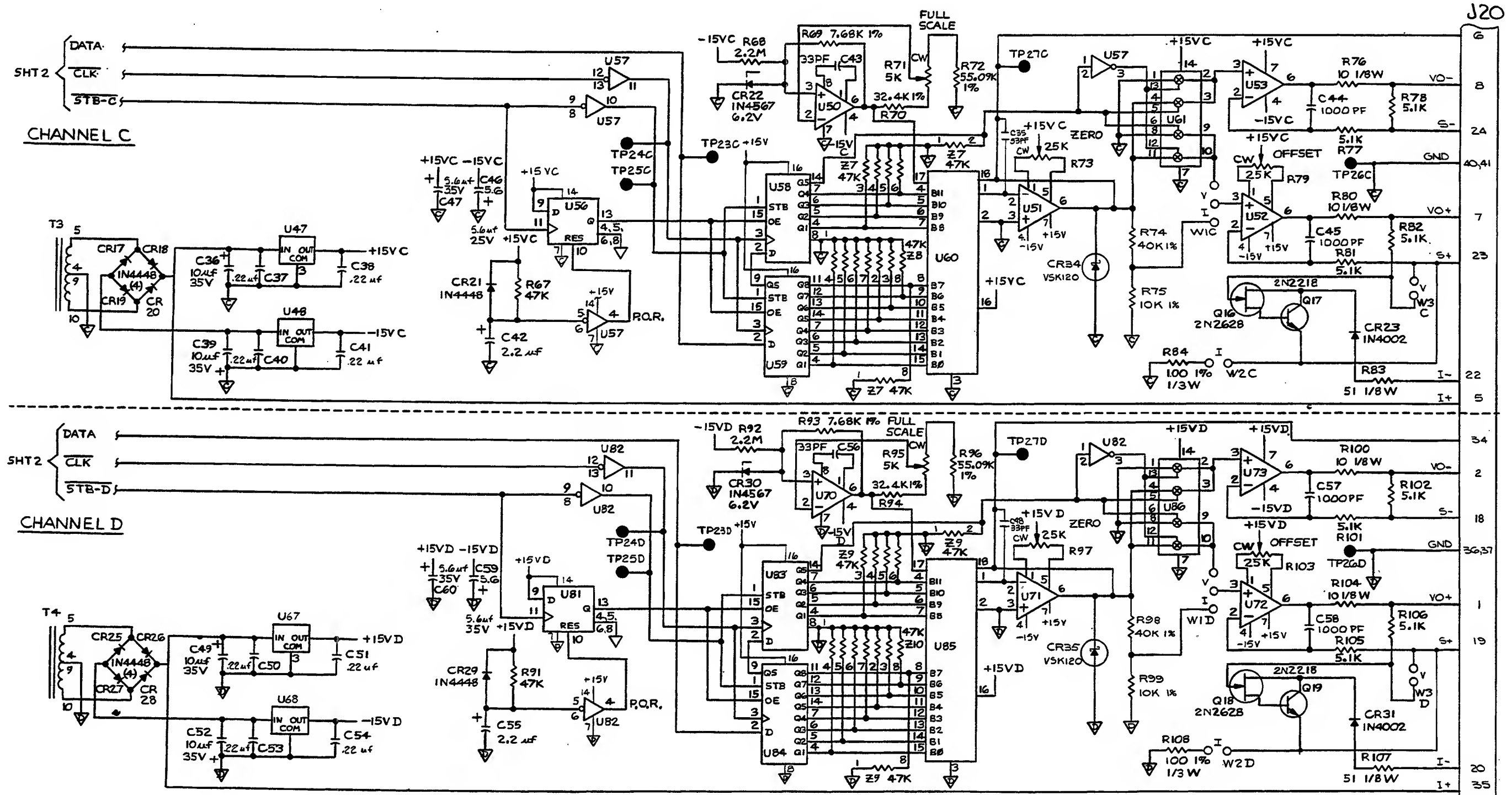


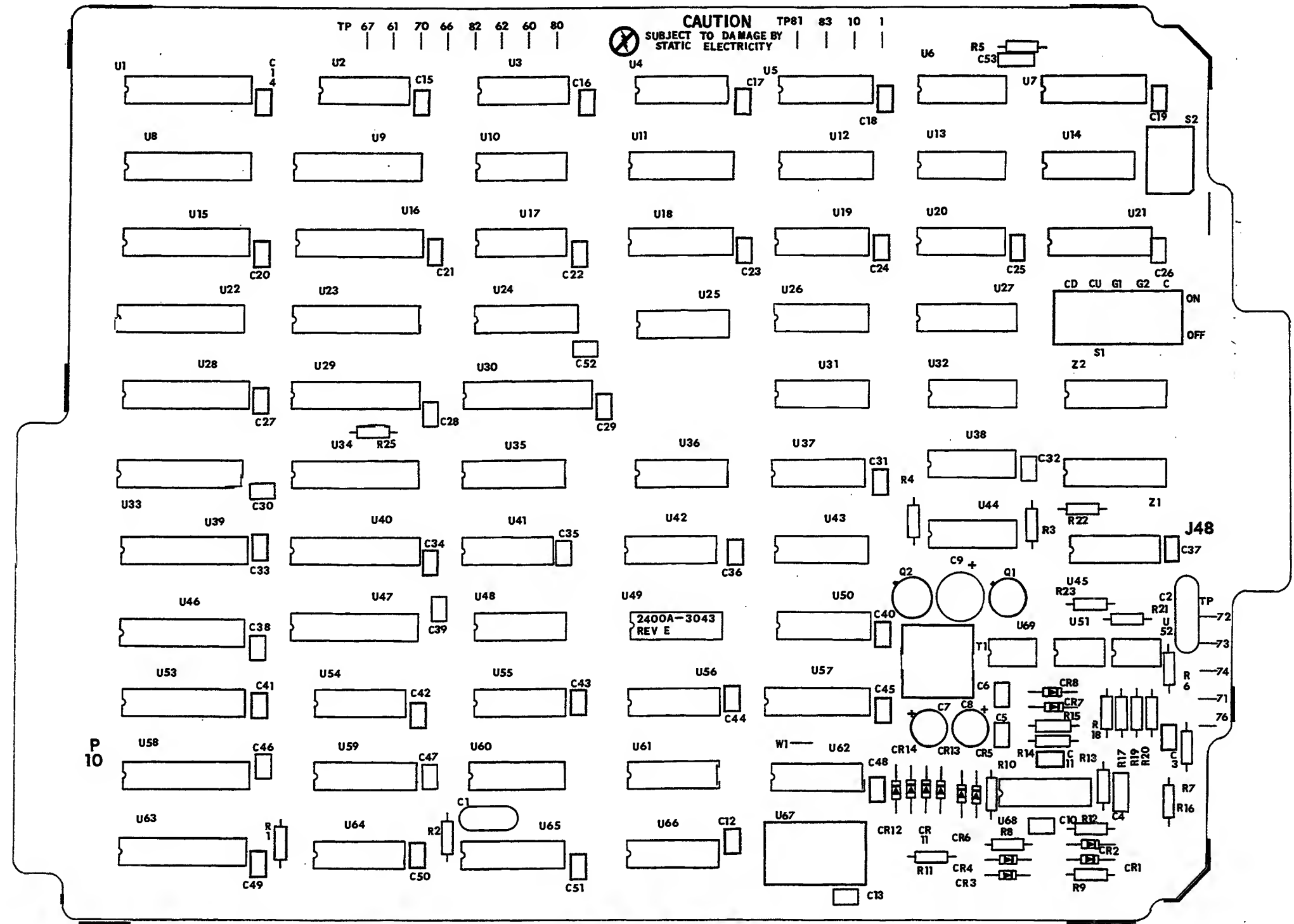
Figure 5-12. 011 Analog Output Module (cont)

Schematic Diagrams



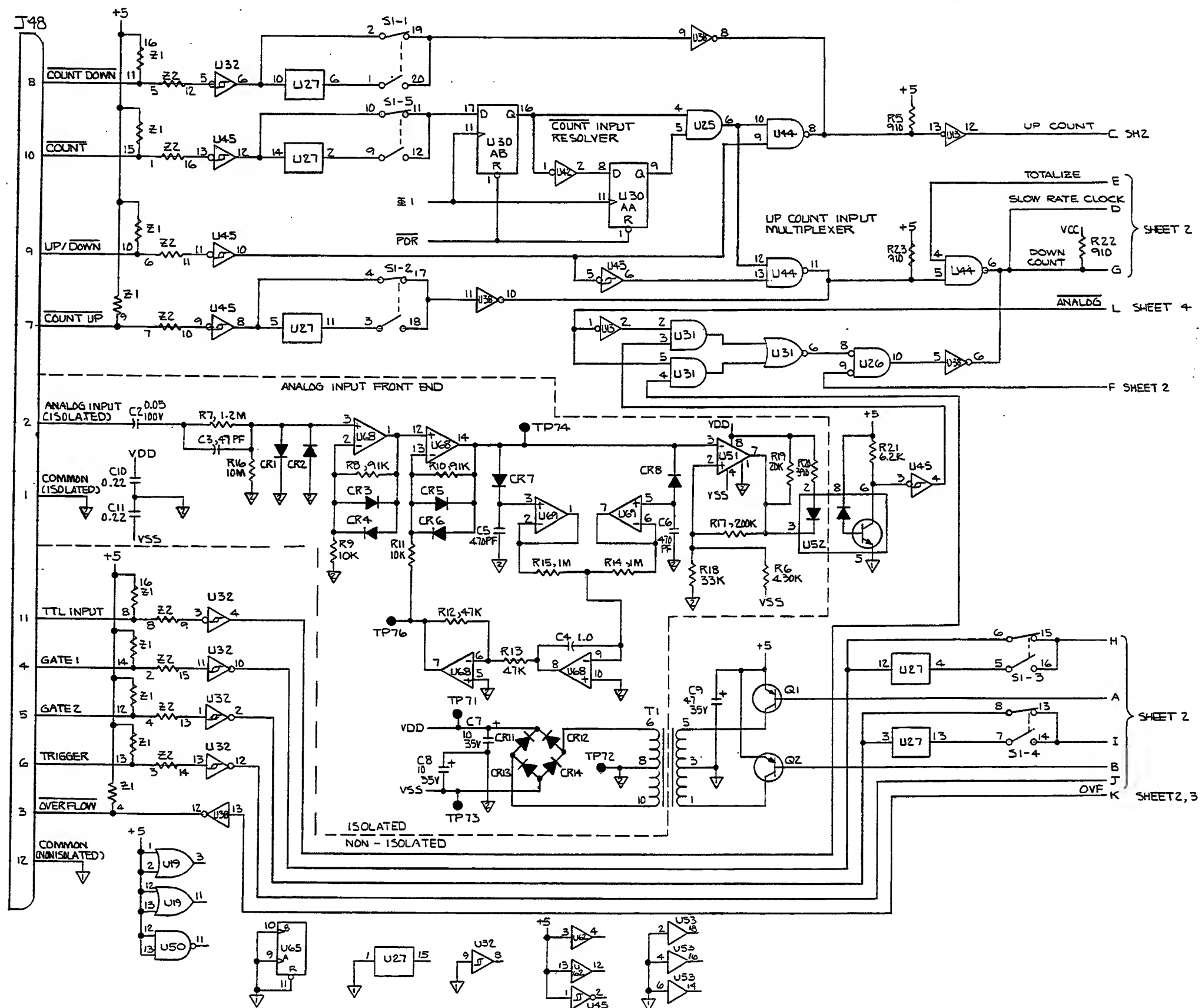
2400A-1009
(4 of 4)

Figure 5-12. 011 Analog Output Module (cont)



2400A-1643

Figure 5-13. 012 Counter/Totalizer Module



- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE ARE IN OHMS AND ALL CAPACITANCE ARE IN MICROFARADS.
 2. ALL RESISTORS ARE 1/4W, 5%.
 3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

I.C.	VCC	V
U1	20	10
U2	14	7
U3	14	7
U4	14	7
U5	14	7
U6	14	7
U7	14	7
U8	14	7
U9	14	7
U10	14	7
U11	14	7
U12	14	7
U13	14	7
U14	14	7
U15	14	7
U16	14	7
U17	14	7
U18	14	7
U19	14	7
U20	14	7
U21	14	7
U22	14	7
U23	14	7
U24	14	7
U25	14	7
U26	14	7
U27	14	7
U28	14	7
U29	14	7
U30	14	7
U31	14	7
U32	14	7
U33	14	7
U34	14	7
U35	14	7

I.C.	VCC	V
U36	14	7
U37	14	7
U38	14	7
U39	14	7
U40	14	7
U41	14	7
U42	14	7
U43	14	7
U44	14	7
U45	14	7
U46	14	7
U47	14	7
U48	14	7
U49	14	7
U50	14	7
U51	14	7
U52	14	7
U53	14	7
U54	14	7
U55	14	7
U56	14	7
U57	14	7
U58	14	7
U59	14	7
U60	14	7
U61	14	7
U62	14	7
U63	14	7
U64	14	7
U65	14	7
U66	14	7
U67	14	7
U68	14	7
U69	14	7
U70	14	7

I.C.	VDD	V	VSS
U51	8	1	4
U68	8	1	4
U69	8	1	4

LAST USED	NOT USED
U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U70	CR9, 10

2400A-1043
(1 of 4)

Figure 5-13. 012 Counter/Totalizer Module (cont)

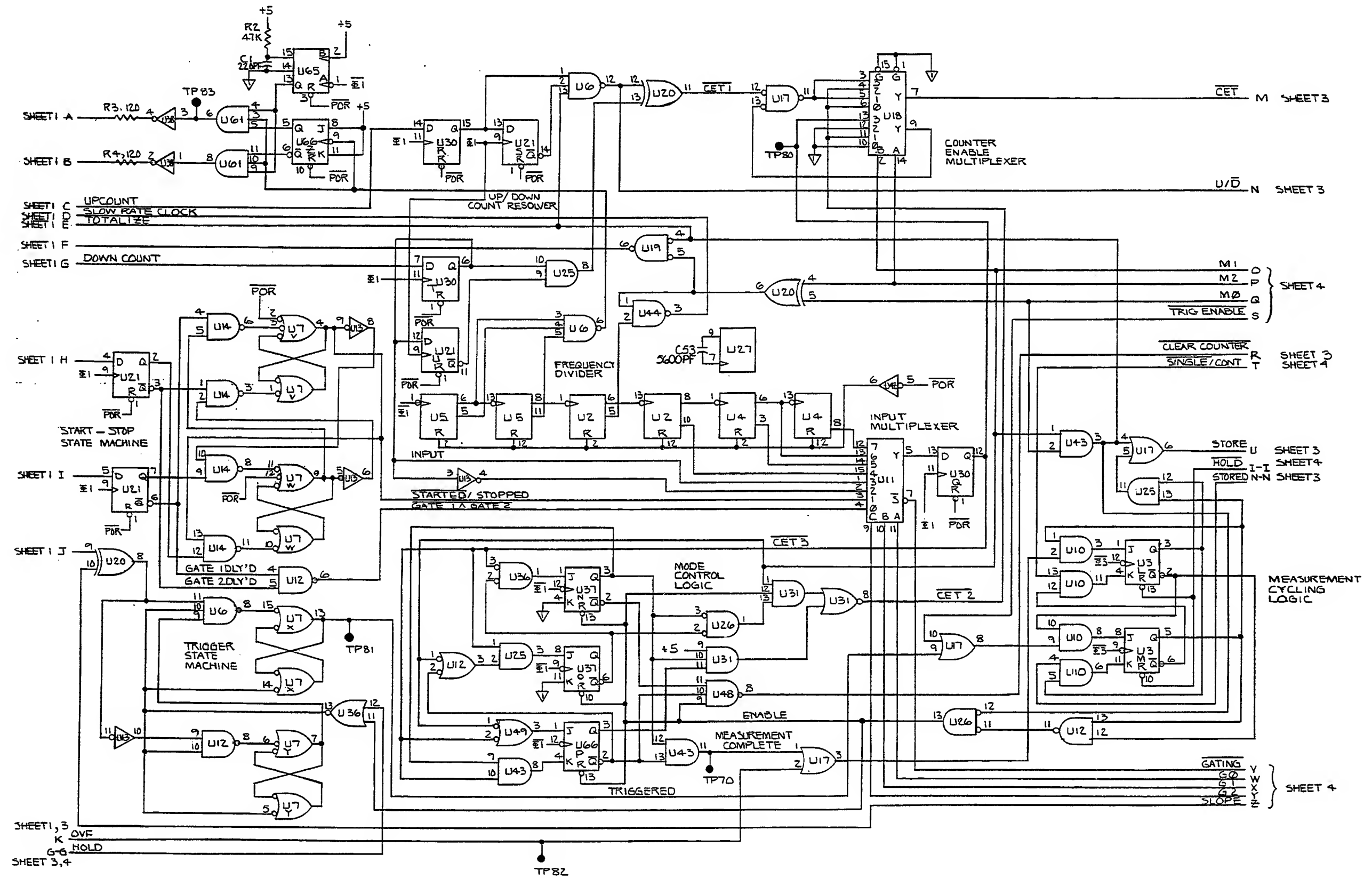
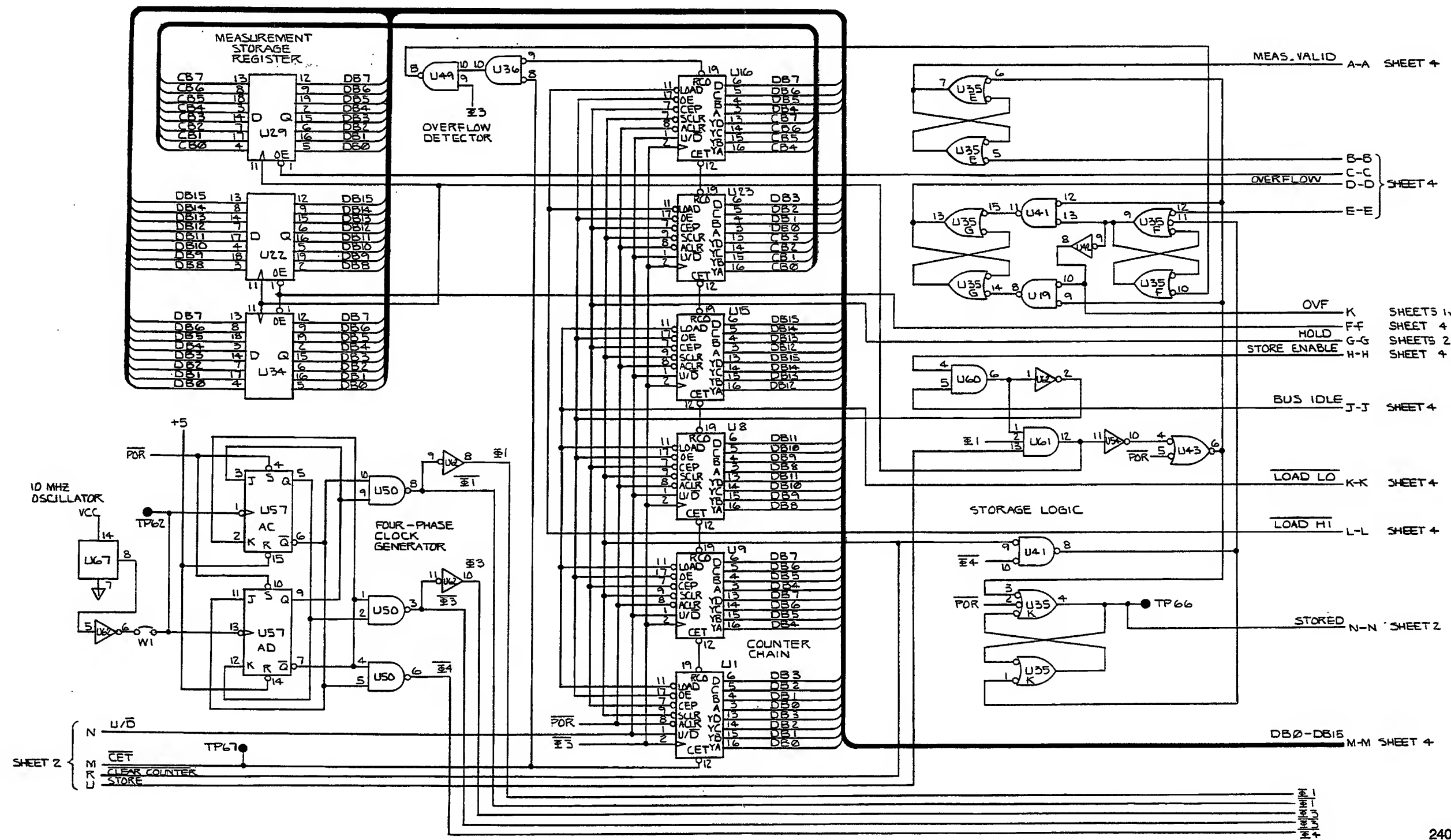


Figure 5-13. 012 Counter/Totalizer Module (cont)



2400A-1043
(2 of 4)

Figure 5-13. 012 Counter/Totalizer Module (cont)

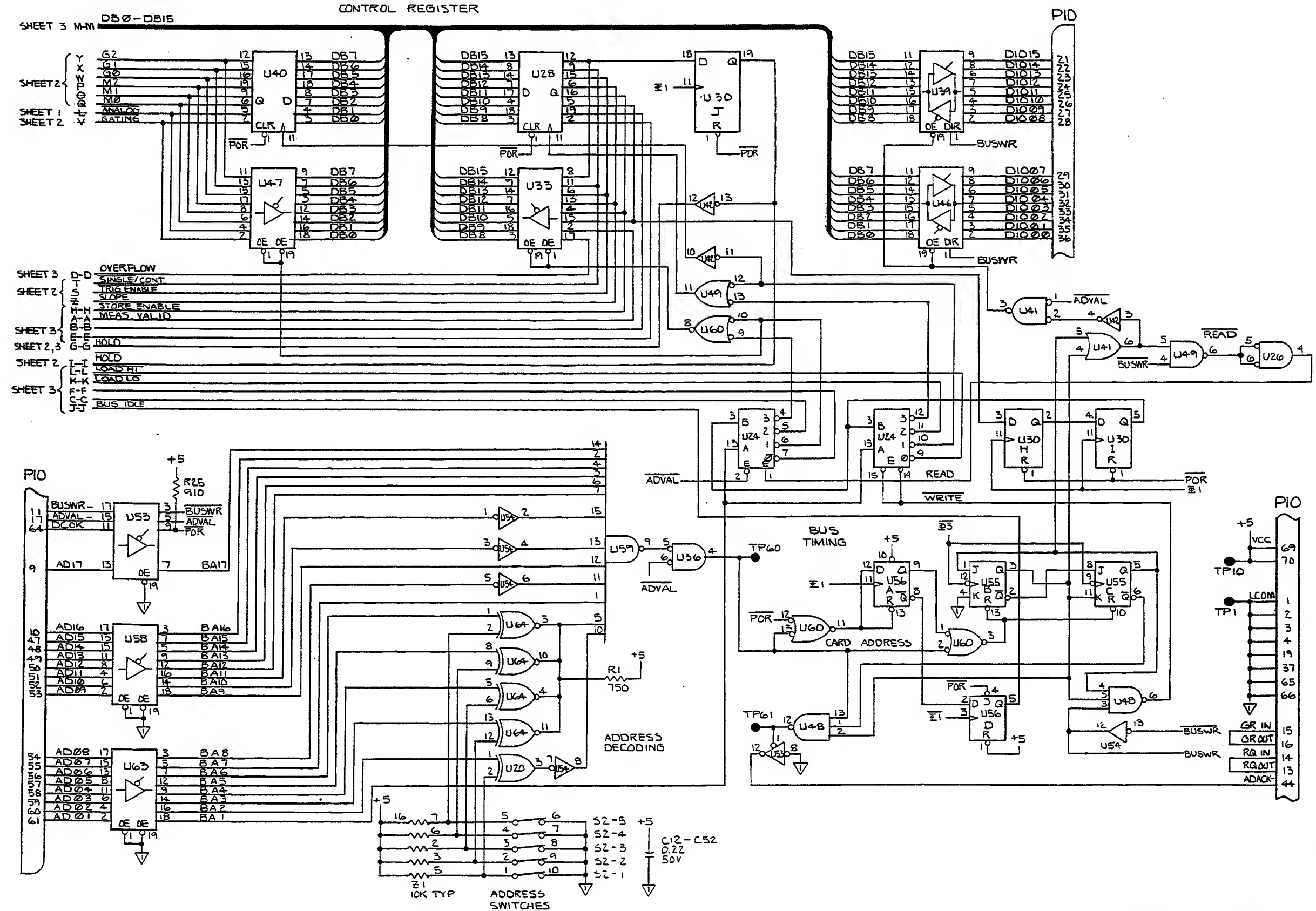
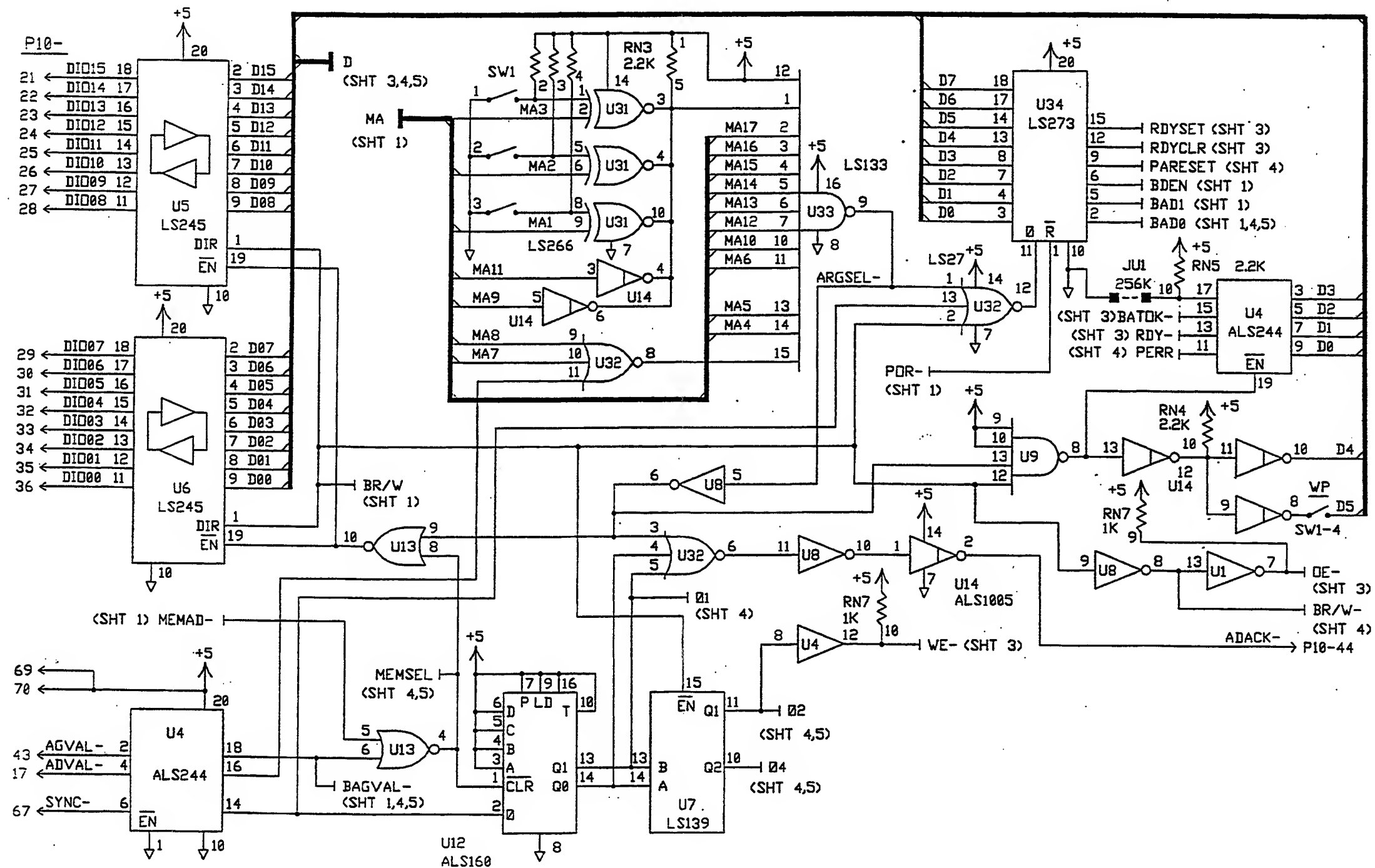


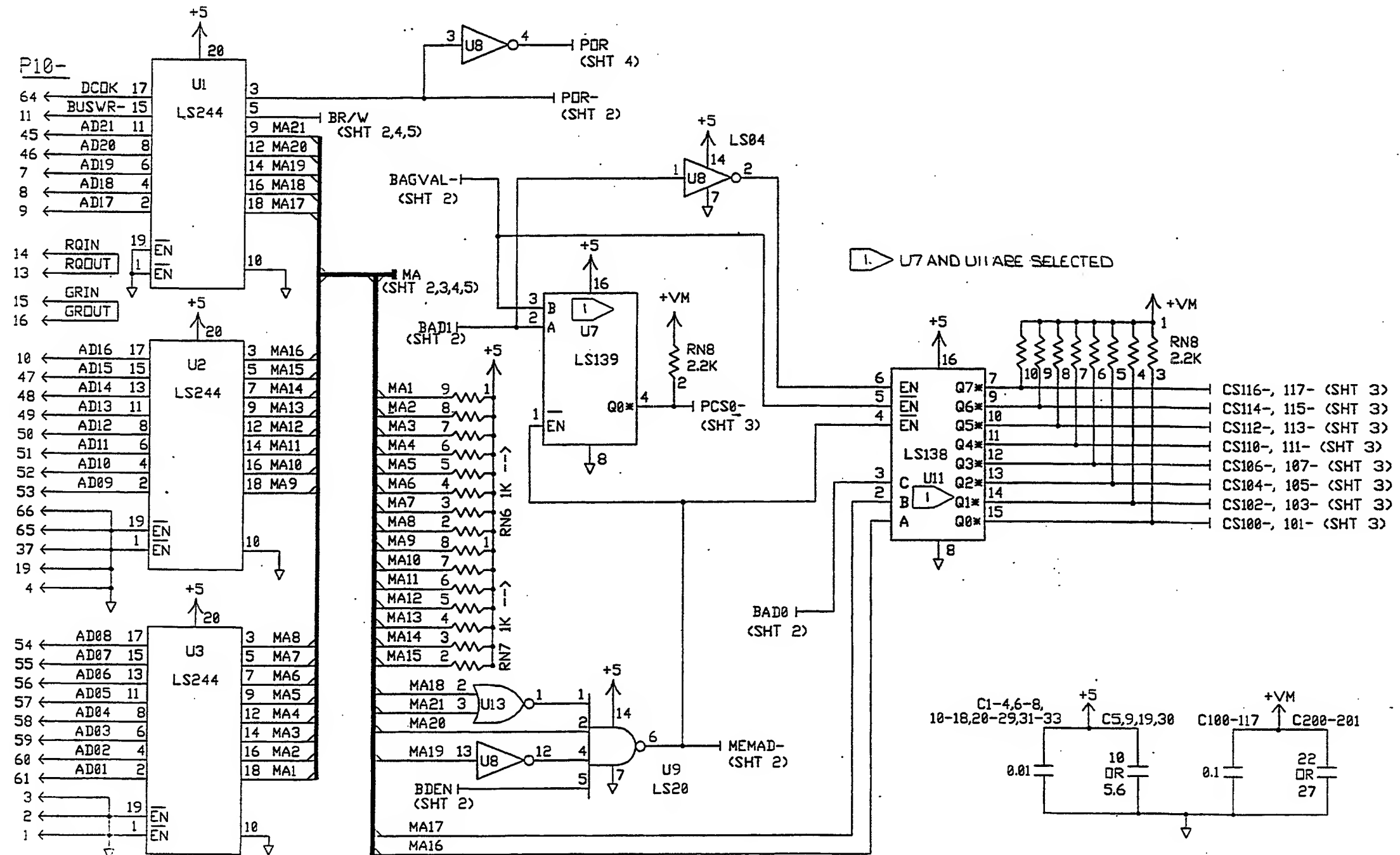
Figure 5-13. 012 Counter/Totalizer Module (cont)

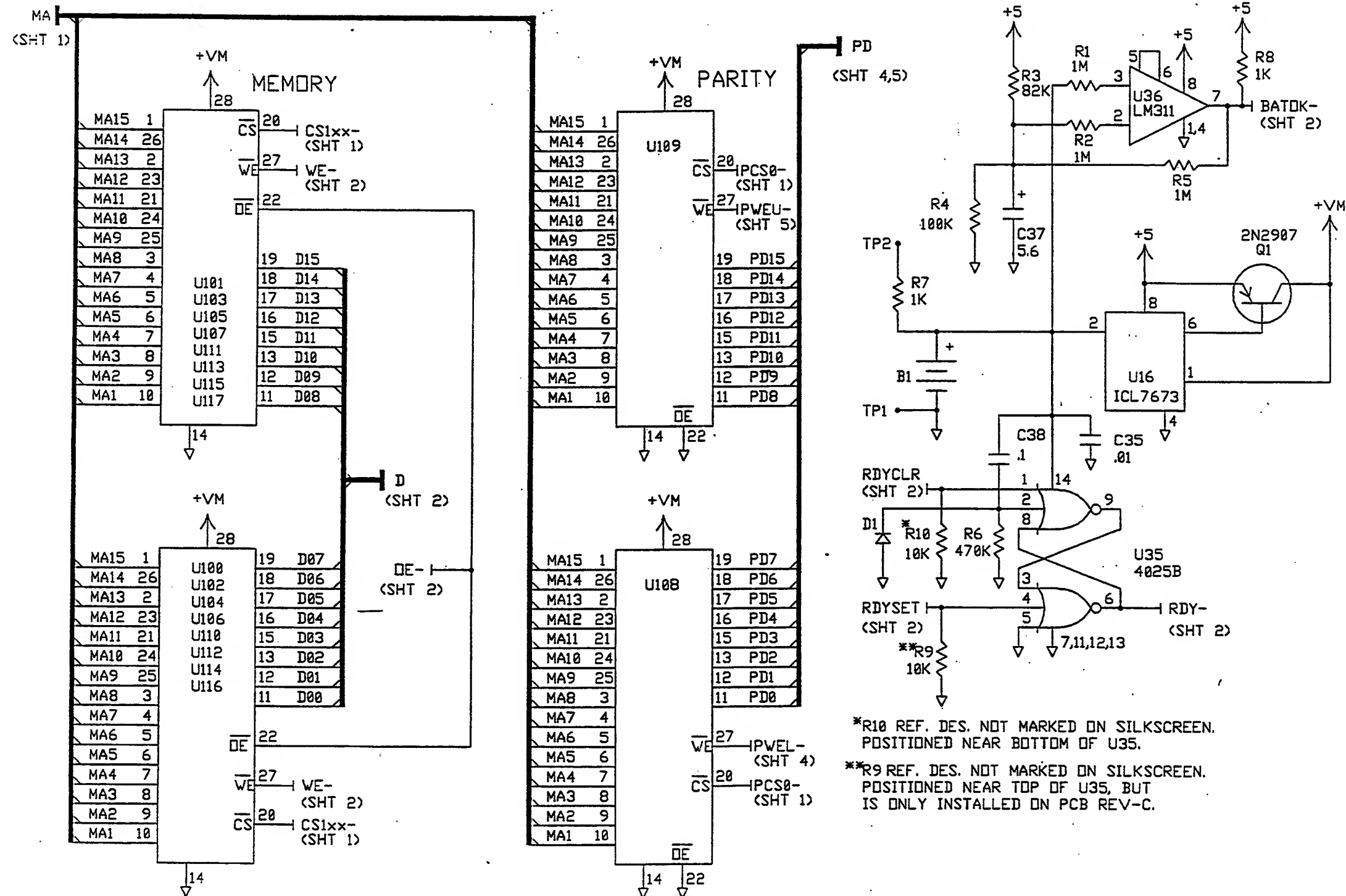
Schematic Diagrams

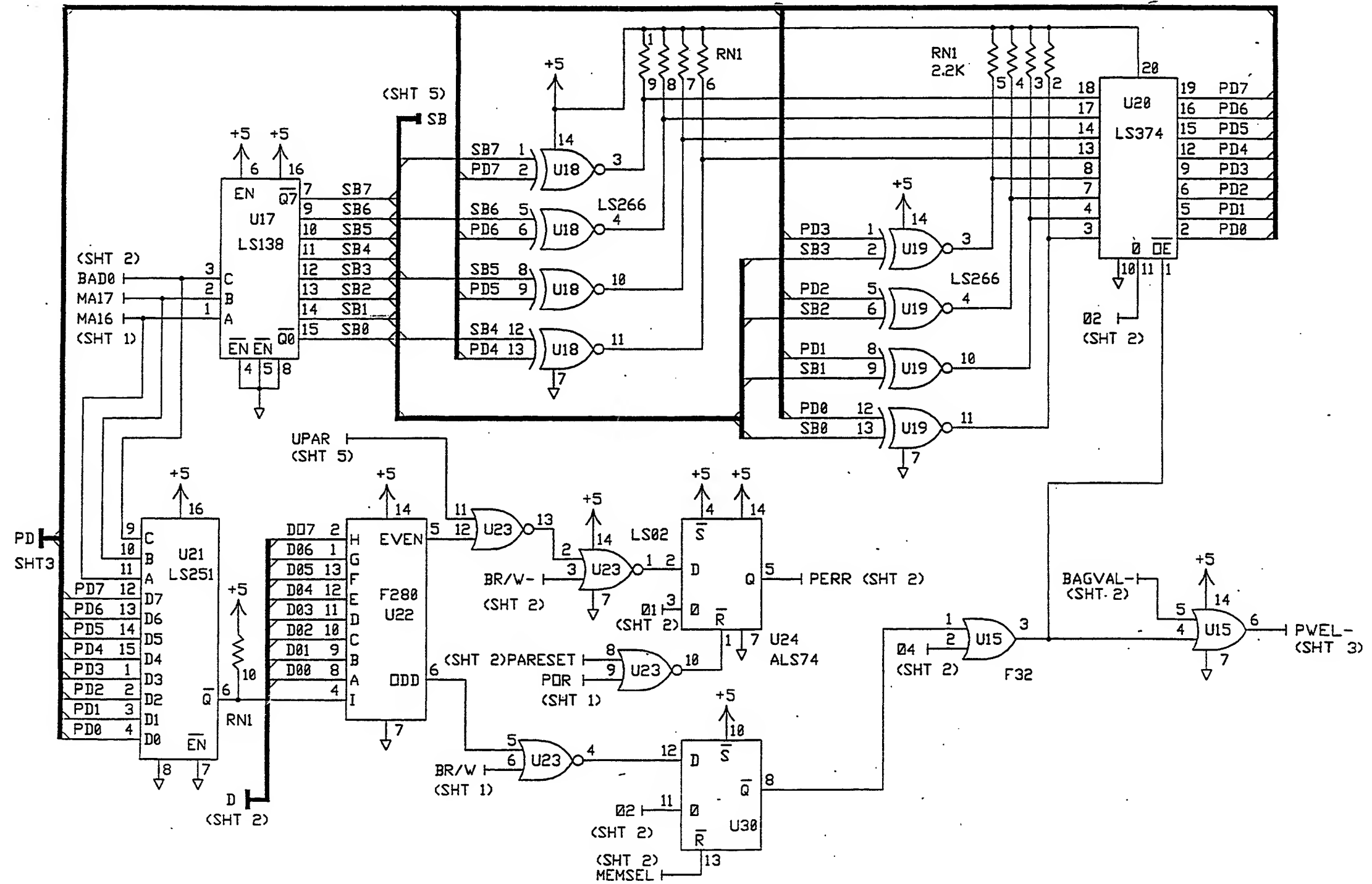


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(1 of 6)

Figure 5-14. 018, 019, 020 NVRAM Modules (Rev. 0)

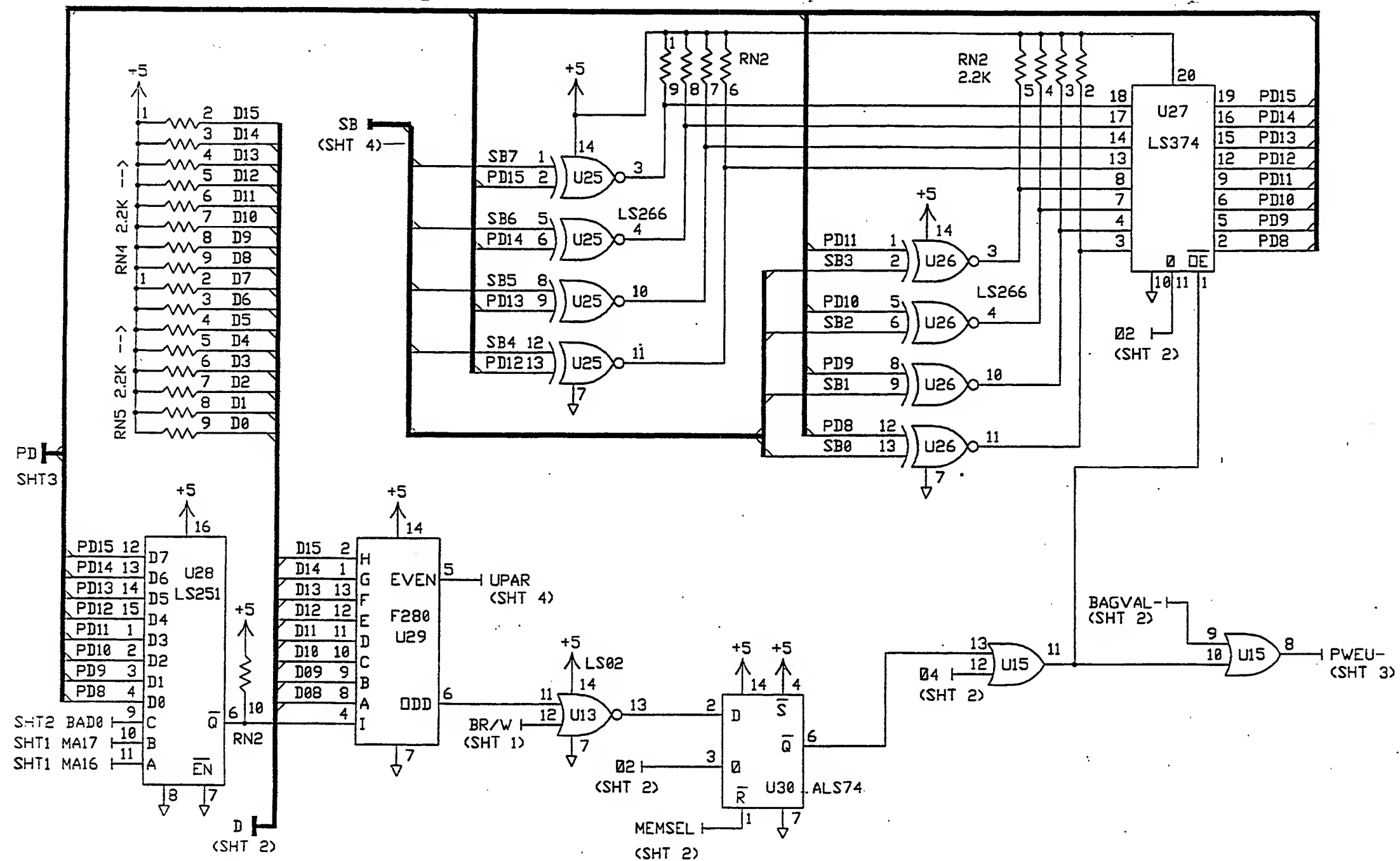


17XXA-1018
(3 of 6)Figure 5-14. 018, 019, 020 NVRAM
Modules (Rev. 0) (cont)



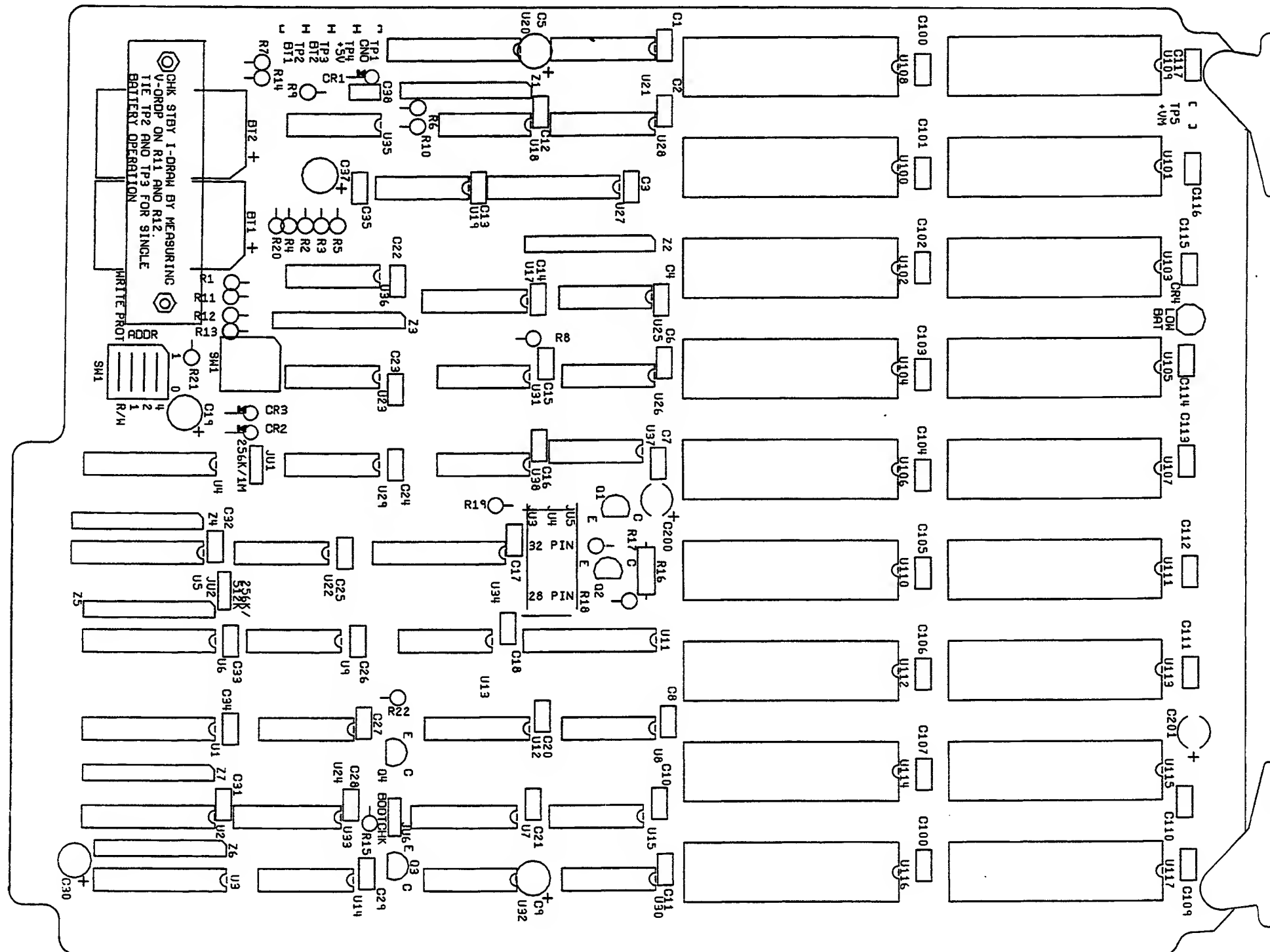
17XXA-1018
(4 of 6)

Figure 5-14. 018, 019, 020 NVRAM
Modules (Rev. 0) (cont)



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(5 of 6)

Figure 5-14. 018, 019, 020 NVRAM
Modules (Rev. 0) (cont)



17XXA-1618-PH2

Figure 5-15. 018, 019, 020 PH2 NVRAM Modules (Rev. A)

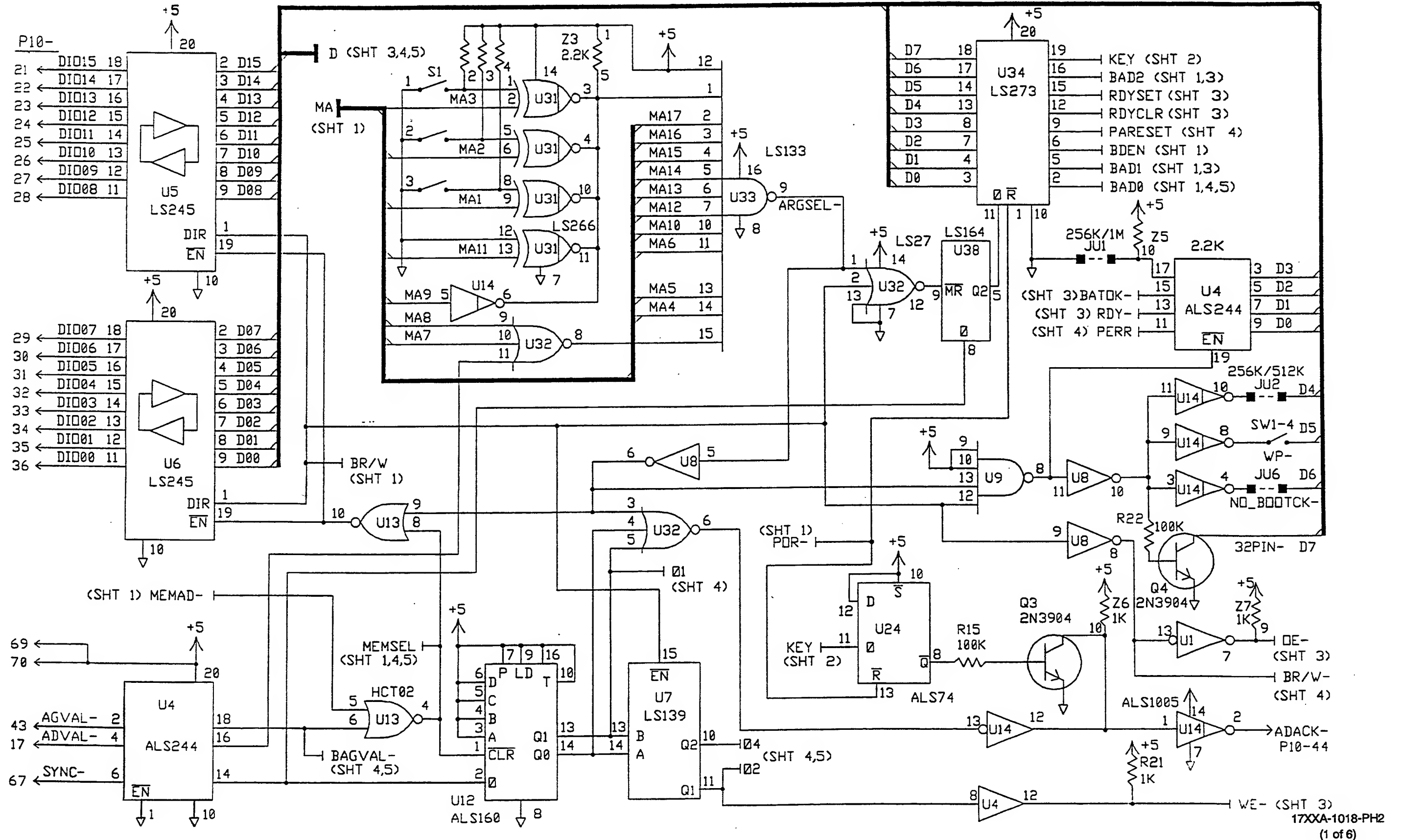


Figure 5-15. 018, 019, 020 PH2 NVRAM Modules (Rev. A) (cont)

Schematic Diagrams

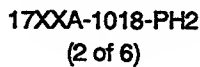


Figure 5-15. 018, 019, 020 PH2 NVRAM Modules (Rev. A) (cont)

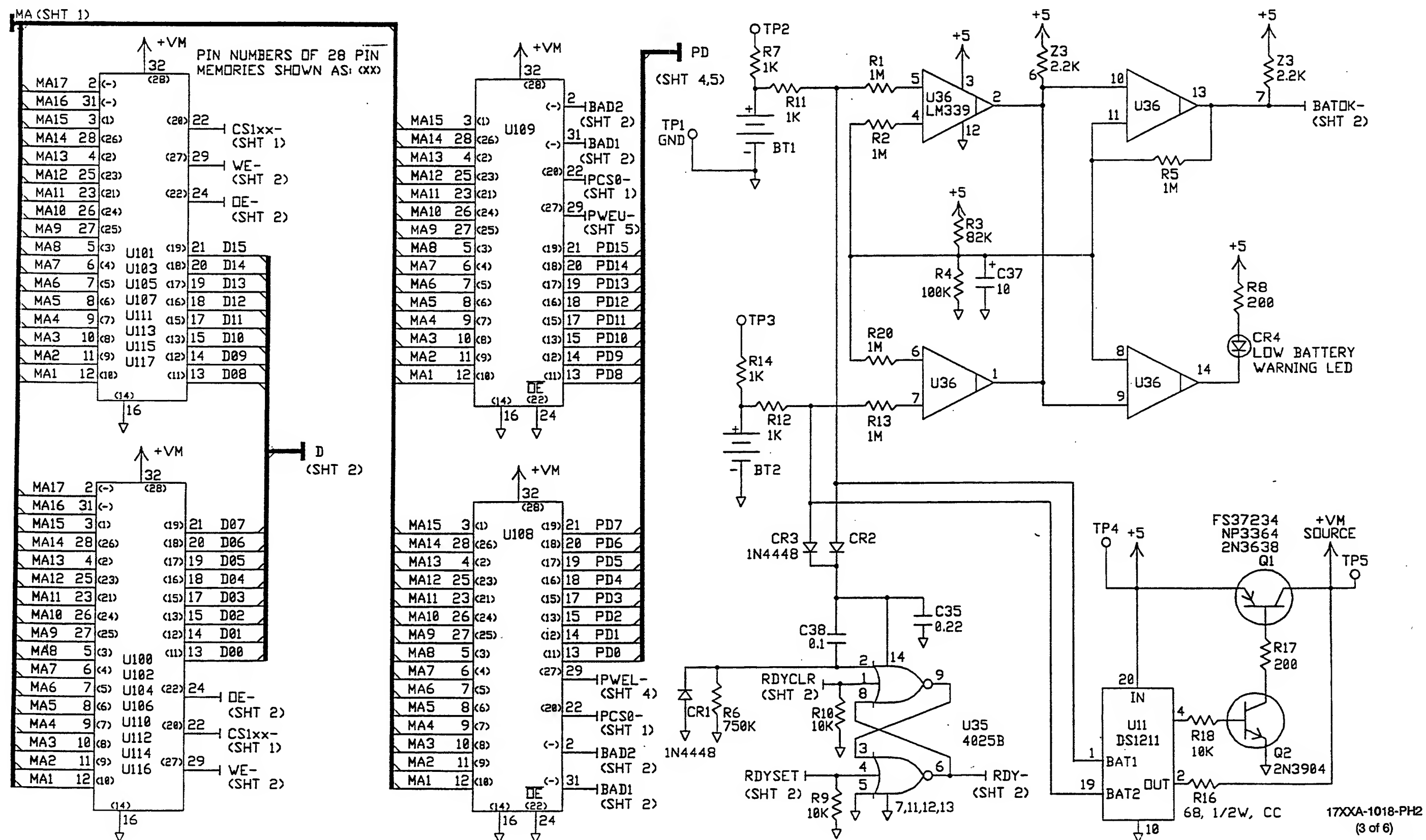
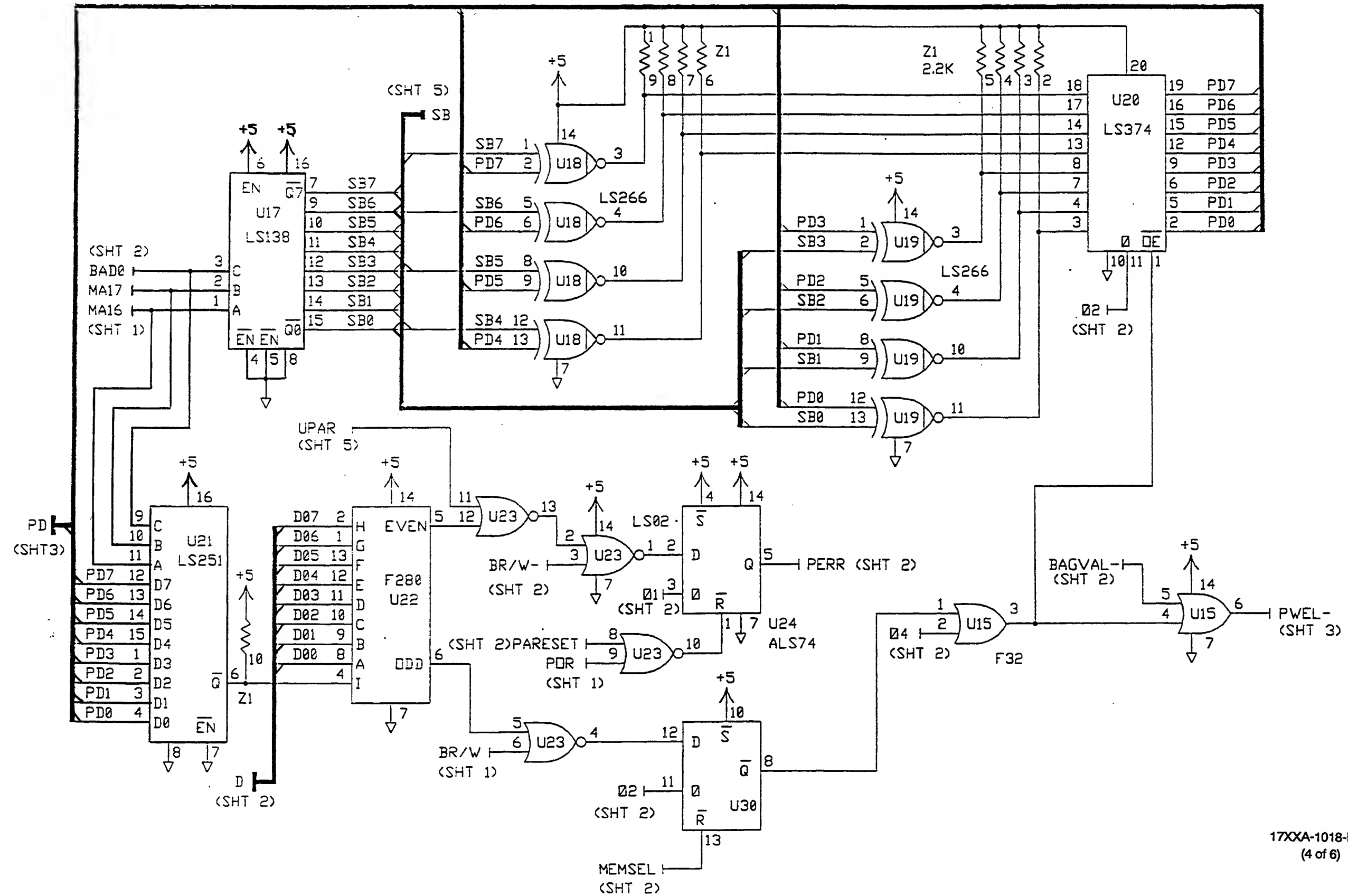


Figure 5-15. 018, 019, 020 PH2 NVRAM Modules (cont) (Rev. A)

Schematic Diagrams



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(4 of 6)

Figure 5-15. 018, 019, 020 PH2 NVRAM
Modules (Rev. A) (cont)

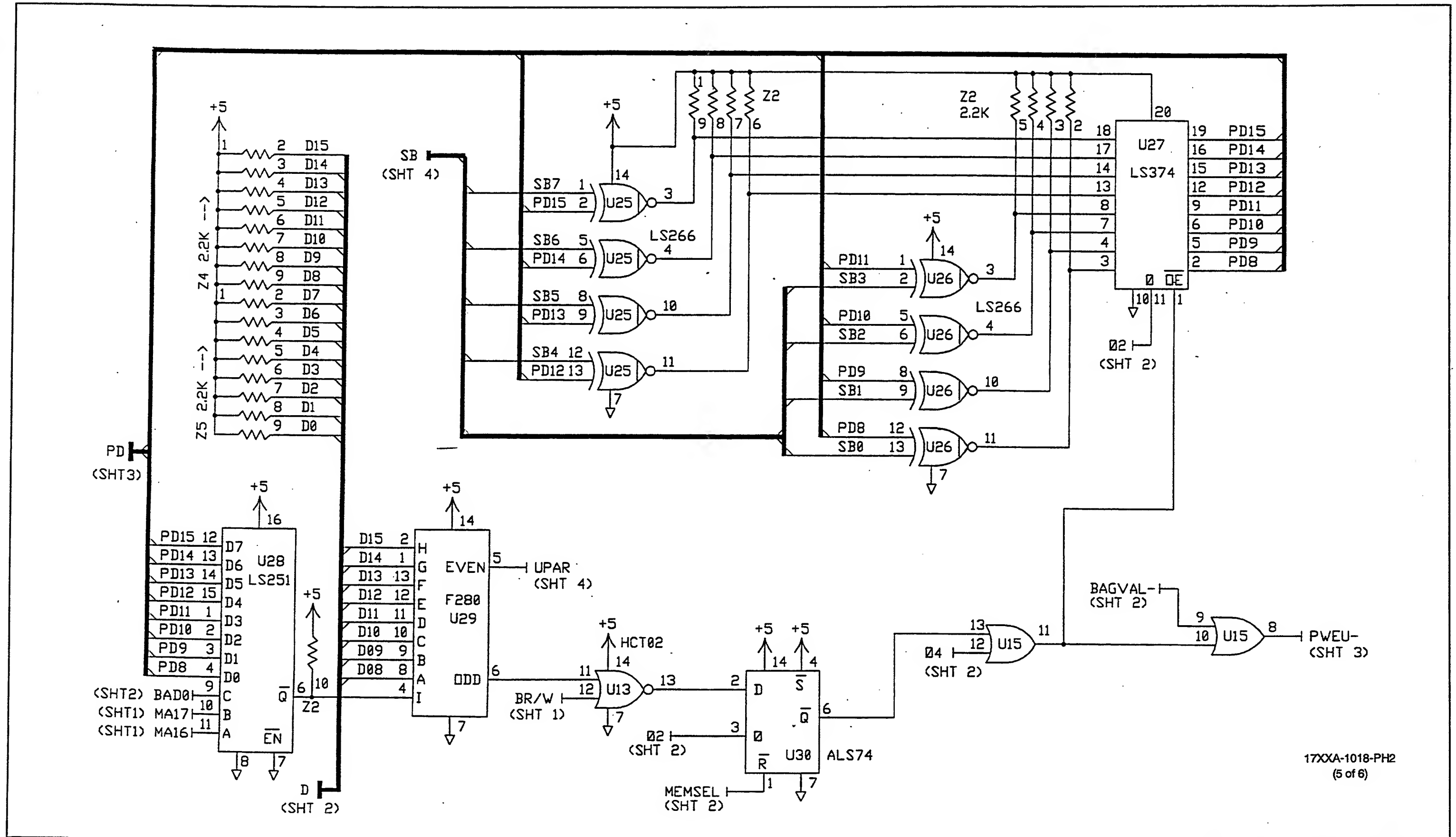
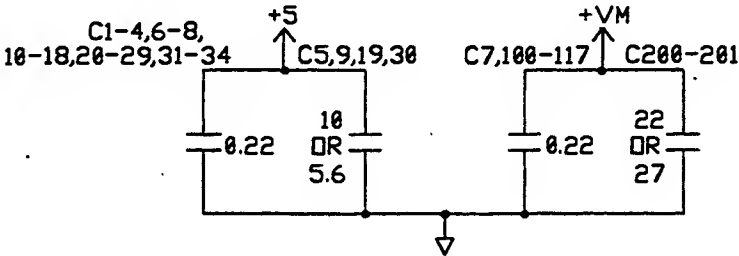


Figure 5-15. 018, 019, 020 PH2 NVRAM Modules (Rev. A) (cont)

Schematic Diagrams

NOTES: UNLESS OTHERWISE SPECIFIED:

- 1. ALL RESISTANCES ARE IN OHMS AND CAPACITANCES ARE IN MICROFARADS.
- 2. ALL RESISTORS ARE 1/4W, CF.
- 3. FOR ASSY DRAWING SEE: 17XXA-4018-PH2-1, -2, -3, OR -4
- 4. FOR REFERENCE DESIGNATION DRAWING SEE: 17XXA-1618-PH2
- 5. THIS SCHEMATIC, 17XXA-1018-PH2, IS FOR ASSY 17XXA-4018-PH2-1, -2, -3, OR -4 REV A OR GREATER WHICH CORRESPONDS TO PCB 17XXA-3018-PH2 REV D AND ABOVE. USE SCHEMATIC 17XXA-1018 FOR PCB REV C AND BELOW WHICH CORRESPONDS TO ASSEMBLY 17XXA-4018-1 AND -2 REV 0 (OR BLANK).



REF	DES	DEVICE	+5	+VM	GND	N.C.
U1-3		74LS244	20		1,10,19	
U4		74ALS244	20		1,10	
U5-6		74LS245	20		10	
U7		74LS139	1-3,16		8	4-7,9,12
U8		74F04	14		7	
U9		74LS20	9,10,14		7	3,11
U11		DS1211	20	2 [R16]	3,10	13
U12		74ALS160	3-7,9,10,16		8	11,12,15
U13		74HCT02	14		7	
U14		74ALS1005	14		7	
U15		74F32	14		7	
U17		74LS138	6,16		4,5,8	
U18-19		74LS266	14		7	
U20		74LS374	20		10	
U21		74LS251	16		7,8	5
U22		74F280	14		7	3
U23		74LS02	14		7	
U24		74ALS74	4,10,12,14		7	6,9
U25-26		74LS266	14		7	
U27		74LS374	20		10	
U28		74LS251	16		7,8	5
U29		74F280	14		7	3
U30		74ALS74	4,10,14		7	5,9
U31		74LS266	14		7,12	
U32		74LS27	14		7,13	
U33		74LS133	12,16		8	
U34		74LS273	20		10	
U35		4025			5,7,11-13	10
U36		LM339	3		12	
U37		74HCT04		14	3,5,7,9,11,13	4,6,8,10,12
U38		74LS164	1,2,14		7	3,4,6,10-13
U100-107		62256LP-12		30 (28)	16 (14)	
		628128LP-12		32	16	1
U108-109		62256LP-12		30 (28)	16,24(14,22)	
		628128LP-12		32	16,24	1
U110-117		62256LP-12		30 (28)	16 (14)	
		628128LP-12		32	16	1
				28 PIN DEVICE (PIN #)		

OPTION JUMPER CONFIGURATION AND POPULATION DIFFERENCES						
X = INTACT or INSTALLED - = CUT or NOT INSTALLED						
OPTION	JU1	JU2	JU3-5	Q3 R15	Q4 R22	PARITY PLUS MEMORY BYPASS
-018 (256K)	X	X				U108-109 (62256LP) PLUS U100-101 (628128LP) OR U100-107 (62256LP) C100-101,116,117 C100-104,113-117
-019 (512K)	-	X				U108-109 (62256LP) PLUS U100-103 (628128LP) OR U100-117 (62256LP) C100-102,115-117 C100-117
-020 (1MEG)	X	-	32	-	-	U100-109 (628128LP) C100-104,113-117
-021 (2MEG)	-	-	32	X	-	U100-117 (628128LP) C100-117

LAST USED	NOT USED	SPARES
BT2 CR4 C201 JU6 Q4 R22 S1 TP5 U117 Z8	C36 C39-99 C118-199 U10,16 U39-99	<p>The diagram shows three spare components: U7 (LS139) connected to +5V, U35 (4025) connected to +5V and ground, and U37 (HCT04) connected to +5V and ground. Pin numbers are indicated for each component.</p>

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(6 of 6)

Figure 5-15. 018, 019, 020 PH2 NVRAM
Modules (Rev. A) (cont)

Section 6 Options

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6-8.	PERIPHERALS	6-4
6-9.	SERVICE INFORMATION	6-4
6-10.	1722A/1752A CONFIGURATION INFORMATION.....	6-4
	17XXA-006/7/16/17 RAM EXPANSION MODULE	006-1
	17XXA-008 IEEE-488/RS-232-C INTERFACE	008-1
	17XXA-009 DUAL SERIAL INTERFACE	009-1
	1752A-010 ANALOG MEASUREMENT PROCESSOR	010-1
	1752A-011 ANALOG OUTPUT MODULE	011-1
	1752A-012 COUNTER/TOTALIZER	012-1
	1752A-013 MAINFRAME INTERFACE ASSEMBLY	013-1
	17XXA-018/019/020 Nonvolatile Memory	018-1
	17XXA-440 40M-Byte Hard Disk	440-1

6-1. INTRODUCTION

A number of options, accessories, and peripherals are available for the 17XXA series instruments (1722A and 1752A). The accessories are listed in Table 6-1, and the options and peripherals are listed in the following paragraphs. Option configuration information is presented in Figure 6-1. At the end of Section 6 each option is documented in its own subsection.

The list of options, accessories and peripherals is complete at this printing; however, because of Fluke's ongoing program of hardware and software development, other options or accessories may become available between reprintings of the manual. Contact your local Fluke representative for the latest information about available options.

6-2. OPTIONS

Options are identified by the unique three-digit identifier appended to a model number. For example, to order the -004 256K Byte Bubble Memory Expansion Module option, you would use number 17XXA-004.

6-3. Memory Options

Memory options greatly increase the available on-line storage capabilities of the Controller. The maximum RAM expansion configuration increases the total on-line system memory in file storage to about 3M bytes; Bubble Memory can provide up to approximately 1.5M bytes of file storage; NVRAM can provide up to approximately 5M bytes of file storage. Combinations are possible; consult the Figure 6-1 for further details. The following memory options are available:

17XXA-004	256K Byte Bubble Memory
17XXA-005	512K Byte Bubble Memory
1722A-006	256K Byte RAM Expansion
1722A-007	512K Byte RAM Expansion
1722A-016	1M Byte RAM Expansion
1722A-017	2M Byte RAM Expansion
17XXA-018	256K Byte NVRAM Memory
17XXA-019	512K Byte NVRAM Memory
17XXA-020	1M Byte NVRAM Memory
1722A-440	40M Byte Hard Drive
1711A/AA-440	40M Byte Hard Drive

6-4. Interface Options

The following Interface options expand the Input/Output possibilities of the Controller:

17XXA-002	Parallel Interface
17XXA-008	IEEE-488/RS-232-C Interface (slot 5 only)

17XXA-009 Dual Serial Interface

NOTE

When it is shipped from the factory, the 1722A Instrument Controller meets or exceeds the Class B requirements of FCC part 15-J and VDE 0871. To ensure continued compliance with these standards, any cables connected must be shielded and incorporate 360-degree metal connector bodies. These cables are available from John Fluke Mfg Co., Inc. using the following part numbers:

IEEE-488 Cables

- 1 meter: 658526
- 2 meter: 682401
- 4 meter: 682419

RS-232-C Cables (see Figure 6-2)

- 2 meter: 518712
- 10 meter: 518720

6-5. 1752A Measurement and Control Options

The 1752A comes equipped with one Analog Measurement Processor option. This option converts voltage or current into digital readings through individually addressable input channels.

Additional options for the 1752A include the Analog Output Module, which provides voltage or current outputs to external control points, and the Counter/Totalizer Module, which performs frequency, time and totalizing measurements. The Mainframe Interface Option connects the 1702A Extender Chassis to the 1752A.

1752A-010	Analog Measurement Processor
1752A-011	Analog Output
1752A-012	Counter Totalizer
1752A-013	Mainframe Interface

6-6. LANGUAGE SYSTEMS

For increased flexibility, the following software options are available to allow programming the Controller in languages other than Interpreted BASIC, which is supplied as the standard programming language. Each language option is supplied as a floppy disk with an accompanying Programming manual.

17XXA-201	Assembly Language Software Development System
17XXA-202	FORTTRAN Software Development System
17XXA-203	Compiled BASIC Software Development System
17XXA-205	Extended BASIC Software Development System

17XXA-912 Non-ANSI C Development System

17XXA-913 Non-ANSI C Compiler

6-7. APPLICATION SOFTWARE OPTIONS

The following application software options are available:

17XXA-900 Binder, to hold manuals for following:

17XXA-901 Gabby

17XXA-902 Touchscreen Toolbox

17XXA-903 Compiled MenuBASIC

17XXA-905 Extended MenuBASIC

17XXA-907 Transport->PC

S1703 Compiled MenuBASIC Development Package

S1705 Extended MenuBASIC Development Package

6-8. PERIPHERALS

The following peripherals are separate products, and can be ordered by the model numbers shown:

10XX Touch Control Screens

1702A Extender Chassis

1780A InfoTouch Display

6-9. SERVICE INFORMATION

Parts lists and schematics for the options are provided in Sections 4 and 5, respectively. Switch settings and service information follow in the option subsections. For more

information on system diagnostics, see Section 3 of this manual.

For complete service information on the -002, -004/5 and -013 options, consult the manual shipped with those options. There is no service information available for Option V7800; this option must be returned to a John Fluke Mfg. Co., Inc authorized Service Center or the Module Exchange Program for repair or exchange.

6-10. 1722A/1752A CONFIGURATION INFORMATION

Figure 6-1 lists the slots available for the 1722A and 1752A plug-in modules. A dot in a column indicates the slots that the option can be placed in. For example, if all available slots are used for 512K-byte RAM expansion memory modules, the system has the maximum memory configuration for this type of memory: 2.6M bytes, but no slots are available for other modules. Take particular notice of the additional constraints on module insertion (defined at the bottom of Figure 6-1.)

Options 1752A-010, -011, -012, -013, and V7800 are available for the 1752A only. The standard 1752A includes one Analog Measurement Processor. The 1752A is also available without the Analog Measurement Processor, as Model 1752A-1. Model 1752A-1 is appropriate for users who either do not intend to make voltage or current measurements, or will be making such measurements only with the V7800 option.

NOTE

The Analog Measurement Processor is shipped in slot 5. Normally it may be used in any of the Input/Output Options slots. Slot 6 has no Input/Output access.

Table 6-1. Accessories

MODEL	DESCRIPTION
	MISCELLANEOUS
Y1700	Keyboard
Y1706	Ten-pack of Blank Unformatted Floppy Disks (Certified)
P/N 533547	Pad of 50 Programmers Worksheets
Y1711	Reinforced Shipping Case
Y1704	Circuit Board Extender for the 1722A/1752A
Y1752	Line Frequency Sync Transformer
	IEEE-488 CABLES
Y8021	IEEE-488 Cable, Shielded, 1 meter
Y8022	IEEE-488 Cable, Shielded, 2 meter
Y8023	IEEE-488 Cable, Shielded, 4 meter
	RS-232C INTERFACE CABLES, STANDARD (FOR DCE DEVICES)
Y1707	RS-232-C Interface Cable, Standard, 2 meter
Y1708	RS-232-C Interface Cable, Standard, 10 meter
	RS-232C INTERFACE CABLES, NULL MODE (FOR OTHER DTE DEVICES)
Y1702	RS-232-C Interface Cable, Null Modem, 2 meter
Y1703	RS-232-C Interface Cable, Null Modem, 4 meter
Y1705	RS-232-C Interface Cable, Null Modem, 0.3 meter
	OTHER CABLES
Y1717	Parallel Interface Cable
Y1709	Printer Cable, 2-meter
2402A-502	I/O Extender Cable, 9 meter flat cable for connecting the 1752A and 1702A.
	CONNECTORS
Y1750	Input Terminal Block w/Cable
2400A-110	Screw Terminal I/O Connector
2400A-111	Solder Pin I/O Connector
	MOUNTING HARDWARE
Y1790	Rack Mount Kit with 24-inch slides
Y1794	Rack Mount kit with 18-inch slides
M00-260-610	18" Rack Slides
M00-280-610	24" Rack Slides
Y1795	Side Carrying Handle

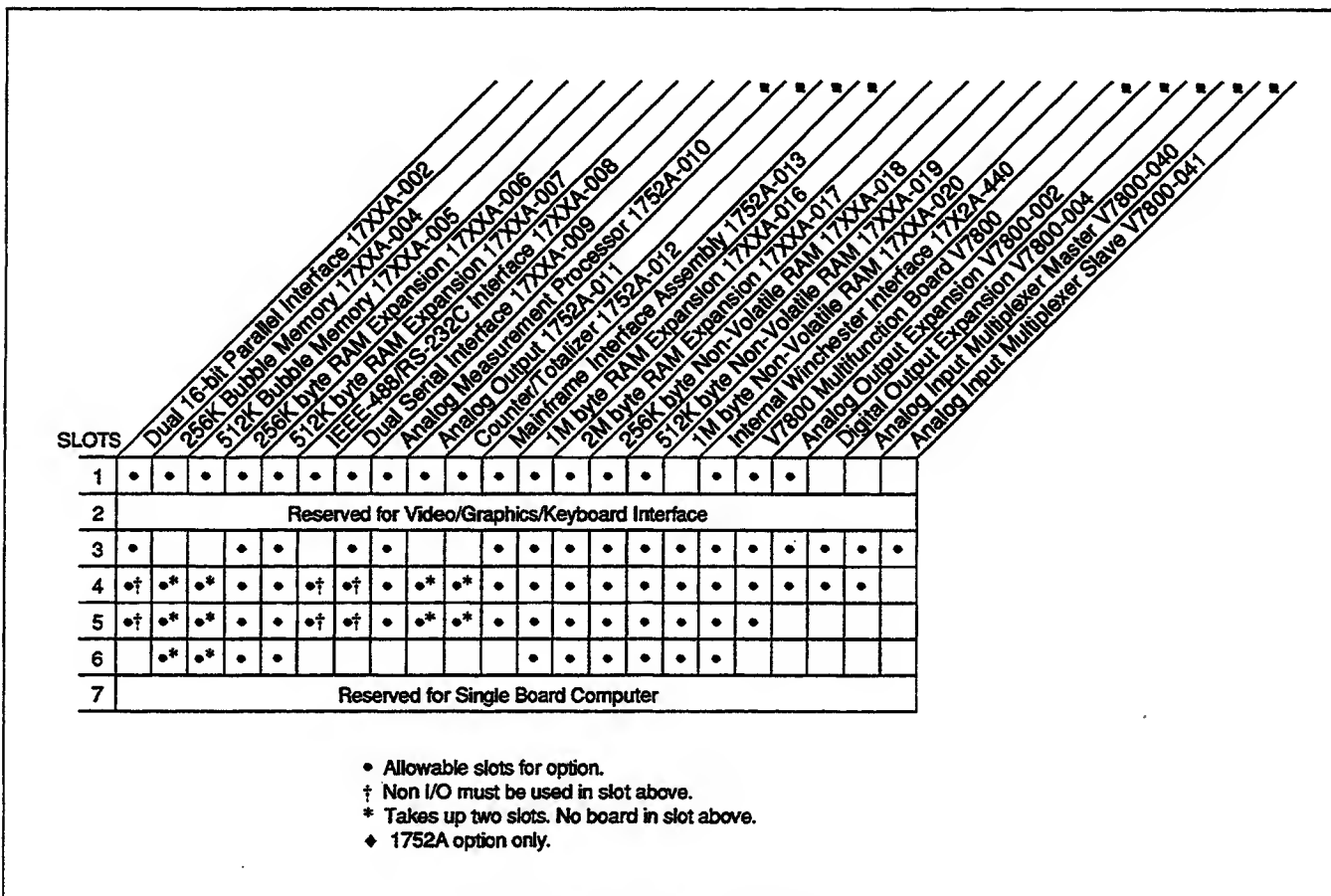
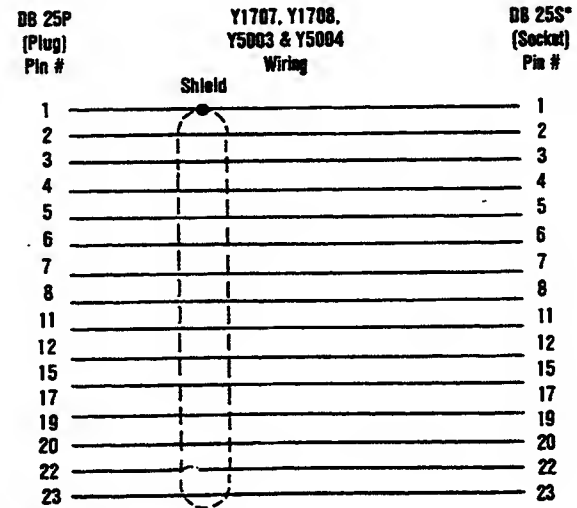
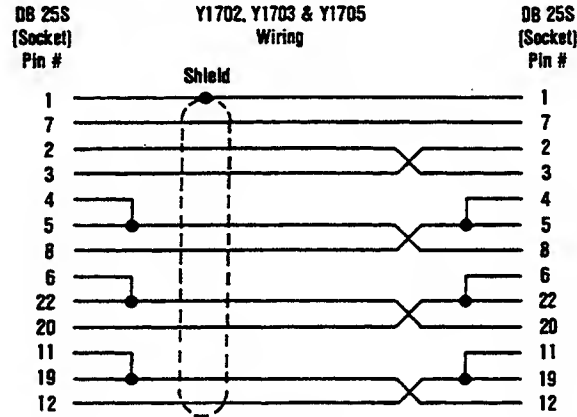


Figure 6-1. Option Configuration

RS-232 Cable Wiring



*DB 25P for Y5003 and Y5004

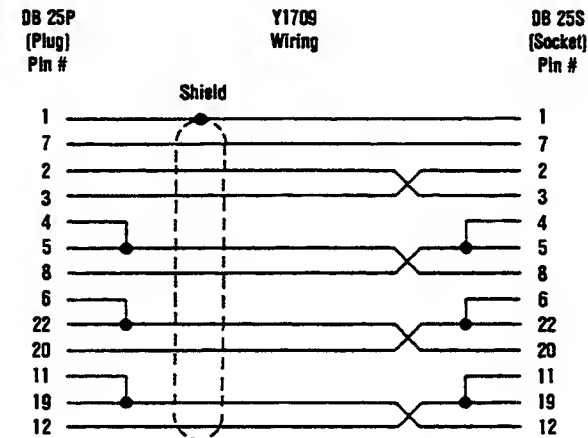


Figure 6-2. RS-232 Cable Wiring

Option 17XXA-002 Parallel Interface Board

002-1. INTRODUCTION

The 17XXA-002 Parallel Interface (PIB) adds two 16-bit parallel interfaces to the 1722A or 1752A. A maximum of three PIBs may be installed in one 17XXA system, for a total of six 16-bit ports. See Configuration Information for allowable configurations for the -002 option.

The PIB can adapt to some of the most unusual interface requirements of connected devices. Using software drivers supplied by Fluke, the PIB provides bidirectional transfer of bits (for monitoring and controlling status), 16-bit words (for communication with BCD instrumentation), or 512-word blocks (for maximum-speed data transfer of 80K words per second). Handshake or strobe protocols

may also be selected under the control of the user's program.

002-2. SWITCH SETTINGS

The operating configuration of the Parallel Interface is set up by the board address switch on the -002 module. Set the board address switch for ports PI0 and PI1, using the table below.

002-3. SERVICING THE 17XXA-002 OPTION

For 17XXA-002 service information, refer to the 17XXA-002 Parallel Interface Board manual, supplied with the option. For information on the System Diagnostic Tests, see Section 3 of this manual.

Table 002-1. Option 17XXA-002 Switch/Address Operating Configuration

BOARD	SW4	SW3	SW2	SW1	PORT PI0	ADDRESS PI1RANGE	ADDRESS
1	N	ON	ON	ON	0	1	F340-F346
2	O	ON	ON	OFF	2	3	F348-F34E
3	T	ON	OFF	ON	4	5	F350-F356
4		ON	OFF	OFF	6	7	F358-F35E
5	U	OFF	ON	ON	8	9	F360-F366
6	S	OFF	ON	OFF	10	11	F368-F36E
7	E	OFF	OFF	ON	12	13	F370-F376
8	D	OFF	OFF	OFF	14	15	F378-F37E

Option 17XXA-004/-005 Magnetic Bubble Memory

004/5.1 INTRODUCTION

The Option 17XXA-004/-005 Bubble Memory Modules provide additional memory for the 1722A or the 1752A. Like a floppy disk, the Bubble Memory is treated by FDOS as a file-structured device. Information is retained in the device when the power is turned off.

The 17XXA-004 Bubble Memory Module contains 256K bytes of memory; the 17XXA-005 module contains 512K bytes. The maximum amount that can be installed in a system is 1.5M bytes (any combination of three modules).

004/5-2. SWITCH SETTINGS

See Configuration Information for allowable configurations for the -004/-005 options.

Each Bubble Memory must be associated with a unique address. The board address switch (SW1) determines device names for this address. Settings are identical for Option -004 (256K byte) and Option -005 (512K byte).

004/5-3. SERVICING THE 17XXA-004/-005 OPTION

For 17XXA-004/-005 service information, refer to the 17XXA-004/-005 Magnetic Bubble Memory manual, supplied with the option. For information on the System Diagnostic Tests, see Section 3 of this manual.

Table 004/5-1. Option 17XXA-004/-005
Switch/Device Name Operating Configuration

DEVICE NAME	ADDRESS CODE	SWITCH POSITIONS			
		1	2	3	4
MB0:	111X	on	on	on	X
MB1:	110X	on	on	off	X
MB2:	101X	on	off	on	X
MB3:	100X	on	off	off	X

NOTES:

1. "1" = on, "0" = off, "X" = don't care.
2. Four device names are available. However, only three are used at a time because only three modules can be installed at one time.

Options 17XXA-006, -007, -016, -017

Memory Expansion Modules

006-1. INTRODUCTION

The memory expansion modules (17XXA-006, -007, -016, and -017) provide additional memory for the 1722A/1752A. This added memory can be configured as electronic disk (E-Disk). The operating system treats memory configured as E-Disk as an electronic version of a floppy disk, storing and retrieving files in a formatted fashion. Any area of the memory expansion module not configured as E-Disk is handled by the operating system as standard RAM.

Memory expansion module capacity is as follows:

- 17XXA-006 256K bytes
- 17XXA-007 512K bytes
- 17XXA-016 1M bytes
- 17XXA-017 2M bytes

A maximum of five modules (not exceeding 3M-bytes of expansion memory) may be installed in the 1722A. A maximum of four modules (not exceeding 3M-bytes) can be installed in the 1752A.

The 17XXA-018/-019/-020 NVRAM options and the Virtech V7800 Multifunction Board use a small section of expansion memory address space for their operation. If any of these options is installed in either a 1722A or a 1752A, the maximum allowable expansion memory that can be installed is reduced to 2.75M bytes.

All four dynamic RAM modules (-006, -007, -016, and -017) are based on the same printed circuit assembly; each assembly is individually configured through a jumper arrangement. Electrically, the RAM modules reside on the 17XXA's system bus (the AGGIE bus and the ARGUS bus.) These two busses share the same address lines. To indicate that a memory or I/O cycle is taking place on the ARGUS bus, the microprocessor sends out the Address Valid signal (ADVAL-). To address devices on the AGGIE bus, the microprocessor sends out the AGGIE Bus Address Valid signal (AGVAL-) along with the address.

Memory on options -006, -007, -016, and -017 is located on the AGGIE bus and can be addressed when AGVAL- is active. The Error Status Register is located on the ARGUS bus.

006-2. THEORY OF OPERATION

006-3. Functional Description

For the following discussion, refer to the block diagram in Figure 006-1 and the schematic diagram in Section 5.

006-4. Memory Array

The memory array contains the memory chips that store data and parity information. On Option -006, the memory array consists of 36 64K RAMs forming 256K bytes (128K words) of memory. On the Option -007, the memory array consists of 72 64K RAMs forming 512K bytes (256K words) of memory.

On Option -016, the memory array consists of 36 256K RAMs forming 1M bytes (512K words) of memory. On Option -017, the memory array consists of 72 256K RAMs forming 2M bytes (1M words) of memory. Bank2 and Bank3 (U37 through U72) are not used on Memory Expansion options -006 and -016.

See Figure 006-2 for a map of the memory array.

006-5. RAM CONTROL SIGNALS

The RAM address lines (RAD0 through RAD8) hold both the row and column addresses for the RAMs. The address lines are multiplexed between the row address and the column address of the internal bit-cell array. With options -006 and -007, the 9th bit of the array (RAD8) is held high and inactive. The row address is strobed in first by the Row-Address Strobe (RAS-) and is replaced by the Column Address Strobe (CAS-). The addresses are latched by the RAMs during the high to low transition of the strobe signals.

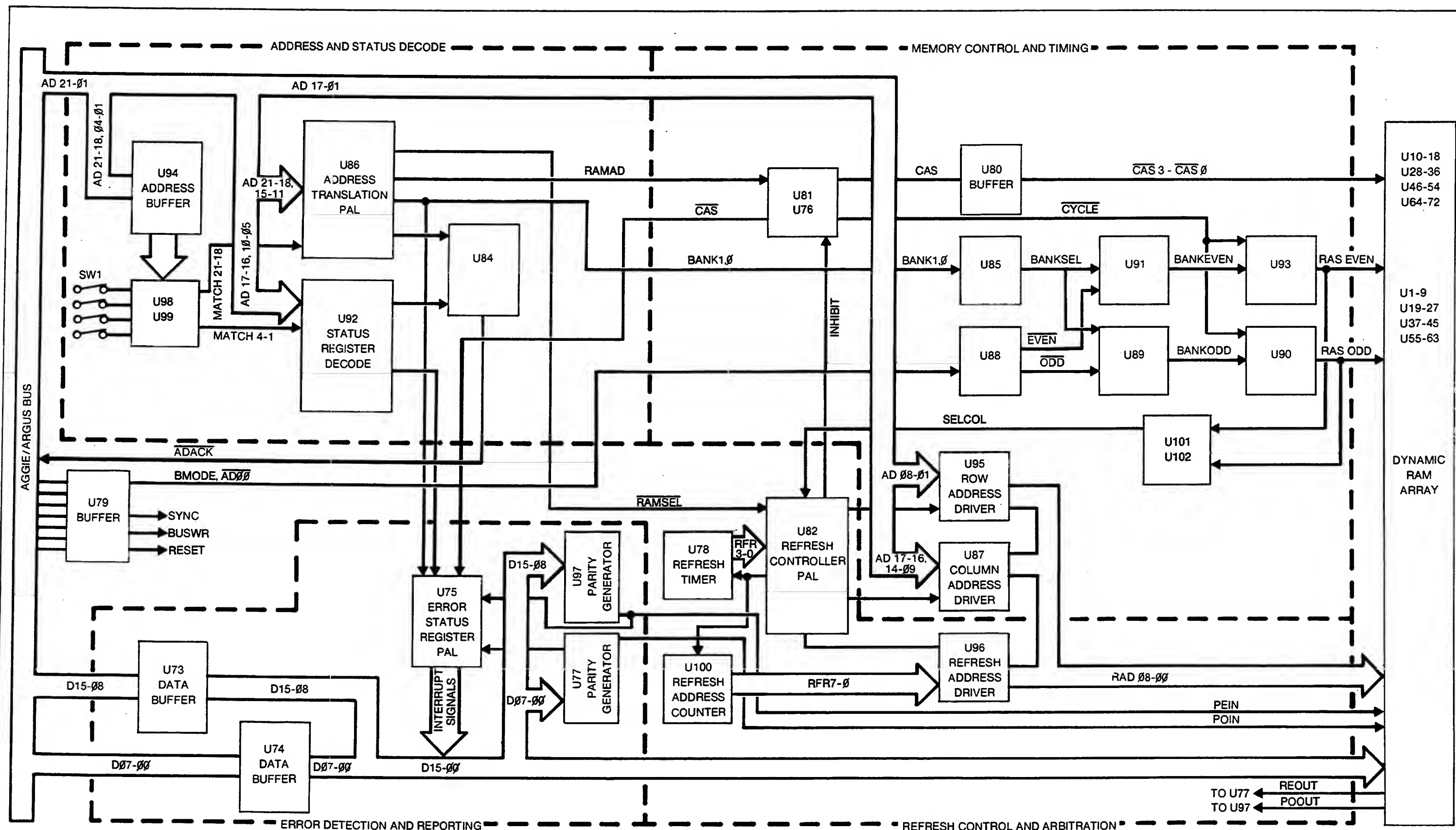


Figure 006-1. Memory Expansion Module
Block Diagram

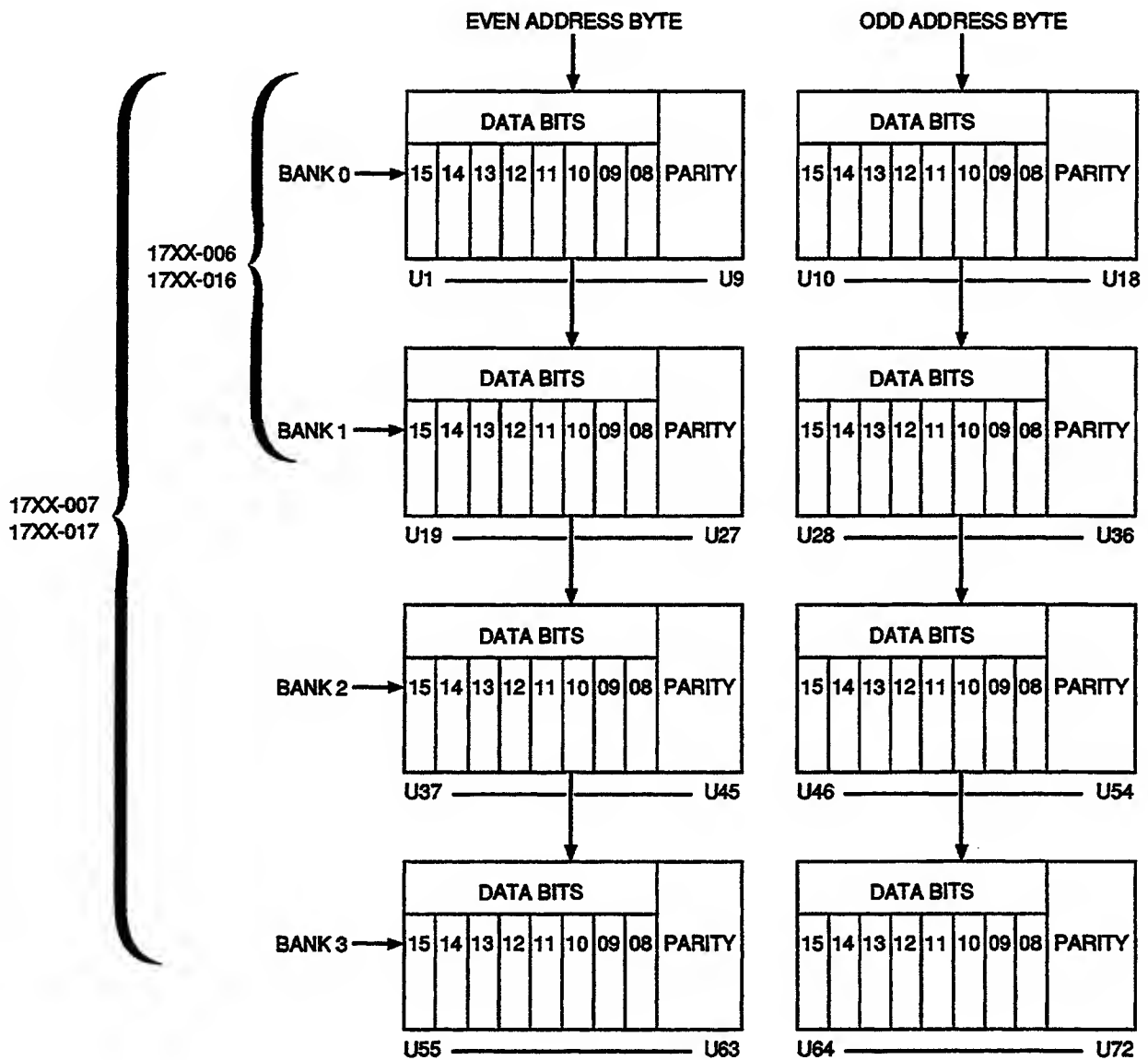


Figure 006-2. Memory Array Map

RAS- drives the RAM chips, signaling them to sample the address lines for a valid row address. The row address must be valid before RAS- goes low. Figure 006-3 shows Row Address Strobe signal timing.

CAS- signals the RAMs to sample the address lines for a valid column address. The column address must be valid before CAS- goes low. Figure 006-4 shows Column Address Strobe signal timing.

The WRITE- signal determines whether data will be read from or written to the RAMs. In the low state, and at the rising edge of CAS-, Data Output (DOUT) of the RAMs will contain valid data read from the RAMs. When WRITE- is in the high state, DOUT will be tri-stated and Data Input (DIN) will contain data to be stored into the RAMs. DOUT from the RAMs is active during read cycles, and tri-stated during write cycles. DIN to the RAMs is only valid during write cycles.

006-6. Address Decoding

The four highest address bits of the AGGIE bus (AD21 through AD18) are fed through a non-inverting buffer (U94) and are compared with the four board address switch bits (S4 through S1). The comparison is performed by quad exclusive OR gates (U98 and U99) which generate outputs MATCH21- through MATCH18-. MATCH21- through MATCH18- are active low as follows: MATCH21- when AD21 matches S4; MATCH20- when AD20 matches S3; MATCH19- when AD19 matches S2; MATCH18- when AD18 matches S1.

The Address Translation PAL (U86) examines the state of the MATCHnn- signals and the board configuration. If the memory on its board is being addressed, the RAM-Addressed signal (RAMAD-) is driven active low, passes through an inverter (U80) and triggers a memory cycle. RAMAD- is also gated with AGGIE Bus Address Valid (AGVAL) and the Inhibit for Refresh Cycle (INHIBIT-) signal to generate ADACK- active low, which signals that the board has recognized its address. If ADACK- does not go low, the device controlling the bus will insert wait-states in the bus cycle. If ADACK- remains inactive high, the controlling device will timeout and abort the bus cycle. If a bus timeout occurs, the 1722A/1752A will display the message: !Non-existent I/O device.

006-7. BOARD CONFIGURATION

Options -006 and -007 differ from one another in the number of banks of memory contained on the board and in the presence of the factory-set jumpers R1 and R2 that set the configuration of the board. R1 is not inserted for options -007 and -017, but must be present for options -006 and -016. R2 is not inserted on options -006 and -007 but is installed on the -016 and -017. The -007 and -017 pca's contain 72 RAMs each. The FULL signal is active (high). When R1 is inserted for options -006 and -016, the operating system (FDOS) will recognize and access the address space for the 36 RAMs on the board. The FULL signal will be inactive (low).

The Address Translation PAL (U86) uses the FULL and 64K signals to determine the size of the memory space on the AGGIE bus that the board must respond to. The Status

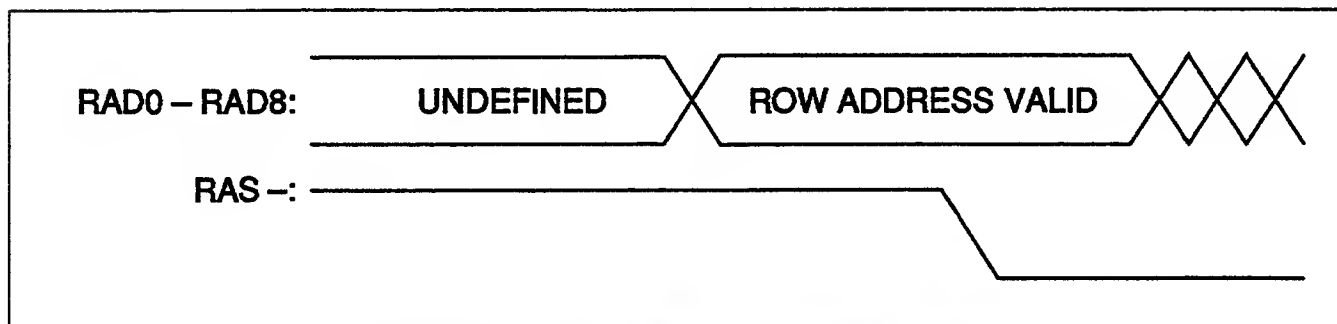


Figure 006-3. Row Address Strobe Signal Timing

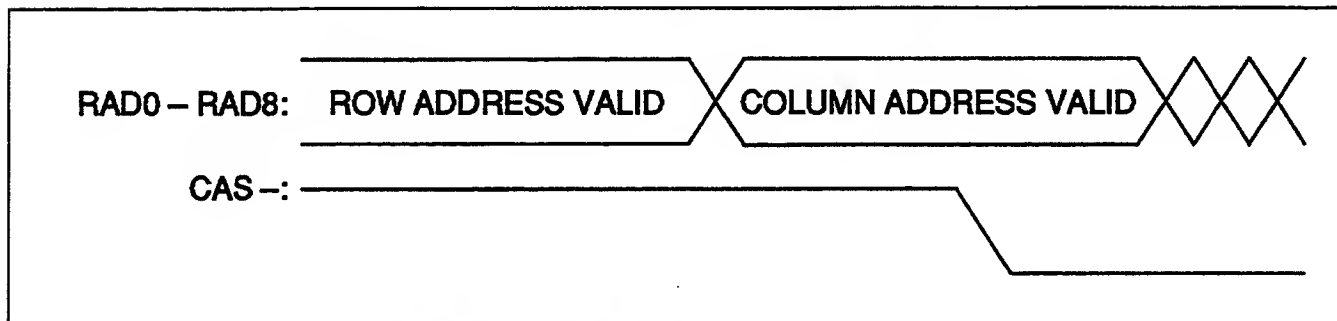


Figure 006-4. Column Address Strobe Signal Timing

Register Decode PAL (U92) uses these signals to determine the size of the memory space on the AGGIE bus covered by the board, and what addresses on the ARGUS bus the Error Status Register must respond to.

006-8. BOARD ADDRESS SELECTION

Refer to Table 006-1 when you are configuring the addresses of the installed expansion memory options. Use the following procedure to set these addresses:

1. Remove any memory options already installed in the controller.
2. Starting with the largest capacity memory expansion option to be installed, set the address switches to the configuration shown at the bottom of the appropriate column in Table 006-1. For example, if Option -016 is the largest installed memory expansion, set the switches to 11XX (OFF, OFF, X, X).
3. A large memory option may overlap the range of several smaller options. Therefore, set the address

switches of the next smaller option to a starting point beyond the address range of the larger option.

For example, for one -017 (2M), one -007 (512K), and one -006 (256K), set the switches to:

2M=1XXX 512K=011X 256K=0100

006-9. ERROR STATUS DECODING

When an error occurs within the memory, the memory board signals the device using the board. An interrupt occurs and the device polls the Error Status Register addresses on the ARGUS bus to locate the error.

Addresses on the ARGUS bus that do not reside on an installed memory board will generate a timeout error. Since each responding status register corresponds to a particular 1/4M byte of memory space on the AGGIE bus, this timeout error indicates a missing 1/4M byte section of memory on the AGGIE bus.

Table 006-1 shows the error status register address space,

Table 006-1. Bus Memory and Error Status Addresses

ADDRESS		OPTION SWITCH SETTINGS			
AGGIE BUS	ARGUS BUS STATUS	-006	-007	-016	-017
100000-13FFFE	3F5C8	0100	010X	01XX	na
140000-17FFFE	3F5CA	na			
180000-1BFFFE	3F5CC	0110	011X		
1C0000-1FFFFE	3F5CE	na			
200000-23FFFE	3F5D0	1000	100X	10XX	1XXX
240000-27FFFE	3F5D2	na			
280000-2BFFFE	3F5D4	1010	101X		
2C0000-2FFFFE	3F5D6	na			
300000-33FFFE	3F5D8	1100	110X	11XX	
340000-37FFFE	3F5DA	na			
380000-3BFFFE	3F5DC	1110	111X		
3C0000-3FFFFE	3F5DE	na			

NOTES

- a. 0 = ON (closed), 1 = OFF (open)
- b. Although the controller may operate properly with the addresses set out of order, setting them in the recommended order ensures that diagnostic software can correctly identify faulty components and prevents possible bus contention problems when mixing options.
- c. Any overlapping address range yields an immediate parity error, but will not damage the option. Reset the address switches to the correct positions and execute a cold boot of the 1722A/1752A.
- d. When testing memory options with the System Diagnostic Program, "Board 0" refers the memory option set to the highest physical address. For example: In a system containing a -016 (set to 11XX), and a -007, (set to 101X), Board 0 would be the -016 and Board 1 would be the -007.

Error status register decoding is performed as follows. The Address Translation PAL (U86) reads the five upper address bits on the ARGUS bus (AD15 through AD11) and drives STATUS- low whenever the bits contain the addresses of the upper part of the Error Status Register address space. The four lower active address bits from the ARGUS bus (AD04 through AD01) pass through the non-inverting buffer (U94) and are compared against the four bits, (S4 through S1). MATCH4- through MATCH1- are generated low as follows: MATCH4- when AD04 = S4; MATCH3- when AD03 = S3; MATCH2- when AD02 = S2; MATCH1- when AD01 = S1.

The Status Register Decode PAL (U92) reads the MATCH(4-1)-, STATUS-, AD17 through AD05, and BUSWR signals along with 64K and FULL board configuration signals to determine when the Error Status Register is being addressed. When the register is addressed, STATAD goes high from the PAL (U92) and is gated with ARGUS Bus Address Valid (ADVAL) in U83 to enable the Error Status Register PAL (U75) onto the bus. STATAD is also gated with ADVAL in U84 to generate Address Acknowledge (ADACK-).

006-10. MEMORY BANK DECODING

The memory board has up to four banks of memory when fully loaded. Options -006 and -016, with only half the number of possible RAMs, use only Memory Bank 0 and Memory Bank 1. With options -006 and -016, the BANK1 signal from the Address Translation PAL (U86) is held low while the BANK0 signal selects Bank 0 or Bank 1.

The BANK1 and BANK0 signals indicate which memory bank is selected. BANK0 is driven by Address Bit AD15. BANK1 is driven by Address Bit AD18 when four memory banks are installed, and Address Bit 0 when two memory banks are installed. The Address Translation PAL (U86) reads ARGUS bus address lines AD15 and lines AD20 through AD18 along with board configuration signals 64K and FULL to determine how to drive BANK0 and BANK1 outputs.

006-11. ROW AND COLUMN ADDRESS DECODING

The RAMs on the memory board use a multiplexed address bus. Each RAM contains one storage cell for each possible combination of row and column addresses. Row and column addresses are read in on the same pins in any given RAM and must be decoded. Refer to Table 006-2.

The lowest order AGGIE address bits provide the row address. The next higher AGGIE address bits are used for the column address, except for AD15, which is used for memory bank decoding.

The 64K-bit RAMs used in options -006 and -007 require 8 bits each of row and column address. The 256K-bit RAMs used in options -016 and -017 require 9 bits each of row and column address. On options -006 and -007, the

unused bit (pin 1) is held high to inhibit the automatic refresh function that is activated when pin 1 is pulled low.

The Address Translation PAL (U86) reads AGGIE bus address lines AD18 and AD15. Together with the configuration signal 64K, it multiplexes either AD18, AD15 or 1 to the RAM address line 8 (RAD8). Select Column (SELCOL) causes the PAL to switch from row address to column address. SELCOL is low during row address and high during column address. The remaining AGGIE address bits are multiplexed using 3 non-inverting buffers, which are controlled by the Refresh Controller PAL (U82). U95, U87, and U96 drive the row, column, and refresh addresses to the RAM address lines or are tri-stated.

006-12. Data Flow

Data flow between the bus and the memory is affected by parity checking and word mode operations.

006-13. PARITY DATA

To ensure the integrity of the memory on the board, each byte contains an extra bit. During a write operation, this parity bit is set or cleared so that the total number of bits in the byte is an even number. During a read operation, the bits are examined for even parity. If parity is not even, an error is reported.

During a write cycle the data flows from the bus through bidirectional buffers (U73 and U74) to the memory chips. In addition, the data is present on the inputs of the parity chips (U97 and U77) ready to generate parity data. Parity Even-byte Input (PEIN) and Parity Odd-byte Input (POIN) will be set if the data bytes on their parity chips contain an odd number of 1's. These two parity bits are then presented to two memory chips. The data bytes, along with their parity bits, are strobed into the RAMs for storage. During a write cycle Parity Even-byte Output (PEOUT) and Parity Odd-byte Output (POOUT) are tri-stated from the RAMs and pulled up by Z6.

During a read cycle the data is driven from the memory chips and flows through buffers (U73 and U74) onto the bus. The data is also present at U97 and U77. PEOUT and POOUT are no longer tri-stated, but contain the original parity information. The parity chips generate PEIN and POIN, which are high when data is correct and go low if the number of bits is in error.

006-14. WORD MODE

During memory cycles, data is transferred between the bus and memory using word mode. In word mode, data is

Table 006-2. Address Decoding

WHEN	RAD0 – RAD7 BECOME	RAD8
Row address time	AD01 – AD8	1
Column address time	AD09 – AD14, AD16, AD17	1
Refresh time	RFR0 – RFR7	1

transferred 16 bits at a time. Each time a read or write operation occurs, a bank of 18 (16 data + 2 parity) bits are accessed.

When in word mode, the BMODE- signal is high on the bus, and flows through an inverting buffer (U79) to become BMODE, which is low. BMODE is fed into a dual 4-input multiplexer (U88) to control the address of inputs that will select odd and/or even bytes. With BMODE low, the address on the multiplexer is either 0 or 1 (S1 = 0, S0 = 1 or 0), which always selects I(0 or 1)A and I(0 or 1)B inputs on the multiplexer. Since these four inputs are grounded, EVEN- and ODD- go low to select the even and odd data bytes for transfer.

006-15. Memory Cycle Generation

See Figure 006-5 for a functional block diagram of the Memory Cycle Generation circuitry. The memory cycle circuitry generates key signals for the dynamic RAMs on the memory board. During a read cycle, information is exchanged with a dynamic RAM by presenting a stable row address to the RAM, strobing it into the RAM, and holding it stable for a short time. Then a stable column address is presented, strobed into the RAM, and held stable.

During a write cycle, information is exchanged in the same manner as during a read cycle. Then a stable column address and valid data are presented, and the column address is strobed into the RAM. The column address and valid data are held stable. Overall bus access timing of data from the RAMs is shown in Figure 006-6.

A simple state machine (U81, U76) controls the generation of the Row Address Strobe (RAS-), the Column Address Strobe (CAS-), and the end of the cycle (CYCLE-). See Figure 006-7 for a timing diagram of the state machine.

When the memory board is being addressed, RAM Address (RAMAD) is active high and RAMAD- is active low. The inputs to a JK flip-flop (U81) will cause it to clear if it is clocked. If the AGGIE bus contains a valid address (AGVAL is active high) and INHIBIT- is inactive high, the two signals will be gated together (in U83) and the JK flip-flop will be clocked. This will trigger the start of a memory cycle.

The output of the flip-flop will go low to generate RAS-. On the rising edge of SYNC-, a second JK flip-flop (U81) is clocked and its Q output drives CAS- low. The Q-output of the flip-flop produces CAS active high. CAS passes through an inverting buffer (U80) to produce four identical CAS- signals (CAS3- through CAS0-) that drive

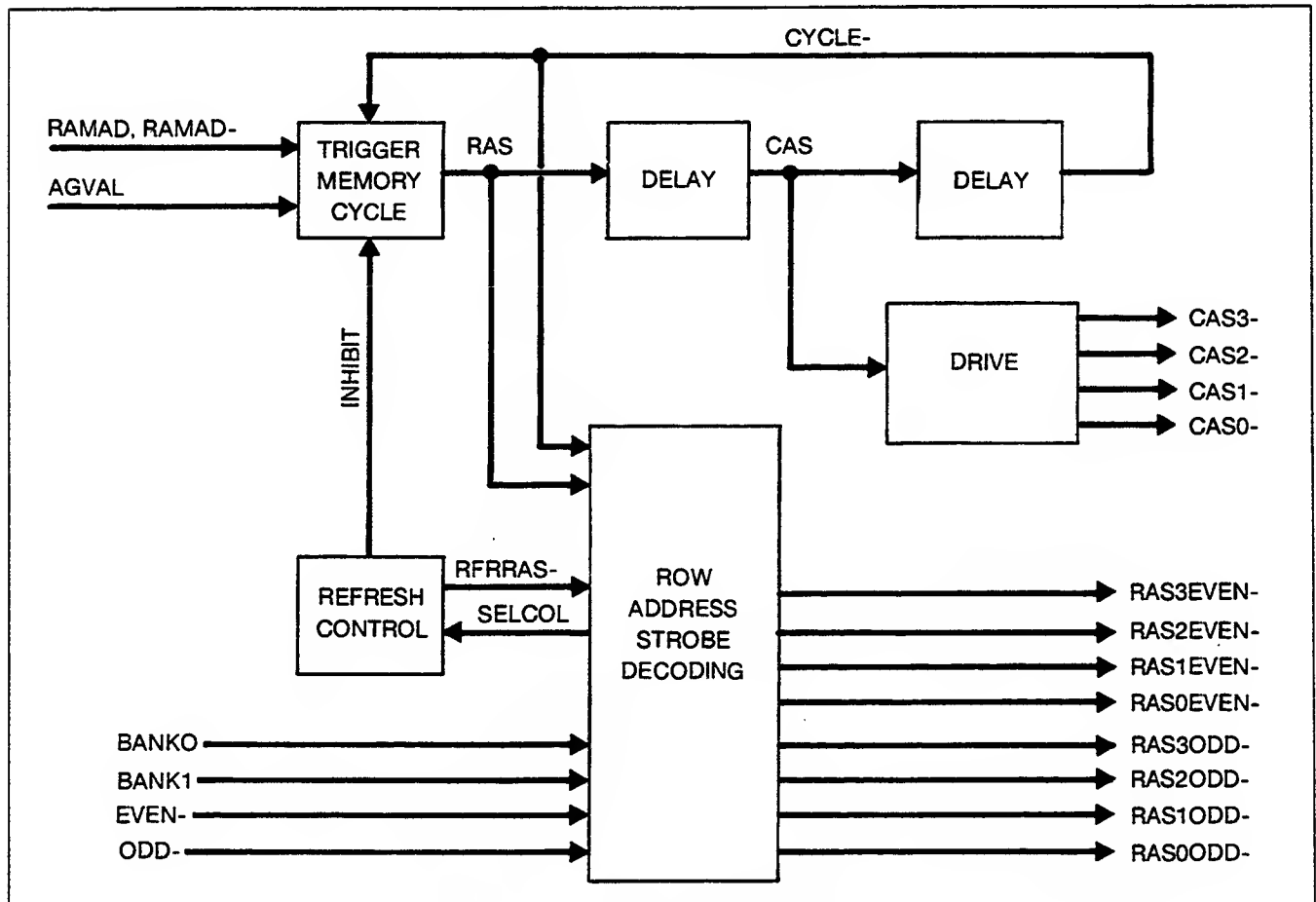


Figure 006-5. Memory Cycle Generation Circuitry

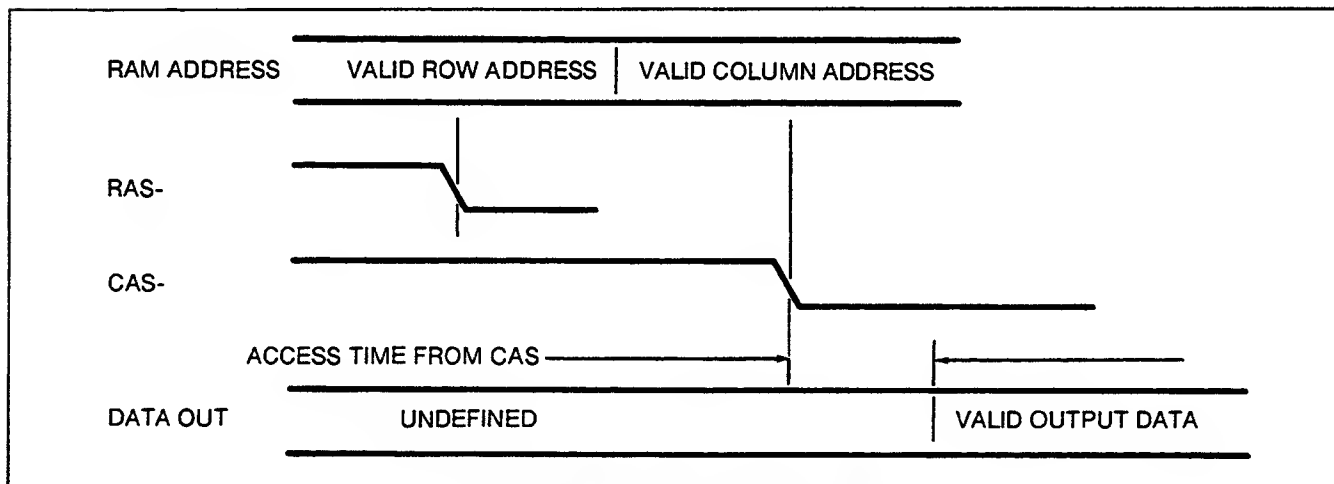


Figure 006-6. Bus Access Timing

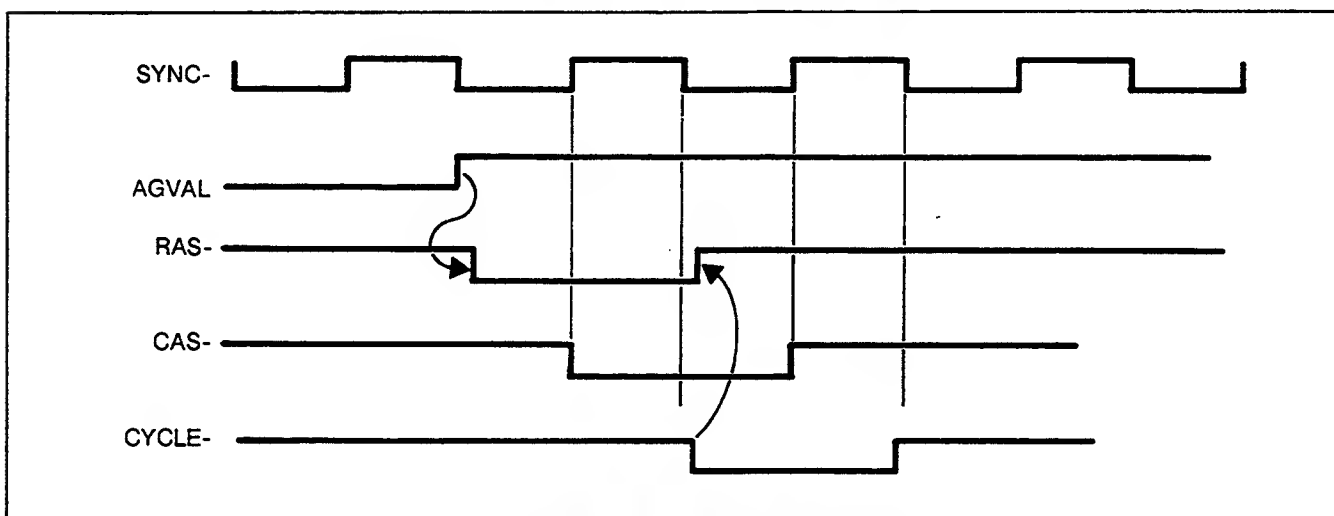


Figure 006-7. Memory Cycle Timing

memory array Banks 3 through 0. Once CAS- is low, on the falling edge of SYNC-, a D flip-flop (U76) is clocked and drives CYCLE- low. CYCLE- removes RAS- by clearing the JK flip-flop that generated it. Once RAS- is inactive high, on the rising edge of SYNC-, the second JK flip-flop (U81) is clocked and drives CAS- into the inactive high state. On the falling edge of SYNC- the CAS-signal is clocked into the D flip-flop and drives CYCLE- into the inactive high state. This completes the memory state machine cycle. The state machine can now be retrig-gered when memory is accessed from the bus.

006-16. RAS DECODING

Since the memory on the board is organized into several banks and not all of the banks are accessed during a memory cycle, the RAS signal must be decoded to select the correct memory bank. The single RAS signal from the state machine must be routed to two of eight separate RAS signals to the RAMs.

First, the memory bank code contained in BANK1 and BANK0 selects one of four outputs. The memory bank select signals (BANKSEL3- through BANKSEL0-) designate one of the four memory banks for data transfer. A multiplexer (U88) determines whether data transfer will take place with the even, odd or both bytes. Its outputs, EVEN- and ODD-, will be active low once the address on the bus has stabilized.

BANKSEL3- through BANKSEL0- are fed to two mul-tiplexers (U91 and U89). The select signal of one mul-tiplexer is driven by EVEN- while the other is driven by ODD-. When active low, EVEN- selects U91 and ODD-selects U89. The bank select signals are then latched through U93 and U90. When the odd byte is selected for data transfer, one of the BANK3ODD through BANK0ODD signals will be driven active high. When the even byte is selected, one of the BANK3EVEN through BANK0EVEN signals will be driven active high.

The D flip-flops (U93 and U90) drive the inverted version of the active high bank selects onto their Q- outputs when RAS- falls. The eight outputs are then gated with the Refresh Row Address Strobe (RFRRAS-) in two OR gates (U102 and U103) to produce the RAS signals to the RAMs. The RAS signals then travel through impedance matching resistors and arrive at the memory array.

The last part of the memory cycle multiplexes the row and column addresses to the memory array. When the RAS signals arrive at the memory array, they also arrive at the inputs of an 8-input OR gate (U101). Its output (SELCOL) signals when the RAM address should be switched from the row to the column address. SELCOL goes high and signals the Refresh Controller PAL (U82) to drive its MUXROW- output high. This de-selects the row driver (U95), and tri-states the row address to the memory array while driving its MUXCOL- output low to select the column driver (U87).

006-17. EFFECTS OF REFRESH

During refresh, the memory array cannot be used for data transfers. To prevent devices from using the memory, the Refresh Controller PAL (U82) drives INHIBIT- low. INHIBIT- is gated with AGVAL in U83, which causes the clock input to the JK flip-flop (U81) to remain high so that a memory cycle cannot be started. INHIBIT- is also gated with RAMAD, which forces ADACK- to remain high. With ADACK- high, the board will not respond with an address acknowledgement if addressed during refresh.

A short refresh cycle prevents a timeout caused by a bus cycle attempting to use the memory. Once normal use of the memory board is inhibited, the Refresh Controller (U82) drives MUXROW- and MUXCOL- high to de-select the row and column address buffers (U95 and U87) during refresh. At the same time, MUXRFR- is driven low to enable the refresh address to flow from the Refresh Address Counter (U100) through a driver (U96) to the RAM address lines (RAD7 through RAD0).

006-18. Refresh Control and Arbitration

The refresh control and arbitration circuitry times the refresh of the memory array and arbitrates with the devices on the AGGIE bus for access to the memory array. This circuitry is essential to the operation of the memory board because the electrical charges stored in the dynamic memory chips lose their charge over time. Reading to or writing from a storage cell refreshes the charge. To refresh the information at any given location, the location must be addressed and held stable while the RAS- signal to the RAM containing the storage cell is cycled low and then high.

The Refresh Controller PAL (U82) arbitrates with other devices for control of the memory, keeps track of when refresh should be performed, and provides the next refresh address to the memory. Arbitration overcomes the conflict in the dynamic RAM between use of the memory array for data storage and the need to refresh for data retention.

To determine when a refresh cycle is needed, the Refresh Controller PAL (U82) monitors the Refresh Timer (U78). The refresh timer is clocked by SYNC. Once the timer indicates that it is time to refresh, the Refresh Control PAL waits for any ongoing memory cycle to finish. The RAM select signal (RAMSEL-) is low when a memory cycle is underway. Once RAMSEL- goes high, the Refresh Control PAL asserts INHIBIT- to inhibit use of the memory by other devices while it performs the refresh.

Once the refresh address has stabilized at the RAMs, the Refresh Controller PAL asserts the Refresh Row Address Strobe (RFRRAS) high. The rising edge of RFRRAS clears the Refresh Timer (U78). RFRRAS also passes through an inverter (U79) and into two quad OR gates (U102 and U103) to generate all 8 of the RAS signals. The Refresh Controller PAL then drives RFRRAS low. The Refresh Address Counter (U100) is incremented to the next refresh address and the Refresh Timer (U78) is released to begin timing the next refresh interval.

The Refresh Controller PAL then drives MUXRFR- high to disable the Refresh Address Driver (U96) and drives MUXROW- low to enable the Row Address Driver (U95) for any subsequent memory cycles. The Refresh Controller ends the refresh cycle by driving INHIBIT- inactive high, allowing other devices to use the memory array.

006-19. Error Detection and Reporting

Error detection notifies a device using the memory board that data corruption has occurred. There are two types of errors that can occur within memory. A hard error is a permanent error caused by a hardware failure. A soft error is normally caused by an alpha particle hitting a storage cell and upsetting its stored charge. Soft errors can also be caused by noise or timing problems. Soft errors can be corrected by rewriting the storage pattern into the corrupted cell.

A device testing the board can determine whether an error is soft or hard by attempting to change the sense of the bit in error. If it can be changed, it is a soft error. If it cannot be changed, it is a hard error.

006-20. BYTE PARITY

Even byte parity is used in the memory expansion options to detect errors. Each byte of RAMs in the memory array includes a parity storage RAM that holds a parity bit. The parity bit operates as a check bit, detecting parity errors when an odd number of bits are corrupted. Since most errors are of this type, even byte parity will detect the majority of errors.

Each byte of incoming data flows through a bidirectional buffer (U74 and U73) and arrives at the RAMs. Each byte is also presented to the A through H inputs of a Parity Generator/Checker (U97 and U77). During the write cycle, the Parity Even-byte Output (PEOUT) and Parity Odd-byte Output (POOUT) lines are tri-stated from the RAMs, pulling up the INPUT lines of the parity generator/checkers.

An odd number of 1's presented on input lines A through H will combine with the extra 1 from the pull up on the input, causing the parity checker to see an even number of 1's and the SUM-even output to be driven high. This high signal is stored in the parity RAM along with the original byte to form a 9-bit pattern with an even number of 1's.

An even number of 1's presented on input lines A through H will combine with the extra 1 from the pull up on the input line, causing the parity checker to see an odd number of 1's and the SUM-even output to be driven low. This low signal is stored as the parity bit along with the original byte to form a 9-bit pattern with an even number of 1's.

006-21. ERROR DETECTION

During a read cycle, the error detection circuitry examines the parity data. The state of CAS-, just prior to the rising edge of SYNC-, signals when data is valid for sampling. At this time, the data and parity information from the RAMs has been checked by the parity checkers and their outputs are stable.

A read cycle is initiated by the device using the memory board, and RAS- is generated to the RAMs. Shortly thereafter, CAS- goes low to signal the RAMs to output their data. The data and parity information for each byte of the word being read appears at the input of the two parity generator/checkers (U97 and U77). During a read cycle, the PEOUT and POOUT lines are not tri-stated, but contain the parity bit for the even and odd byte, respectively. If there is no error, the SUM-even output of the parity checker will be driven high. If an error has occurred with the byte, the SUM-even output will be driven low.

The SUM-even outputs of each parity checker are monitored by the Error Status Register PAL (U75) along with the CAS- and BUSWR signals. If either of the outputs of the parity checkers goes low when BUSWR = 0 and CAS- = 0, the Error Status Register PAL notes which bytes of the word being read are in error and begins the error reporting process.

006-22. ERROR REPORTING

The Error Status Register PAL (U75) keeps track of the byte(s) containing the error and of the memory bank in which the byte in error is located. The PAL also initiates an interrupt on the AGGIE bus to report the error to the device. (Refer to paragraph 006-9, Error Status Decoding.)

When BUSWR is low, a read cycle is underway and parity data will be sampled for errors. When STATSEL- is low, the Error Status Register is being read by an external device. This causes EVENERR-, ODDERR-, EBNK1-, and EBNK0- to leave tri-state and drive the bus. When high, these signals keep track of the error status within the Error Status Register PAL and are tri-stated externally to the PAL.

When CAS- is low during a read cycle (BUSWR = 0), the Parity Generator/Checker outputs will be sampled to check for errors. When CAS- and BUSWR are low, and PEVEN- is low, there is an error in the even byte being read. When

CAS-, BUSWR AND PODD- are low, there is an error in the odd byte.

The Error Status Register PAL determines the location of an error using the BANK1,0 signal, which contains the 2-bit binary code of the memory bank being read. When the Refresh/Interrupt signal (RINT-) is low, devices can gate their interrupts to the controlling device onto the bus. This signal also tells devices on the bus when they may use a data line to assert an interrupt.

The interrupt request line (INTREQ-) is active when an error has been detected by the Error Status Register PAL. INTREQ- is driven active low when RINT- goes low, signaling that interrupts may be asserted on the bus. When RINT- is high or when there are no errors on the board, INTREQ- remains tri-stated. At that time, all memory boards containing parity errors will assert active low interrupt requests on Interrupt Level 11. All the interrupts are either low or tri-stated.

The Error Status Register automatically clears itself and begins monitoring for new errors once it has reported an error to the device using the memory. Information regarding an error can only be read once. It will be cleared immediately following the read operation.

006-23. TROUBLESHOOTING THE MEMORY EXPANSION OPTIONS

Component-level troubleshooting is recommended only when it is not possible to replace a defective module. If you attempt to repair a module, you will need, at a minimum, the following equipment: a multi-trace oscilloscope, a digital multimeter, a logic probe, and replacement ICs. Most chips are soldered into the circuit board, so it will be necessary to unsolder DIP ICs in order to swap them.

CAUTION

Use extreme care when removing and replacing components to avoid irreparable damage to the multi-layer printed circuit assemblies (pca's).

If the -006 or -007 module is failed by the System Diagnostic Software, the following troubleshooting procedures may be used to isolate the failure. If the procedures fail to isolate the cause in conjunction with standard troubleshooting techniques, return the option to a Fluke Service Center or the Module Exchange Program.

The most common problems occur in three major areas:

- Memory Chip Failure
- Address Decoding Problems
- Control Logic or Timing Problems

If the System Diagnostic indicates a variety of different problems, suspect that the PALS are bad and replace them. See Section 4 for a list of replacement PALS.

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

006-24. Memory Chip Failure

SYMPTOM 1:

The System Diagnostic indicates a memory chip failure and no other faults.

POSSIBLE CAUSE:

A bad memory chip.

ACTION:

Replace the chip.

SYMPTOM 2:

Two or more RAM chips fail the System Diagnostic tests.

POSSIBLE CAUSE:

Not likely to be in the RAM chips themselves. Unless there has been a catastrophic accident to the board, the probability of more than one bad RAM chip is very low.

ACTION:

If multiple errors are indicated, don't replace the chips. Check further for data and address errors.

SYMPTOM 3:

The System Diagnostic reports a memory bank address error.

ACTION:

Consult Table 006-3 to locate the memory bank in error.

SYMPTOM 4:

The System Diagnostic reports failures in only the upper or lower byte of the RAM Array.

POSSIBLE CAUSE:

The RAM array is faulty.

ACTION:

Check the data buffers (U73 and U74), or the Byte Mode logic (U88, U89, U90, U93, U102, and U103).

If the fault is isolated to the Byte Mode logic, check for activity on U88, pins 4 and 13. Check that pin 1 of U89 and U91 is low. Check U90, U93, U102, and U103.

006-25. Address Decoding Problems

SYMPTOM 5:

The System Diagnostic reports the incorrect amount of RAM.

POSSIBLE CAUSE:

Address Translation PAL (U86) is bad.

ACTION:

Replace U86.

SYMPTOM 6:

The System Diagnostic reports several address bits in error.

ACTION:

Check the address buffers, U94 and U79.

Replace the Refresh Controller PAL (U82) and check the activity on pins 5, 6, 7, and 8. If there is no activity, suspect the refresh logic.

Check the Refresh Timer (U78), and U100.

SYMPTOM 7:

Table 006-3. Memory Bank Location

OPTION	DEVICES	MEMORY	BANK LOCATIONS
17XXA-006	36	256K bytes	BANK0 xx(0-7)xxx
17XXA-016	36	1M bytes	BANK1 xx(8-f)xxx
17XXA-007	72	512K bytes	BANK0 x(0-3,8-b)(0-7)xxx
17XXA-017	72	2M bytes	BANK1 x(0-3,8-b)(8-f)xxx BANK2 x(4-7,C-f)(0-7)xxx BANK3 x(4-7,C-f)(8-f)xxx
NOTE: x=(0-F)			

Several different data bit errors and different address line errors are reported.

ACTION:

Check data buffers U73 and U74. Check the RAM select signal at U82, pin 3. Also check U83.

Check the refresh logic at U82, U78 and U100 for activity on the pins.

SYMPTOM 8:

No data bits are reported and one address line is failed by the System Diagnostic.

ACTION:

Start at the address line signal destination and work backward until you locate signal activity. Check for valid logic levels. Check Address Decoding PAL (U86) to make sure that all address lines are valid at the chip.

SYMPTOM 9:

1722A reports that many memory options are installed or options appear at addresses that don't match the switch settings.

POSSIBLE CAUSE:

Board Select Switch circuitry is bad.

ACTION:

Open all switches, then close them one at a time and check for correct logic levels at U98 pins 2, 5, 10, 12, and U99 pins 2, 5, 9, and 13.

Check Address Buffer U94 to make sure that address signals AD01 - AD04 and AD18 - AD21 reach U98 and U99 from the card edge connector.

Check that the address match signals from U98 and U99 reach the Address Decoding PAL (U86) and Status Register Decode PAL (U92).

SYMPTOM 10:

The System Diagnostic indicates that the controller doesn't recognize the board or that the board is not installed.

POSSIBLE CAUSE:

Address decoding is not reading the switch properly.

ACTION:

Check the address switch. Also check U92 and U84.

Check U86's RAM address line, output pin 16, for activity and valid logic levels. If pin 16 goes low, everything back to the ARGUS bus is good. If there is no activity, suspect gates U98 and U99 in the Address Decoding Circuitry or buffer U94.

Also see Symptom 11 under Control Logic and Timing Problems.

006-26. Control Logic and Timing Problems**SYMPTOM 11:**

The 1722A reports that no memory options are installed.

POSSIBLE CAUSE:

Memory timing and control logic may be bad.

ACTION:

Probe TP5 and TP6 and see if these signals go active when the 1722A attempts to access the memory option.

SYMPTOM 12:

The System Diagnostic reports an error in U100, U96 and/or other components in the Memory Refresh Logic.

POSSIBLE CAUSE:

The Refresh Address Counter (U100) may not be counting properly.

ACTION:

Use an oscilloscope to probe pins 3, 4, 5, 6, 8, 9, 10, and 11.

POSSIBLE CAUSE:

The Refresh Address Buffer (U96) may not be working properly.

ACTION:

Use an oscilloscope to probe pins 1 and 19. U96 should be enabled every 15.6 us.

Trigger the oscilloscope on pin 1 or 19, and check the logic level. The logic level should be the same for the output and input.

Check that U87, U95, and U96 are not enabled at the same time.

Option 17XXA-008

IEEE-488/RS-232-C Interface

008-1. INTRODUCTION

The 17XXA-008 IEEE-488/RS-232-C Interface option doubles the number of communications ports for the 17XXA, providing additional bi-directional data and control exchange between the Instrument Controller and compatible external devices. The 17XXA Single Board Computer (SBC) has a single IEEE-488 port and a single RS-232-C port. The IEEE-488 port device name is GPO: when used as an output device and Port 0 when used by a program as an instrument port. The RS-232 port device name is KB1:.

On the 17XXA-008 option, the IEEE-488 port has the device name GP1: or Port 1, and the RS-232 port has the device name KB2:. The ports are addressed by high level languages. The same FDOS drivers support both the standard ports (KB1: and GP0:) and the ports on the -008 option.

The 1722A and 1752A have 5 slots available for options. IEEE-488/RS-232-C Interface modules can be installed in slot 5 on the 1722A and in either slot 4 or 5 on the 1752A. Only a memory option can be used in the slot above an installed -008 option.

Circuitry is identical to the circuitry on the SBC, with the exception of the address decoding circuitry. On the 1722A, the RS-232-C port is tied to the local bus and address decoding logic resides on the SBC. On the -008 option, the RS-232-C port talks over the AGGIE bus rather than the SBC local bus. Since it is not on the same board as the SBC, it requires its own address decoding circuitry.

The configuration switch on the interface option is identical in function to the one indicated on the SBC. (See Figure 2-4 for switch settings for the -008 option.)

008-2. THEORY OF OPERATION

008-3. Functional Description

For the following discussion, refer to the block diagram in Figure 008-1 and the schematic diagram in Section 5.

008-4. Bus Interface

Port address decoding is implemented in the Address Decode PAL (U3), which generates the chip enable signals for the RS-232 Controller (U2) and the IEEE-488 Controller (U1).

The 17XXA-008 option communicates with the 1722A over the ARGUS Communications Register Unit (CRU) I/O bus. The CRU bus is a bit-mapped serial I/O address and data bus that resides on the ARGUS bus. CRU signals on the CRU I/O bus enable CRU I/O operations and detect valid data.

The control signal, Address Valid (ADVAL-) signals that a bus cycle is taking place on the ARGUS Bus. Address Decode PAL (U3) gates the signal through U7 and converts it to an open collector signal in U6, then presents the signal to the ARGUS bus as the Address Acknowledge signal (ADACK-).

The 9902 signal from the Control PAL (U4) enables RS-232 Controller (U2), a Universal Asynchronous Receiver/Transmitter (UART). 9902 is gated through U7 and U6 to produce an open collector output, which generates the Communications Register Unit Acknowledge (CRACK-) signal on the ARGUS Bus. The 9914 signal from U4 is applied to pin 19 of U3 and enables the IEEE-488 Controller (U1).

The Bus Write (BUSWR-) signal controls data direction on the ARGUS bus. When BUSWR- is low, the CPU is writing data. When BUSWR- is high, ADVAL is low, and an address is present, data is being read from the processor.

The UART (U2) also generates the Communications Register Out (CRUOUT), Communications Register In (CRUIN) and Communications Register Clock (CRUCLK) signals on the Communications Register Unit (CRU) bus.

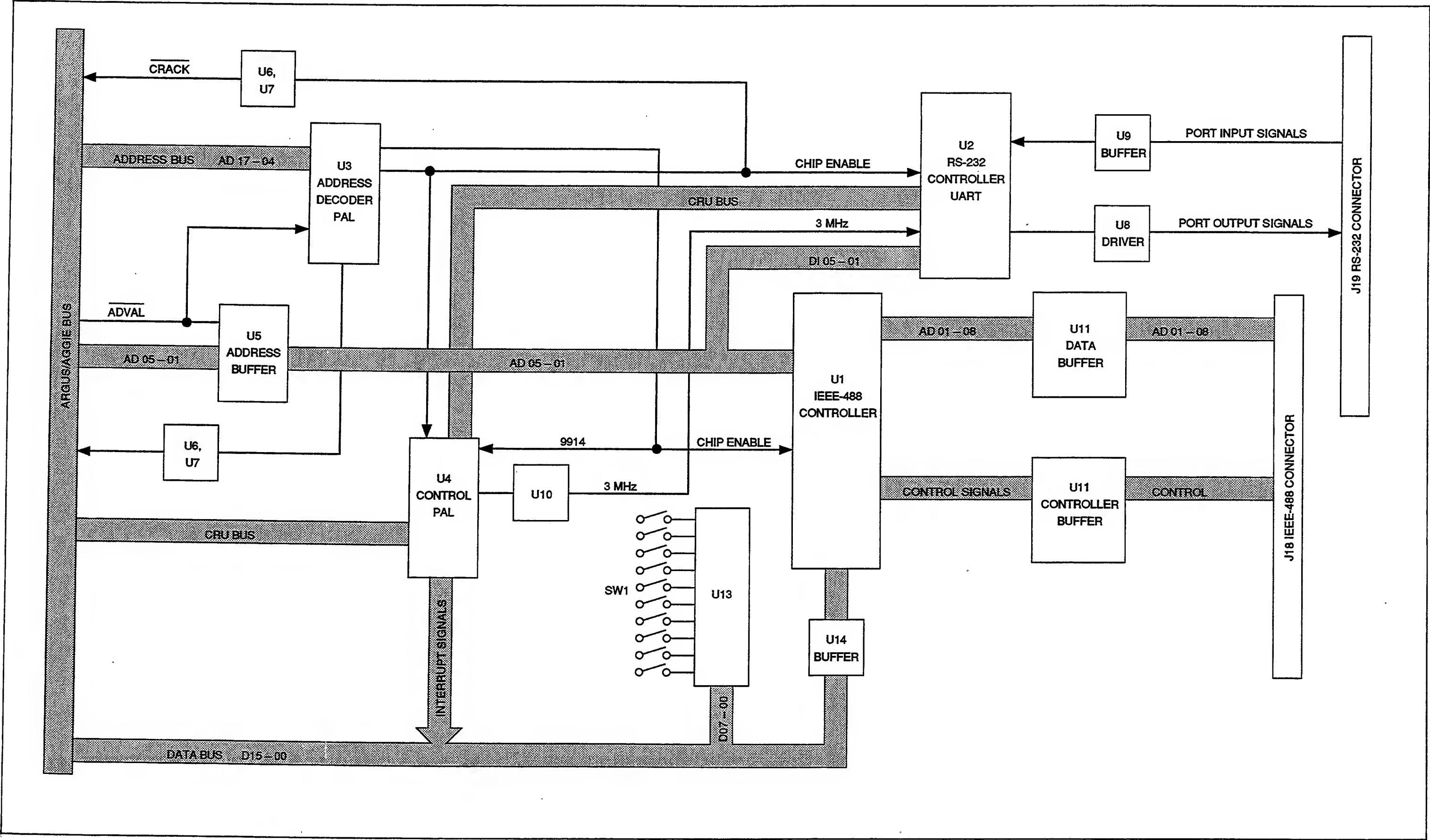


Figure 008-1. IEEE-488/RS-232-C Interface Module
Block Diagram

The Control PAL (U4) buffers bus control and interrupt signals, and initiates the timing functions for the 17XXA-008 option. INT10 provides the interrupts for U1 and INT06 provides the interrupts for U2. When Read Interrupt (RINT-) from the bus is active, interrupt requests may be placed on the data lines. RS-232 and IEEE timing functions are supplied by U10, which divides the Bus Clock Signal (SYNC-) in U4 from 6MHz to 3MHz.

Buffer U5 passes address lines AD05-01 to U2 and U1. S0-S4 address 32 bits within the RS-232 Controller. RS0-RS2 address 8 bits within the IEEE Controller.

008-5. RS-232-C INTERFACE

The RS-232-C Interface uses a TMS 9902N UART (U2), which is mapped in the SBC serial address space from 1F3E through 1F00.

The port input signals from the 25-pin RS-232-C Connector Jack (J19) to the RS-232 Controller are buffered by receivers U9 that are biased ON unless driven otherwise. A 10K Ohm resistor (Z1) and capacitors (C2-C5) bias the signals, allowing the interface to work with a minimum of connections. Line driver U8 converts the outgoing TTL signal levels used by the RS-232 Controller UART into the voltage levels required by the RS-232-C protocol. Signals not controlled by the 17XXA are held ON by Z3. RS-232-C pinouts are shown in Appendix C.

Switches 2 through 4 on the ten position switch (SW1) select the baud rate for the RS-232-C port during power-up. Switch settings are read and interpreted by software, except switch 5, which is reserved for the System Controller function. Switch settings for the RS-232-C Interface are shown in Figure 2-4.

008-6. IEEE-488 INTERFACE

The IEEE-488 Interface uses a TMS 9914A Controller (U1), which is mapped in the SBC's parallel I/O address space from 3F40E through 3F400. U1 implements bus control, synchronization, and data transfer on the IEEE port. Driver U13 communicates data and commands to complete the interface to the 17XXA. The IEEE-488 Controller (U1) controls bus transceivers U11 AND U12. U11 buffers data on data input lines 1 through 8. U12 buffers control and handshake lines to the 24-pin IEEE-488 Connector Jack (J18). The switch input (SC) in U12 implements the system controller function used on buses with more than one controller. See Appendix B for a pinout diagram of the standard IEEE-488 Interface Connector and a description of each of the signal lines.

Switches 6 through 10 on SW1 select the IEEE-488 port address. Switch 5 selects whether the port is to be a system controller. Except for the system controller function, the switch settings are read and interpreted by software. Whenever a data input from the IEEE-488 Controller occurs, the switch settings are read onto the data bus. See Figure 2-4 for switch settings for the IEEE-488 Interface.

008-7. BUS OPERATING SIGNALS

There are 16 signal lines on the IEEE-488 bus; all are active low TTL levels. The signals are divided into three categories:

- Five bus management lines, that operate in command mode
- Eight data lines, that operate in data mode
- Three handshake lines

The controller uses the command mode to control the various instruments connected to the bus. It places the system into command mode by sending an Attention signal (ATN). All devices on the bus must then interpret the data byte as a command message. Only a controller may issue commands.

Data mode is used to transfer information on the Data I/O lines. Data mode is implemented when the controller sets the ATN line false. All devices will then treat information on the bus as data. This data can originate from either a talker or the controller.

The three handshaking signals handle data transfers on the bus. The three signals are:

- Data Valid (DAV)
- Not Ready For Data (NRFD)
- Not Data Accepted (NDAC)

NOTE

Pin 12 is connected to the cable shield. This pin is not a reference point for signals. Its purpose is to connect the cable shield to a system ground. Use of this connection should not result in circular grounding paths (loops) through the system. Ground loops can conduct enough current to interfere with data transmission.

008-8. Multiple Controller Systems

Because the two ports are effectively two separate systems, both the standard IEEE-488 port and the added port can be set up as System Controller. However, if both ports are connected to the same bus, one of the ports must be set up as an idle controller.

The System Controller drives the control lines Interface Clear (IFC) and Remote Enable (REN). When it is powered up, the system controller is the controller in charge. There can be only one controller in charge on a port at a time and it is the only device that can send interface messages by setting the Attention (ATN) line true.

008-9. Power-up Configuration

When the IEEE Controller (U1) is read, switch SW1 appears in the lower byte. All positions are sensed except for position 5. Position 5 is reserved for the System Controller function.

008-10. BOARD ADDRESS SELECTION

Initial set-up establishes the module's IEEE-488 address as 0 and its function as System Controller. This configuration also sets the RS-232 port to 4800 baud for power up. Switch 1 is configured as shown in Table 008-1.

Refer to Figure 2-4 in Section 2 for other baud rate settings. The baud rate can also be changed using the SET Utility Program.

The controller in charge can pass control to an idle controller. When this happens the idle controller becomes the controller in charge and the former controller in charge becomes an idle controller. If the system controller sets the Interface Clear (IFC) line true, it gains control on the port and becomes controller in charge.

008-11. SET Utility Program

The purpose of the SET Utility program is to configure the Instrument Controller to enable it to communicate with other pieces of equipment that use the RS-232-C standard. The SET Utility Program permits changing the values of the parameters at the port. The port parameters are set to default values when the operating system is loaded.

The following port characteristics can be changed:

- Baud Rate (data or bit rate)
- Number of Data Bits
- Number of Stop Bits
- Parity
- End of Line and End of File Terminators (EOL affects data input. EOF affects both input and output data.)
- Stall Input/Output Enable/Disable (SI affects data being received at the serial port. SO affects data being sent from the Controller.) (ASCII XON/XOFF Protocol)
- Time out value (Affects input and output data.)

008-12. DIP Switch SW2

Some versions of this board have a DIP switch labeled "SW-2". This switch was intended to select the board number when multiple boards were allowed in a system

with FDOS 1.7 and 2.0. It was later found that the use of multiple -008 boards caused the system to exhibit problems with missed IEEE interrupts. This multiple board capability was removed in FDOS 2.1 and later.

This switch has been removed and replaced with two jumpers on board revision 'G' or greater. These jumpers are positioned to properly select the board. For boards with SW-2 installed, all four of the SW-2 positions should be in the "ON" or "CLOSED" position (regardless of the silk-screen indication.) SW-2 did not exist on boards revision 'C' or prior.

008-13. TROUBLESHOOTING THE -008 INTERFACE OPTION

System Diagnostic software is provided with the 17XXA to aid in identifying faulty modules. The software contains subtests for specific functions of the -008 option. The System Diagnostic for the RS-232-C port consists of Internal, External and Port-To-Port Loopback tests. The System Diagnostic for the IEEE-488 port consists of Internal and Port-to-Port Loopback tests. For more information on the System Diagnostic tests, see Section 3.

If an error is encountered by the System Diagnostic during the execution of a test, an entry is made in an error log. IF STOP ON FAIL was selected from the Main Menu, an error message will be displayed on the screen. If an error is reported, run the Dip Switch SW1 Status test to determine if the switches are correctly set, and re-run the original test. (For the correct switch settings, refer to Figure 2-4 and paragraph 2-44.) If the error condition persists, verify that the module is faulty and replace it. (If the System Diagnostic will not load and run, see Section 3, Troubleshooting.)

Component-level troubleshooting is recommended only when it is not possible to replace a defective module. To attempt to repair a module, you will need, at a minimum, the following equipment: a Circuit Board Extender (Fluke model number Y1704, P/N 518688 or equivalent), a Loopback Connector (Fluke P/N 732107 or equivalent), a multi-trace oscilloscope, a digital multimeter, a logic probe and replacement components. Since most components are soldered into the circuit board, it will be necessary to unsolder them for replacement.

CAUTION

Extreme care should be used when removing and replacing components to avoid irreparable damage to the printed circuit boards.

Table 008-1.Initial Switch Configuration

SWITCH 1									
1	2	3	4	5	6	7	8	9	10
OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

If the ports or board are failed by the System Diagnostic software, the following troubleshooting procedures may be used to isolate the failure.

008-14. Troubleshooting the RS-232-C Port

If Data is not being exchanged with the external device,

- Use the SET Utility Program to check the port characteristics (Data Rate, Parity, Number of Data Bits, Number of Stop Bits, Baud Rate, End of Line and End of File Terminators, Stall Input/Output Enable/Disable and Time Out Value). Verify that the port characteristics match those of the External Device.
- Verify that the correct cable is being used for the current external device configuration. See Table 008-2 to match the proper cable to the device configuration.
- If the problem persists, you will need an RS-232 Loopback connector, Fluke P/N 732107 to run the necessary tests.

The RS-232 Loopback Connector ties the Transmit and Receive (pins 2 and 3) and Request to Send and Clear To Send (pins 4 and 5) lines on the connector together, enabling the UART to transfer data to itself through the buffers.

- Faults can occur in three different signal groups. See Table 008-3 for descriptions of these signal groups.
- Attach the loopback connector to the port under test.
- Follow the steps in the troubleshooting procedure, Figure 008-2.
- If the System Diagnostic procedure fails to isolate the cause of trouble in conjunction with standard troubleshooting techniques, return the option to a Fluke Service Center on the Module Exchange Program.

008-15. Troubleshooting the IEEE-488 Port

If Data is not being exchanged with the external device,

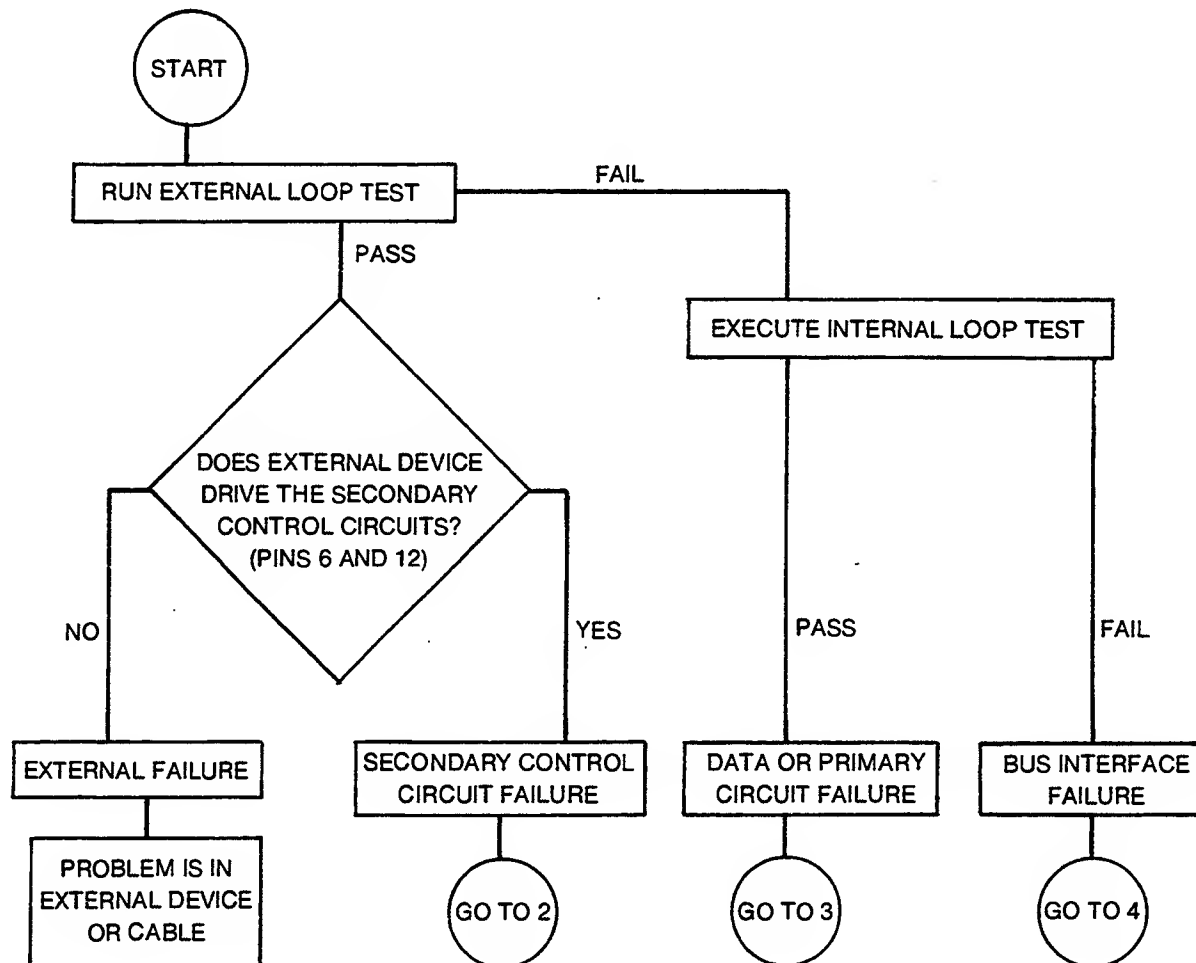
- Follow the steps in Figure 008-3.
- If the suggested procedures fail to isolate the cause in conjunction with standard troubleshooting techniques, return the option to a Fluke Service Center on the Module Exchange Program.

Table 008-2. Cable Verification

EXTERNAL DEVICE CONFIGURATION	CABLE
Data Communication Equipment (modems, etc.)	RS-232 (straight through) (Fluke model Y1707 or Y1708)
Data Terminal Equipment (terminals, computers, etc.)	Null Modem (signal pairs crossed) (Fluke model Y1702, Y1703 or Y1705)
Other (printer, plotter, etc.)	Null Modem (signal pairs crossed) (Fluke model Y1702, Y1703 or Y1705) or custom cable

Table 008-3. RS-232-C Functional Signal Groups

TYPE	NAME	PIN	NOMINAL CONNECTOR	VOLTAGES
Data	TXD	2	Mark (-3 -> -25V)	Space (+3 -> -25V)
Circuits	RXD	3	Mark (-3 -> -25V)	Space (+3 -> -25V)
Primary	RTS	4	ON (+3 -> +25V)	OFF (-3 -> -25V)
Control	CTS	5	ON (+3 -> +25V)	OFF (-3 -> -25V)
Secondary	DSR	6	ON (+3 -> +25V)	OFF (-3 -> -25V)
Control	SRLSD	12	ON (+3 -> +25V)	OFF (-3 -> -25V)



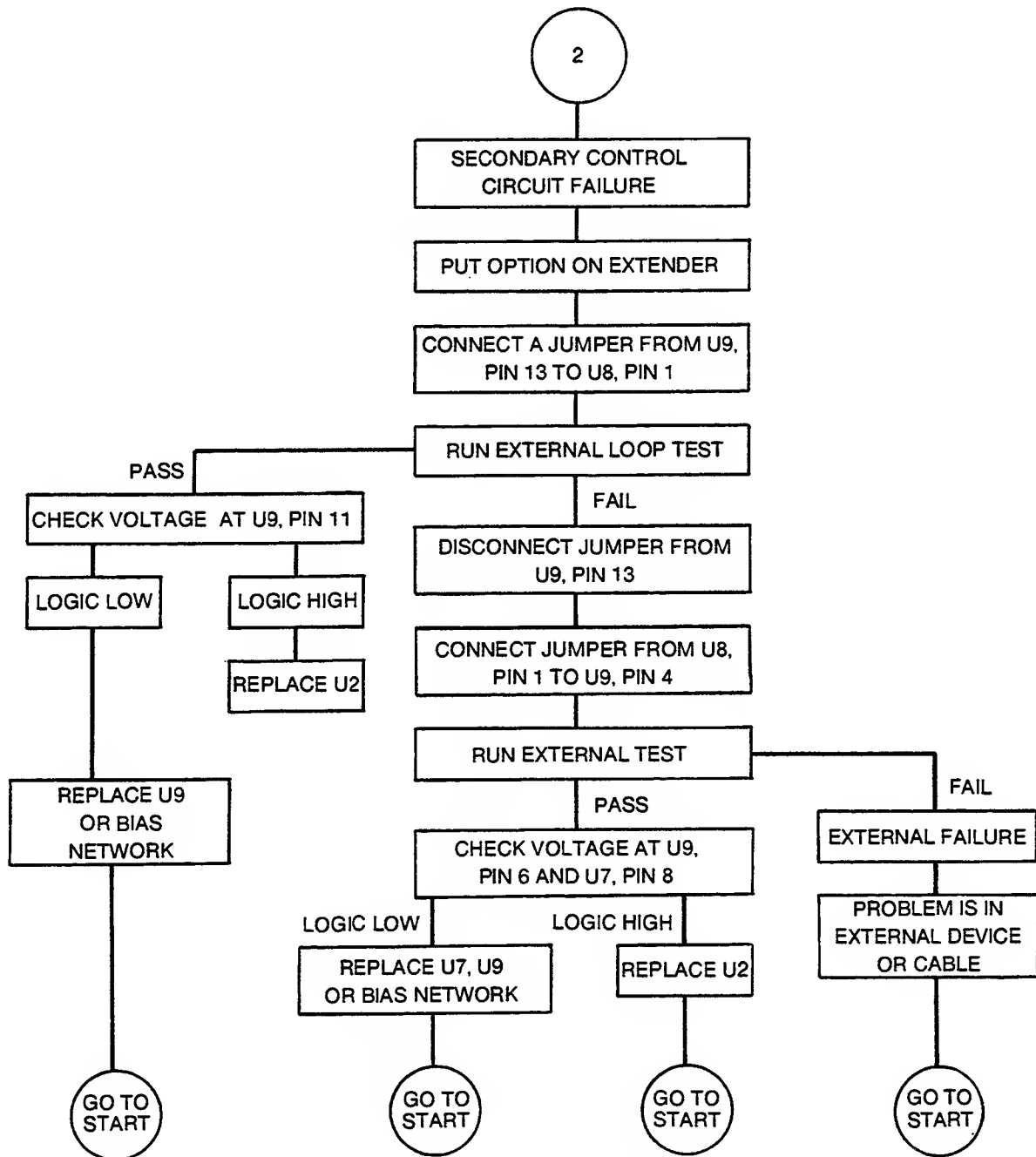
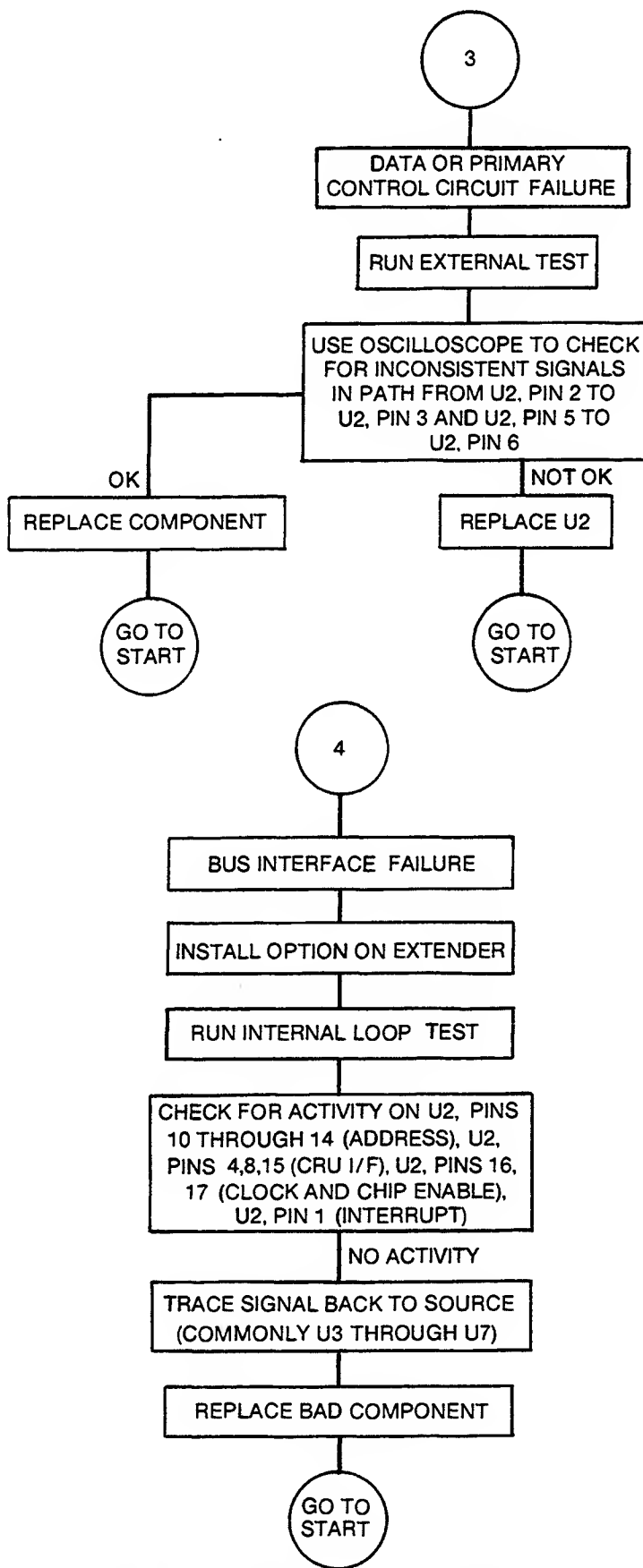


Figure 008-2. Troubleshooting the RS-232-C Port (cont)



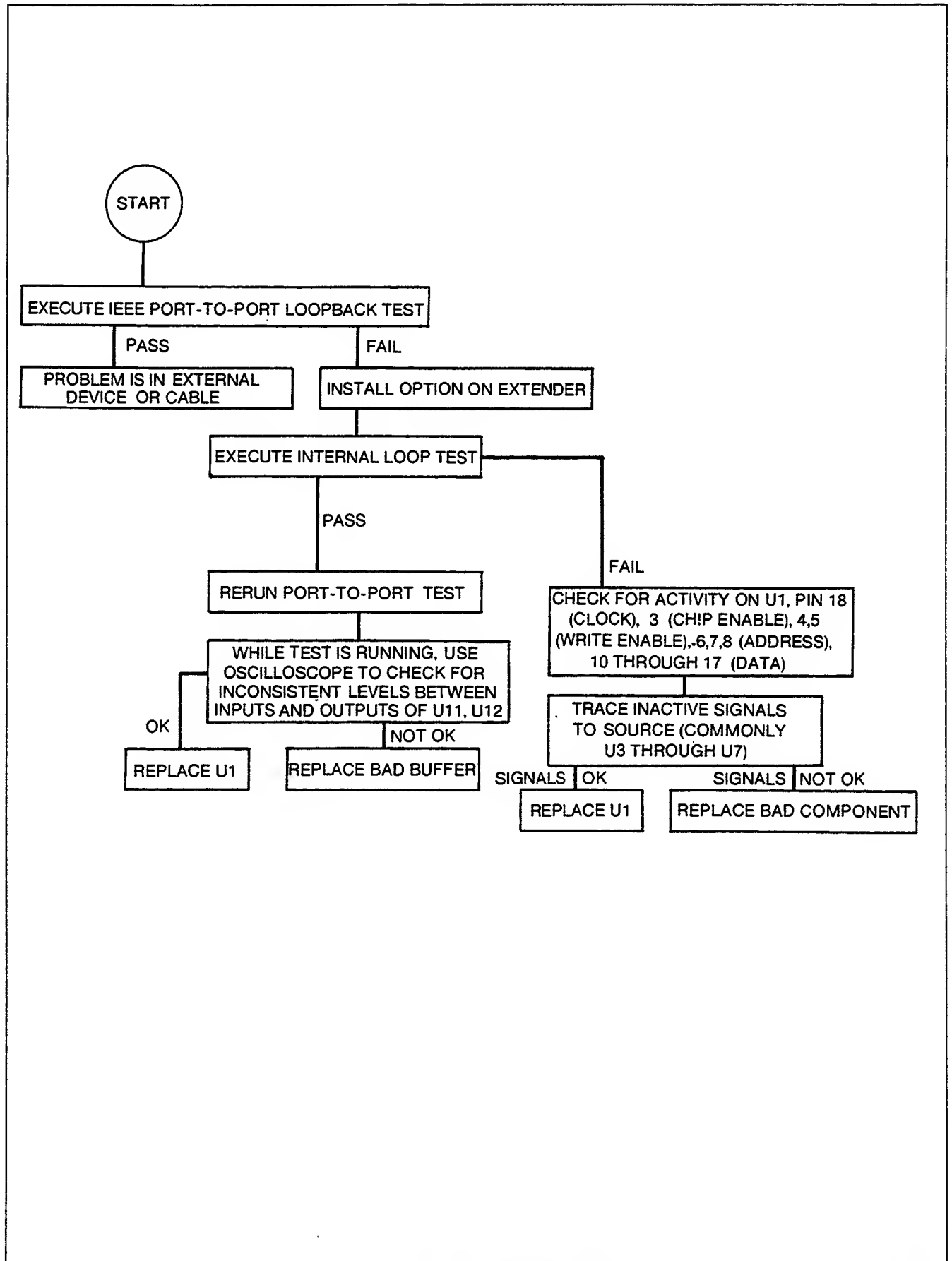


Figure 008-3. Troubleshooting the IEEE-488 Port (cont)

Option 17XXA-009 Dual Serial Interface

009-1. INTRODUCTION

Each 17XXA-009 Dual Serial Interface (DSI) provides the 17XXA Instrument Controller with two additional communications ports. The 17X2A accommodates up to three DSI modules, for a total of six serial ports per system. The 1711A/AA accommodates up to five DSI modules, yielding a total of ten serial ports per system. Each port may be configured for these electrical interfaces:

- RS-232-C
- RS-422/423
- 20 mA Current Loop

DSI ports are addressed as SPO: through SP9: through the SET Utility Program and high level languages. They are treated similarly to KB0: and KB1: on the Single Board Computer (SBC) and KB2: on the IEEE-488/RS-232-C Option (17XXA-008). SP0: through SP9: are supported by a different FDOS driver than KB1: and KB2:.

The SET Utility program configures the Instrument Controller to enable it to communicate with virtually any other piece of equipment that uses the RS-232-C standard. Different applications are accommodated by changing the values of the parameters at the port.

The following port characteristics can be changed:

- Baud rate (bit or data rate)
- Number of data bits
- Number of stop bits
- Parity

- End of Line and End of File Terminators
- Stall Input/Output Enable/Disable
- Time Out Value

Each port buffers incoming and outgoing data and signals the external device when the buffers are nearly full to prevent loss of data. The signaling method or protocol is user-selectable. The ports are controlled by a microprocessor that reduces the overhead on the SBC. System throughput is a function of the data being transferred at the floppy disk and the IEEE-488 and KBx: ports. If the load from these devices is heavy, external devices will be held off more frequently regardless of the data rate selected.

009-2. THEORY OF OPERATION

009-3. Functional Description

For the following discussion, refer to the block diagram in Figure 009-1 and the schematic diagram in Section 5.

009-4. Bus Interface

The Dual Serial Interface appears as a Universal Asynchronous Receiver/Transmitter (UART) in the serial address space (CRU) of the Single Board Computer (SBC). The CRU (Communications Register Unit) bus is a bit serial I/O bus that resides on the ARGUS bus. CRU signals on the CRU I/O bus enable CRU I/O operations and detect valid data. See Table 009-1 for a map of the CRU address space.

SBC UART (U8), Bus Interface UART (U7), and Port UARTs U116 and U216 use the Communications Register Out (CRUOUT), Communications Register In (CRUIN) and Communications Register Clock (CRUCLK) signals to communicate on the CRU bus.

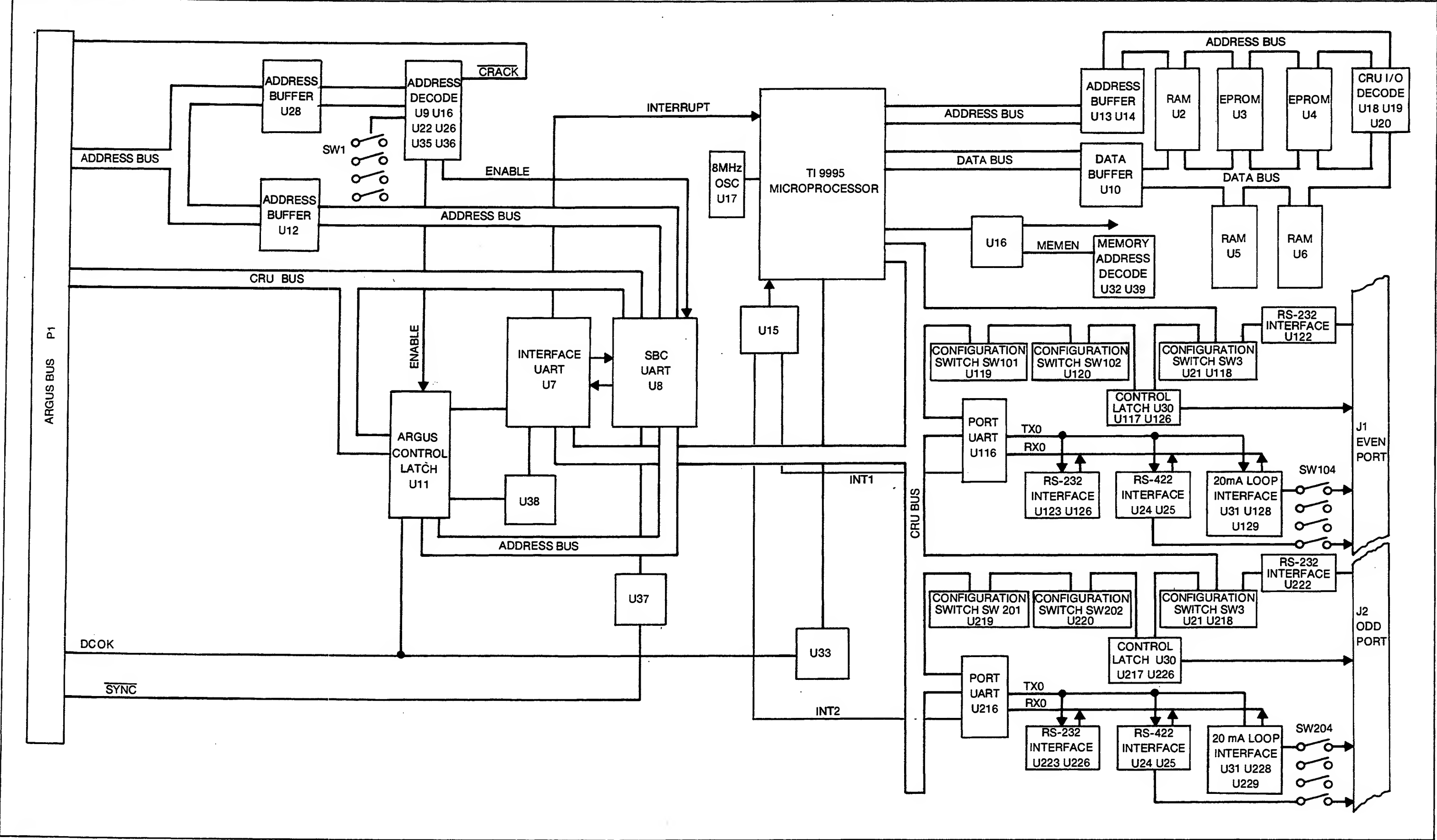


Figure 009-1. Dual Serial Interface Block Diagram

Within the 32 bits used by the SBC UART (U8), there are seven unused control bits. Control Latch (U11) is mapped into this space to allow the SBC to enable interrupts from U8 after gating the control line DI12 through U20 and U31. The Control Latch enables U7 through U22 and U38 to transmit by sending the Clear to Send signal (CTS). Table 009-2 shows the line addresses for the control line. The offset is added to the base addresses listed in Table 009-1.

Table 009-1. CRU Address Space

BOARD ADDRESS SWITCH	PORT	ARGUS CRU ADDRESS
0100	9,8	213e-2100
0011	7,6	20fe-20c0
0010	5,4	20be-2080
0001	3,2	207e-2040
0000	1,0	203e-2000

Table 009-2. Control Line Addresses

OFFSET	BIT	FUNCTION
1b	27	ABIT2 Readable by 9995 (not used)
1a	26	ABIT1 Readable by 9995 (not used)
19	25	DINT Enable Interrupt from DSI
18	24	CTS Clear to Send (to DSI)

Control latches U117 and U217 are mapped in the DSI's serial address space, and gate the CTS signal through U22 and U37 before sending it to the SBC UART (U8) to enable it to transmit.

The SBC UART (U8) timing functions are enabled by flip-flop U37, which divides the AGGIE Bus Clock Signal (SYNC-) from 6MHz to 3MHz. The 2MHz Clock Out (CLKOUT) signal from the DSI microprocessor (U1) drives the timing functions for the Bus Interface UART (U7). The UARTs (U7, U8) are connected back to back to allow transfer of only one character at a time. Flip-flop U38 sends its CTS input to U7 and flip-flop U37 sends its CTS input to U8. When a character is received by either UART, the INT pin is set low to notify the DSI microprocessor that a character is available. When the INT pin is low on the receiving UART, a Not Clear to Send input is sent to the transmitting UART. The microprocessor reads the character and returns the INT pin de-asserted, allowing another character to be sent. U7 and U8 may also be held off by the control lines (Q0, AUART-) that enable the flip-flop inputs through U22.

ARGUS Bus Address Decoding Logic enables the SBC UART (U8) or Control Latch (U11). AGGIE Bus address lines AD05 through AD01 are buffered by

Address Buffer U12 and passed on to the decoding logic (U9, U16, U22, U26, U35, U36), the Control Latch and the SBC UART. Address lines AD12 through 6 are buffered and inverted by U28 and gated with Board Address Switch SW1 in U36. When all bits match, U16 returns the Communications Register Unit Acknowledge signal (CRACK-). Depending on the outputs of U22 and U16, either U11 or U8 is enabled. The LATCH signal, asserted by U16, enables U11. U8 is enabled by LATCH-, which is asserted by U22.

009-5. Kernel

The Dual Serial Interface is controlled by a TI 9995 microprocessor (U1). An 8MHz oscillator (U17) drives the microprocessor, which divides the clock signal (CLKIN) to 2MHz at the CLKOUT pin. U1 normally runs without wait states. At power up, U15 holds READY low and at the release of RESET, U15 invokes the No Wait State mode. RESET is driven by U33 and the bus reset signal DC Power OK (DCOK). DCOK is low when the controller is cold booted.

Interrupts from the Port UARTs (U116, U216) are gated through U16 and appear on the INT1 pin of the microprocessor. Since data must be read before the next character is received, this is the highest priority interrupt. The Bus Interface UART (U7) drives INT4. Since the handshake with the SBC UART is of lesser importance than incoming data, this is the lowest priority interrupt.

Address lines PA0-15 are buffered by Address Buffers U13 and U14. Data lines are buffered by a bidirectional buffer (U10) that enables the data bus only during a read or write operation. Both busses are distributed to the system memory and memory decoding on Address lines IA0 through IA15 and Data lines ID0 through ID7.

Static RAMs U2, U5 and U6 comprise the interface workspace and Port Data Buffers, and are 2 Kbytes each. The interface firmware resides in EPROMs U3 and U4, which are 8K byte devices.

Memory address decoding for the RAM is accomplished by U39 and U32. They are enabled by the Memory Enable signal (MEMEN) from the microprocessor and a valid high order address. U39 and U32 output the signals RAM2- and RAM1-, which select U5 and U6, and the signal RAM0-, which selects U2. PROM0- and PROM1- are also output by U39 and U32. They provide the Chip Enable signal for EPROMs U3 and U4. The memory map in Figure 009-2 shows how the 9995 memory space is divided between RAM and EPROM.

The CRU address space used by the port UARTs (U116, U216), bus Interface UART (U7), and general serial I/O is decoded by U18 and U19. The decoders are enabled

during a valid CRU cycle. A valid CRU cycle occurs when U20 detects D7-D5 low, a MEMEN cycle is not occurring, and the appropriate address is present. IA8 separates the UARTs from general I/O devices, as shown in the memory map in Table 009-3.

009-6. Ports

Both RS-232-C ports include a UART (U116, U216), drivers and receivers for RS-232-C, RS-422, and 20 mA current loop. In addition, each has a pair of active current and voltage sources and sinks. To ensure compatibility with standard RS-232-C equipment and cables, SW 104 and SW204 allow the connector pins used for the 20 mA current loop and RS-422 interfaces to be disconnected. The data output from the UART is transmitted from all three interfaces. However, the UART can receive from only one at a time as selected by JPR117 and JPR217.

NOTE

The following descriptions refer to the U numbers on the even port. U numbers for the odd port are identical, except for 3-digit numbers. The correct U numbers for the odd port are arrived at by adding 100 to the numbers on the even port. For example, U117 on the even port becomes U217 on the odd port.

009-7. RS-232-C INTERFACE

The outgoing signals for Data Communications Equipment (DCE) from Control Latch (U117) and UART (U116) are converted to RS-232-C levels by gates U126 and U127. Incoming DCE signals are buffered to TTL

levels by U122 and U123 and are routed to the UART (U116) and synchronizing latch U21. See Table 009-11 for an explanation of the DCE signals' pin number, circuit name and function.

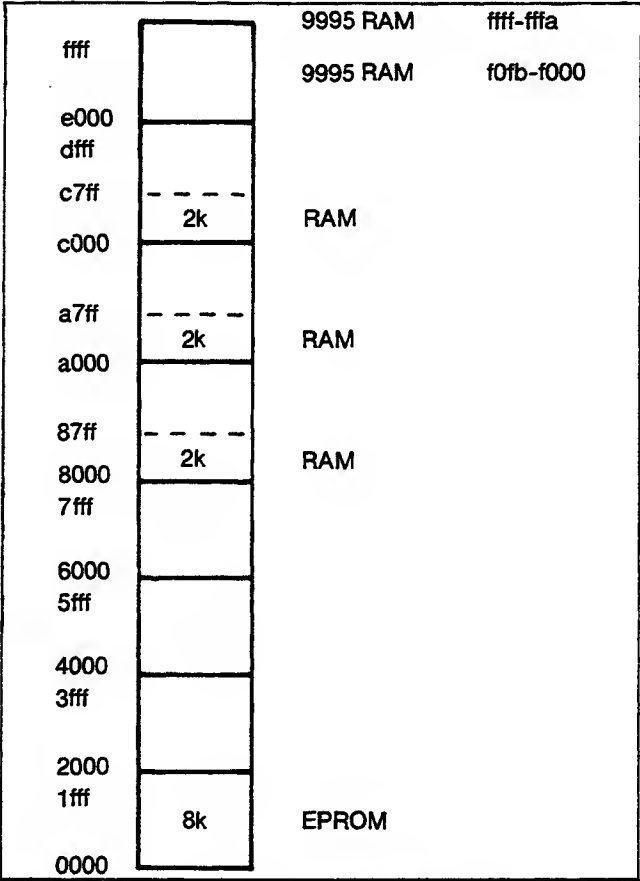


Figure 009-2. Memory Map

Table 009-3. CRU MAP

BASE ADDRESS	DEVICE(S)	FUNCTION
1C0	Reserved	Bus Interface UART
180	U7	Odd Port UART
140	U216	Even Port UART
100	U116	
The following appear twice from fe-00		
70	U220 SW202	Not Used
60	U219 SW201	Power-up Configuration
50	U218 SW3	Power-up Configuration & Synchronized Inputs
40	U217	Handshake Latch
30	U120 SW102	Not Used
20	U119 SW101	Power-up Configuration
10	U118 SW3	Power-up Configuration & Synchronized Inputs
00	U117	Handshake Latch

009-8. RS-422 INTERFACE

The RS-422 drivers (U25) are paralleled to provide extra drive capability and redundancy. The diodes and resistors network clamp external transient voltage faults. A similar network is used with the RS-422 receiver (U24). U24 creates the TTL level required by the UART. Switch 1 and 2 of Signal Enable Switch (SW104) must be closed to enable the RS-422 interface to work.

009-9. 20 MILLIAMP CURRENT LOOP INTERFACE

The current loop transmitter consists of U31, U129, and Q101. It is optically isolated from the external device by U129. The 20 mA receiver is optically isolated by U128. U123 creates the TTL level required by the UART (U116). Switches 3 and 4 of Signal Enable Switch (SW104) must be closed for the 20 mA current loop interface to work. Depending on the external device, the interface may be used passively or actively with the current source/sink described in paragraph 009-10.

009-10. SOURCES/SINKS

Each interface has a pair of 20 mA current and voltage sources controlled by JPR102 and JPR103 and a pair of -12/current sinks controlled by Signal Enable Switch (SW104). A typical active current interface would be wired from current source to transmitter Tx+, from transmitter Tx- to external receiver Rx+, from external receiver Rx- to interface current sink. The voltages are provided for signal biasing needs.

009-11. Board Addressing

The following paragraphs provide factory configurations, power-on configuration, protocols and reconfiguration information for the RS-232-C, RS-422 and 20 mA Current Loop interfaces.

009-12. FACTORY CONFIGURATION

The 17XXA-009 option is configured at the factory as follows:

Electrical Interface	RS-232-C
Data Rate	4800 Baud
Data Bits	7
Parity	none
Stop Bits	2
Board Address	0 (SP0: and SP1:)
Switch Settings	SW101, SW102 (Port Characteristics):
	1 2 3 4 5 6 7 8
	on off on on on off off on
	SW1 (Board/Port Address):
	all off

SW3 (Flow Control: XON/XOFF): all off
SW104, SW204 (Signal Enable Switches): all off

Jumper Settings

JPR116 and JPR216: left position
JPR117 and JPR217: right position
JPR102 and JPR202: center position
JPR103 and JPR203: center position
JPR1, 2,3,4,5,6,29, and 35 are not user-configurable.

Figure 009-3 shows the factory configuration and location of all jumpers and switches.

The signals for RS-232-C, RS-422 and 20 mA Current Loop interfaces are available on both of the DSI port connectors. Refer to paragraphs 009-18 or 009-19 to configure the DSI for RS-422 or 20 mA current loop operation. Different cables are required, depending on the standard to be used. Data Communications Equipment (DCE) requires an RS-232-C cable and Data Terminal Equipment (DTE) requires a null modem cable. Refer to Table 009-15 for connections to external devices.

009-13. POWER-ON CONFIGURATION

When the Dual Serial Interface is powered on, the configuration switches are read, the RS-422 drivers are enabled and the DSI waits for input or output. The Port Characteristics and Flow Control switches are read only at power-up. The initial states of the control lines are shown in Table 009-12.

009-14. PROTOCOLS

XON and XOFF are two ASCII codes used to control data transfer between devices. If the input buffer of the device receiving data is full or nearly full, XOFF is sent to the transmitting device to request that transmission be stopped. When the receiver can accept more data, the XON code is sent to resume the transmission. The SET Utility program can be used to enable or disable this protocol. SET Utility refers to the protocol as Stall Input and Stall Output.

Secondary Request to Send (SRTS) is a handshake line that is used for flow control with external devices that cannot respond to XON/XOFF codes. The polarity of SRTS is set by the Flow Control configuration switch (SW3).

OPTION 17XXA-009
DUAL SERIAL INTERFACE

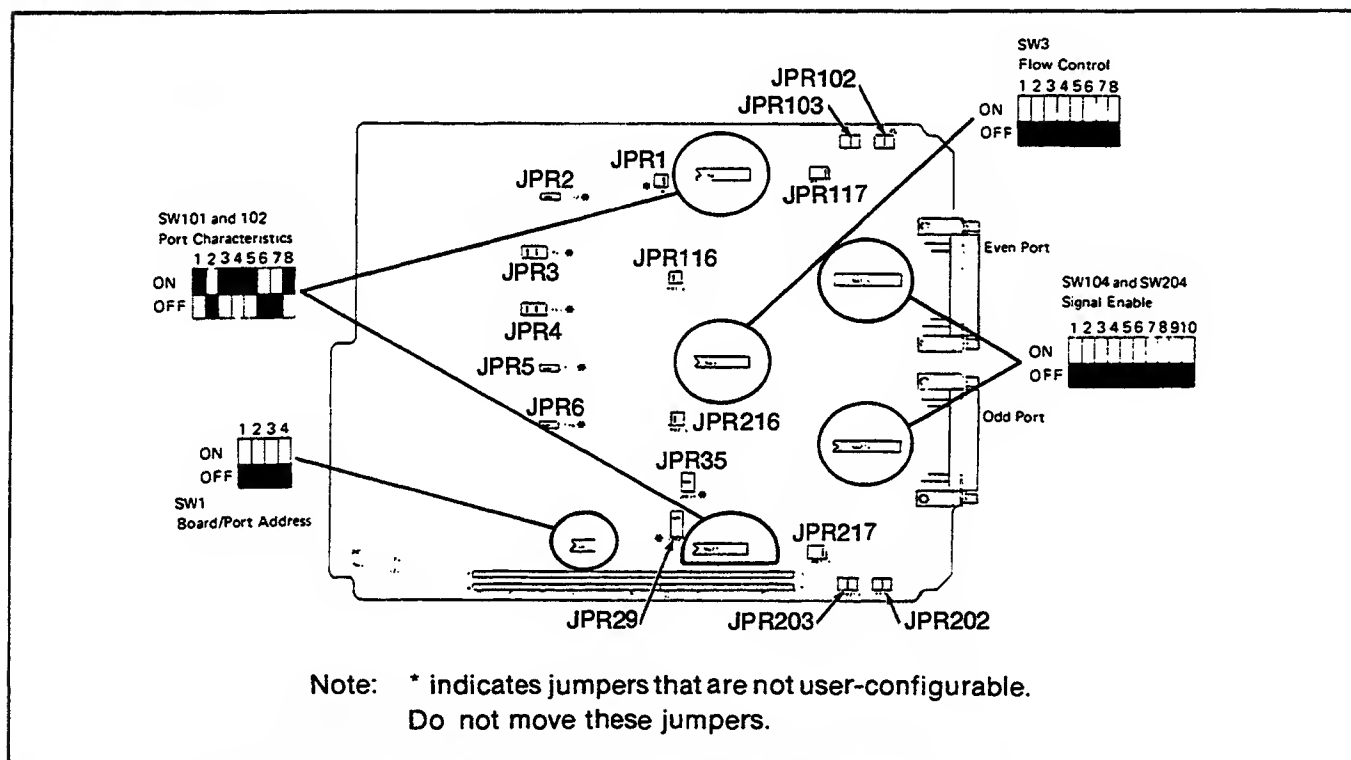


Figure 009-3. Jumper and Switch Location

009-15. RECONFIGURATION

The electrical interfaces and power-up configuration can be changed using the switches and jumpers described in Tables 009-4 through 009-10. Port characteristics can also be changed using the SET Utility program.

009-16. Electrical Interfaces

The following paragraphs discuss each interface and typical setups.

009-17. RS-232-C INTERFACE

Maximums

Distance 50ft.

Data Rate 19200 Baud

Typical applications

Data Communications Equipment (DCE)

Modems (use RS-232-C cable)

Data Terminal Equipment (DTE)

1780A

VT100

Printers (use Null Modem cable)

RS-232-C Port Connections

See Table 009-11

Jumper and Switch Configuration

Refer to factory configuration information.

Table 009-4. Board/Port Addresses (SW1)

BOARD	PORT	SWITCH			
		1	2	3	4
1	1, 0	0	0	0	0
2	3, 2	0	0	0	1
3	5, 4	0	0	1	0
4	7, 6	0	0	1	1
5	9, 8	0	1	0	0

Note:

ON = 1 = closed = enabled

OFF = 0 = open = disabled

J1 = EVEN Port

J2 = ODD Port

The Clear To Send jumpers (JPR116 and 216) allow the CTS input to the UART (U116 or U216) to be either the Clear to Send (CB) circuit or the logical AND of CB and Secondary Received Line Signal Detector (SCF). This feature is useful for external devices that use the SCF circuit as a busy indicator.

Clear To Send (Pin 5 on the port connector) controls the transmission from the port. When it is ON, the corresponding UART is permitted to transmit. When it is OFF, the UART stops transmitting, beginning at the next character boundary. This behavior is a function of the UART hardware and cannot be disabled. If not used by the receiving device, leave Pin 6 unterminated.

Table 009-5. Port Characteristics (SW101 and SW201)

SWITCH	1234	5678
	1111	19200 Baud
	1110	19200
	1101	9600
	1100	7200
	1011	4800
	1010	3600
	1001	2400
	1000	2000
	0111	1800
	0110	1200
	0101	600
	0100	300
	0011	150
	0010	134
	0001	110
	0000	75

Table 009-6. Flow Control (SW3)

SWITCH	1	2	3	4	5	6	7	8
	1							Even Port
	0							enable
		1						disable
		0						active high
			x	x				active low
								not used
					1			Odd Port
					0			enable
						1		disable
						0		active high
							x	active low
							x	not used

Table 009-7. Port Connector Signal Enable Switches

Port Connector Signal Enable Switches (SW104 and SW204)		
SWITCH	CONFIGURATION	SIGNAL
1	RS-422	Rx+
2		Rx-
3	20 mA	Rx+
4		Rx-
5	RS-422	I1-/-12v
6		I2-/-12v
7		Tx+
8		Tx-
9	20 mA	Tx+
10		Tx-

Table 009-8. JPR116 and JPR216 Settings

Clear To Send (CTS) Input to UART		
Left	CTS	
Right	CTS	SRLSD

Table 009-9. JPR117 and JPR217 Settings

UART Receive Input Jumpers	
Left	20 mA current loop
Middle	RS-422
Right	RS-232-C

Table 009-10. JPR102, JPR103, JPR202, JPR203 Settings

Voltage/Current Sources	
Left	20 mA
Middle	OFF
Right	+12V

Table 009-11. RS-232-C Port Connections

To DCE		
Pin	Circuit Function	
1	AA	Shield
7	AB	Signal Common
2	BB	Transmitted Data
4	CA	Request to Send
20	CD	Data Terminal Ready
19	SCA	Secondary Request to Send
11	UND	RS-232-B
From DCE		
Pin	Circuit Function	
3	BA	Received Data
5	CB	Clear to Send
6	CC	Data Set Ready
22	CE	Ring Indicator
12	SCF	Secondary Received Line Signal Detector
8	CF	Received Line Signal Detector

OPTION 17XXA-009
DUAL SERIAL INTERFACE

Table 009-12. Control Line Power-on States

SIGNAL	PIN	STATE
BB	2	MARK
CA	4	ON
SCA	11, 19	OFF
CD	20	ON

JPR103 and JPR203: center position
JPR1, 2,3,4,5,6,29, and 35 are not user-configurable.

009-18. RS-422 INTERFACE

Signal Enable Switches 104 and 204 are configured as follows:

1 2 3 4 5 6 7 8 9 10
on on off off off off on on off off

Maximums

Distance 4000 feet
Data Rate 19200 Baud

Typical Applications

2400B
1780A/AU

Protection Networks

The RS-422 circuitry incorporates protection networks on the drivers and receivers to reduce susceptibility to high voltage transients and faults.

RS-422 Port Connections

See Table 009-13

Switch Settings

SW104, SW204 (Signal Enable Switches)

1 2 3 4 5 6 7 8 9 10
on on off off off off on on off off

SW1 (Board/Port Address): user configurable
SW3 (Flow Control: XON/XOFF): user configurable
SW101, SW201: user configurable

Jumper Settings

JPR116 and JPR216: user configurable
JPR117 and JPR217: center position
JPR102 and JPR202: center position

Table 009-13. RS-422 Port Connections

To External Device		
PIN	SWITCH	SIGNAL
9	7	Tx+
10	8	Tx-
7		Signal Ground
From External Device		
PIN	SWITCH	SIGNAL
14	1	Rx+
15	2	Rx-

009-19. 20 MILLIAMP LOOP INTERFACE

Signal Enable Switches 104 and 204 are configured as follows:

1 2 3 4 5 6 7 8 9 10
off off on on on on off off on on

Maximums

Distance 1000 feet
Data Rate 4800 Baud
Voltage 30 Vdc

Typical Application
Teletype (TTY)

20 mA Current Loop Port Connections

See Table 009-14

Switch Settings

SW104, SW204 (Signal Enable Switches)

1 2 3 4 5 6 7 8 9 10
off off on on on off off off on on

SW101, SW201: user configurable

Jumper Settings	<p>SW1 (Board/Port Address): user configurable</p> <p>SW3 (Flow Control: XON/XOFF): user configurable</p> <p>JPR116 and JPR216: user configurable</p> <p>JPR117 and JPR217: left position</p> <p>JPR102 and JPR202: left position</p> <p>JPR103 and JPR203: center position</p> <p>JPR1, 2,3,4,5,6,29, and 35 are not user-configurable.</p>
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009-20. TROUBLESHOOTING THE 17XXA-009 OPTION

System Diagnostic software is provided with the 17XXA to aid in identifying faulty modules. The diagnostic program SPTEST performs a Port-To-Port Loop test between the two DSI ports on up to three -009 Options installed in the 17XXA. SPTEST may be executed with the DSI configured for any of the three electrical interfaces. A null-modem cable (Y1705 or equivalent) can be used to test the RS-232-C interface, but a DSI Test Cable (P/N 754648) is required to test the RS-422 or 20 mA current loop interfaces. Figure 009-4 shows the DSI test cable connections. For more information on the System Diagnostic tests, see Section 3.

If the 17XXA-009 passes the System Diagnostic, but data is not being exchanged when it is connected to an external device, do the following:

- Use the SET Utility Program to check the port characteristics (Data Rate, Parity, Number of Data Bits, Number of Stop Bits, Baud Rate, End of Line and End of File Terminators, Stall Input/Output Enable/Disable, Flow Control, and Time Out Value) on both the 1722A and the external device.
- Verify that the correct cable is being used for the current external device configuration. See Table 009-15 to match the proper cable to the device configuration.

If an error is encountered by the System Diagnostic during the execution of a test, check to ensure that the board is fully seated in the card cage. Also check to see that the cables and switch and jumper positions are correct for the application before re-running the original test. See paragraphs 009-17 through 009-19 for information on jumper and switch configurations.

Because of the complexity of the -009 Option, it is very difficult to troubleshoot to the component level. Therefore, it is recommended that the module be exchanged and sent back to the factory for repair if at all possible. If component-level troubleshooting is necessary, you will need, at a minimum, the following equipment: a multi-trace oscilloscope, a digital multimeter, a Circuit Board Extender, a DSI Test Cable, a logic probe and replacement components. Since most components are soldered into the circuit board, it will be necessary to unsolder them for replacement.

CAUTION

Extreme care should be used when removing and replacing components to avoid irreparable damage to the printed circuit boards.

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

Using the diagnostic program SPTEST, it is possible to isolate the problem to one of two areas: data circuit failures, or kernel and ARGUS bus interface failures. Data circuit failures are indicated if the -009 Option passes SPTEST when the board is configured for one type of interface (RS-232, RS-422, or 20ma current loop) but not another. Kernel or ARGUS bus interface failures will usually result in the message "Option missing, faulty, or improperly configured".

For data circuit failures, it is possible to run SPTEST in loop mode while checking for proper signal levels and tracing faulty signals back to their source. With the help of the schematic it is possible to quickly narrow down the failure to a few components.

For kernel or ARGUS bus interface problems, however, it is likely that the SBC cannot communicate with the CPU on the -009 Option. There is no easy way to exercise the -009 while looking for failures. It is possible to check for activity in the kernel hardware to see that the 9995 microprocessor (U1) is putting out valid addresses and data, and that the program EPROM (U3) and workspace RAM (U2) are being selected. If the kernel appears to be functioning it is possible that one of the UARTs (U7 and U8) or associated buffers in the communication path from the SBC to the -009 Option is faulty. Beyond that there are too many possibilities to effectively troubleshoot in the field. Figure 009-5 summarizes the approach to be used in diagnosing problems with the -009 Option.

Table 009-14. 20mA Current Loop Port Connections

To External Device			From External Device		
PIN	SWITCH	SIGNAL	PIN	SWITCH	SIGNAL
12	9	Tx+	24	3	Rx+
23	10	Tx-	25	4	Rx-
18	5	I1-/+12v	17	JPRx02	I1+/-+12v
16	6	I2-/+12v	13	JPRx03	I2+/-+12v

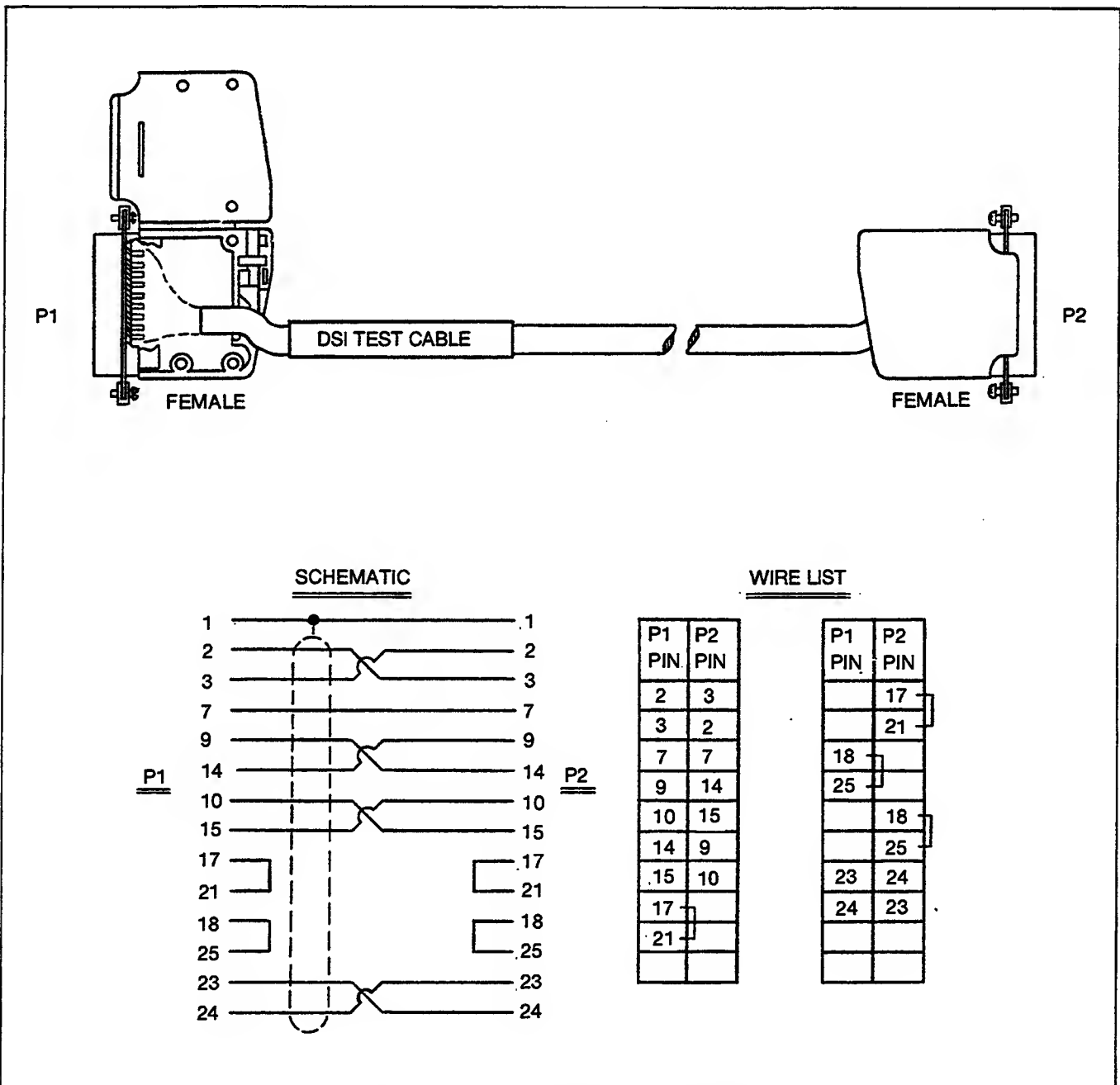


Figure 009-4. DSI Test Cable Connections

Table 009-15. Cable Verification

External Device Configuration	Cable
Data Communication Equipment (modems, etc.)	RS-232 (straight through) (Fluke model Y1707 or Y1708)
Data Terminal Equipment (terminals, computers, etc.)	Null Modem (signal pairs crossed) (Fluke model Y1702, Y1703 or Y1705)
Other (Printer, plotter, etc.)	Null Modem (signal pairs crossed) (Fluke model Y1702, Y1703 or Y1705) or custom cable

OPTION 17XXA-009
DUAL SERIAL INTERFACE

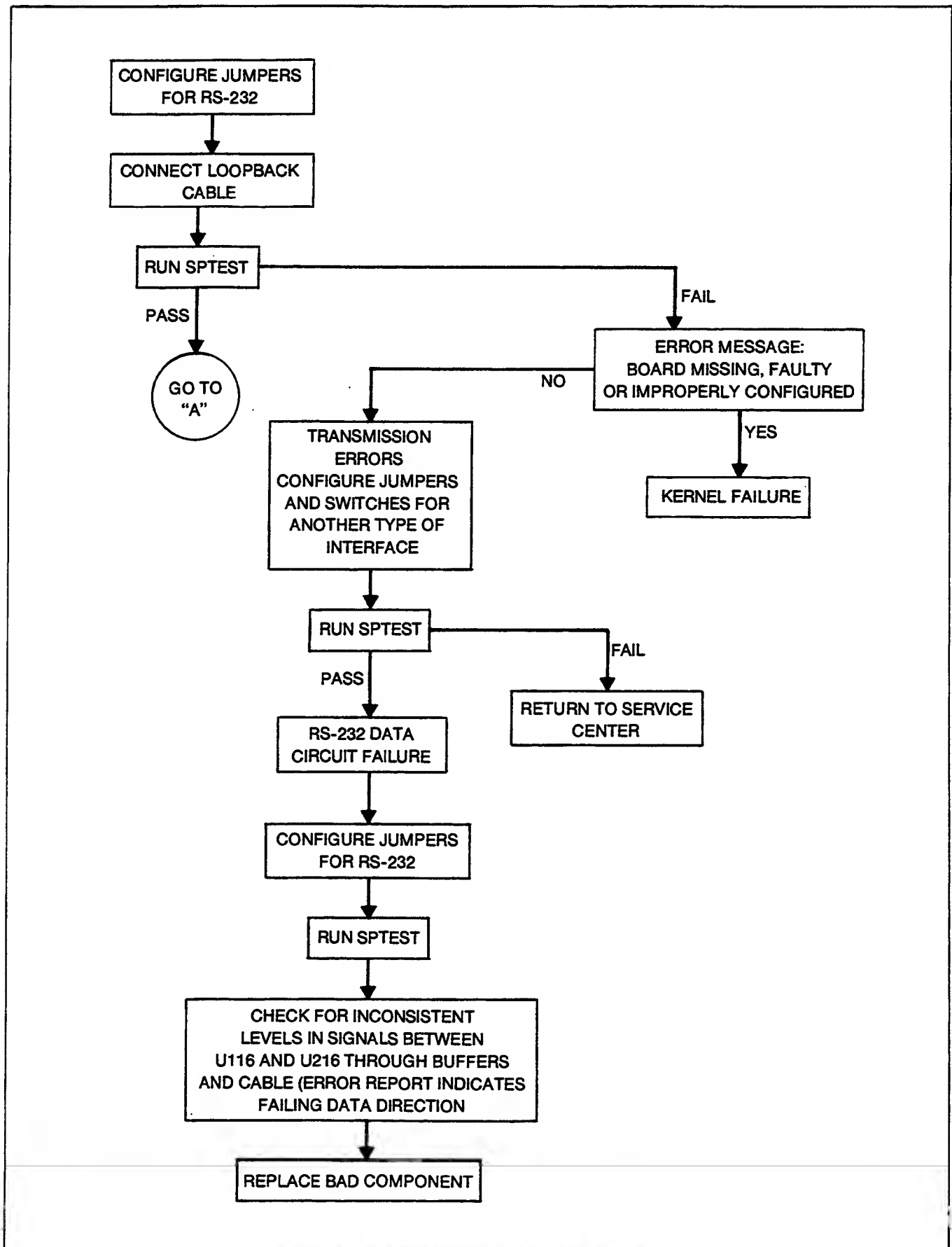


Figure 009-5. Troubleshooting the 009 Option

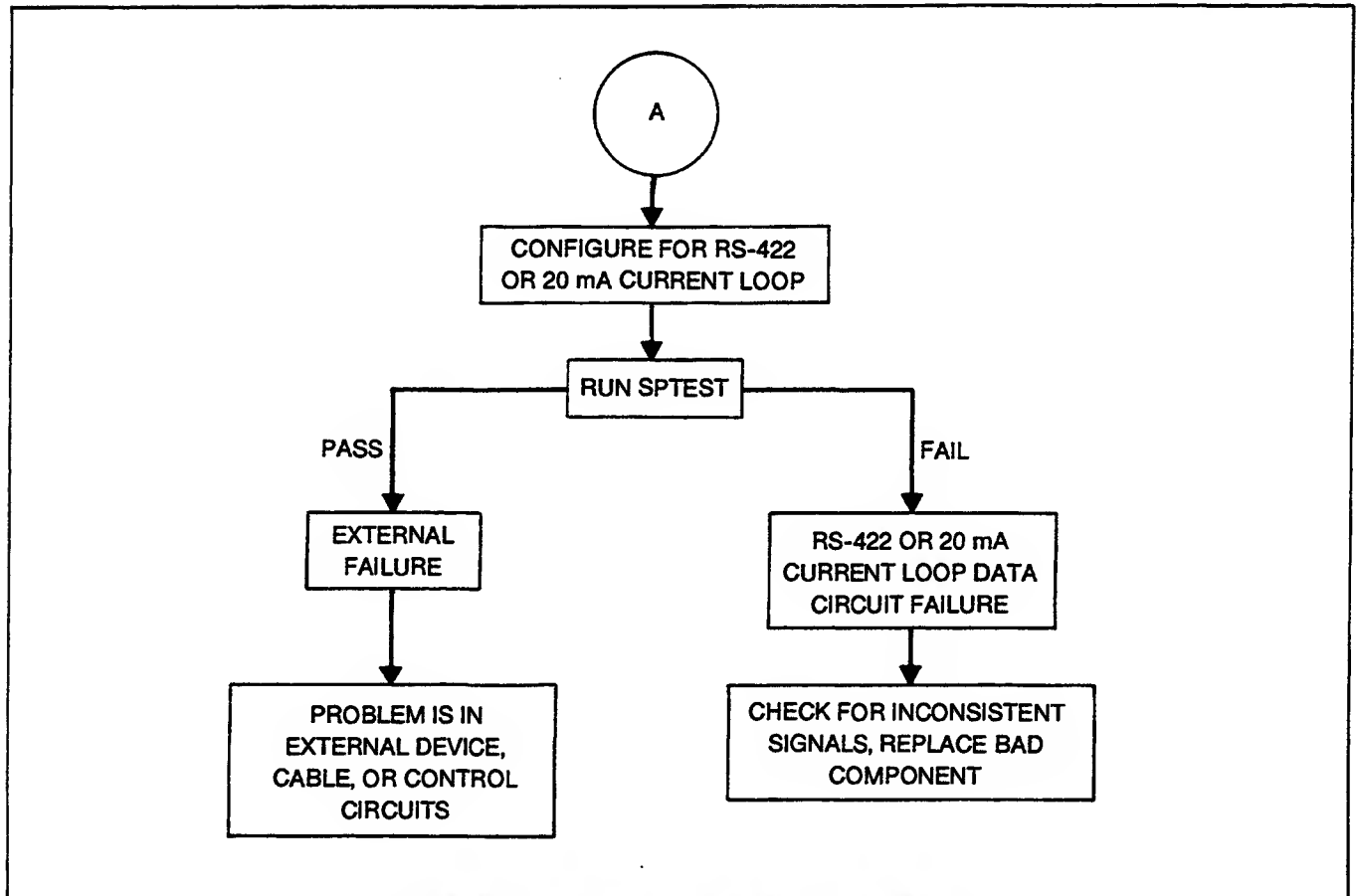


Figure 009-5. Troubleshooting the 009 Option (cont)

Option 1752A-010

Analog Measurement Processor

010-1. INTRODUCTION

The Analog Measurement Processor is a printed circuit assembly that mounts in the 1752A chassis and measures voltages and currents. The Analog Measurement Processor digitizes the readings for manipulation by the 1752A. At the heart of the processor are a successive approximation Analog-to-Digital (A/D) converter and a 32-channel input scanner. The processor is controlled by BASIC subroutines that are provided on the 1752A System Disk.

Two external connectors on the Analog Measurement Processor provide 32 individually-addressable input channels. The processor features two voltage ranges, two current ranges, single-ended and differential input modes, selectable software filtering and synchronous and asynchronous scanning modes.

010-2. SPECIFICATIONS

See Table 010-1 for Analog Measurement Processor specifications.

010-3. THEORY OF OPERATION

010-4. Introduction

This section presents a functional and circuit description of the 1752A-010 Analog Measurement Processor. These descriptions are supported by Figure 010-1 and the schematic diagrams in Section 5.

010-5. Functional Description

Figure 010-1 is a functional block diagram of the 1752A Analog Measurement Processor. The processor uses the successive approximation technique to obtain conversion rates of up to 1,000 readings per second. On-board CMOS multiplexers allow voltage measurements on 16 differential or 32 single-ended channels. Current shunts

are provided for a 65 mA current range on each differential channel. There are two voltage ranges, 10V full scale and 1V full scale.

An on-board microprocessor controls measurement timing and corrects for errors due to gain and offset drifts. The microprocessor also provides programmable digital filtering for each measurement channel. Range, filtering, and measurement results for each channel are passed between the controller and the A/D converter via a dual-port memory. The bus address range of this shared memory is selected by switches on the A/D converter, allowing up to four Analog Measurement Processors to run simultaneously in one system.

010-6. Circuit Description

The following paragraphs provide a detailed circuit description of each functional block in Figure 010-1.

010-7. BUS INTERFACE LOGIC CIRCUITRY

The 1752A Single Board Computer (SBC) exchanges commands and channel readings with the Analog Measurement Processor through 512 bytes of Dual Port RAM using memory mapped I/O operations. Address Select switches S1, segment 3 and S1, segment 4 determine what range of bus addresses the Analog Measurement Processor will respond to (and therefore its board address).

Refer to Figures 010-2 and 010-3 for a block diagram and a timing diagram of the Bus Interface Logic. The address decode circuitry monitors the Address lines AD10 through AD17 and the Address Valid (ADVAL-) signal from the SBC. When the bus address sent from the SBC falls within the range of addresses selected by switch S1, and when ADVAL- is asserted low, the SELECT signal is asserted high after the next rising edge of the system clock (SYNC).

OPTION 1752A-010**ANALOG MEASUREMENT PROCESSOR****Table 010-1. Analog Measurement Processor Specifications**

Number of Channels	32 single-ended or 16 differential (single-ended and differential channels may be mixed).
System Capacity	4 Analog Measurement processors, 128 single-ended channels.
Synchronization Modes	Internally Synchronized: 50, 60, or 400 Hz Externally Synchronized: 45 to 65 Hz or 360 to 520 Hz Asynchronous.
Ranges (full scale, each channel)	$\pm 10.158\text{V}$ $\pm 1.0158\text{V}$ $\pm 67.718\text{ mA}$ 4 to 20 mA, displayed as 0 to 100% of scale
Reading Rate	Synchronized Modes: 400 readings/sec @ 50 Hz 480 readings/sec @ 60 Hz 400 readings/sec @ 400 Hz Asynchronous Mode: 1000 readings/sec
Accuracy (90 days, 10° to 40°C)	10V Range: $\pm(0.02\%$ of reading + 1.24 mV) 1V Range: $\pm(0.02\%$ of reading + 248 μV) 65 mA Range: $\pm(0.05\%$ of reading + 16.533 μA)
Resolution	10V Range: 310 μV 1V Range: 31 μV 65 mA Range: 2.0667 μA (15 Ω , 0.04%, 20 ppm TC sense resistor)
Filtering	Software filter, 1 to 128 readings, software selectable in powers of two.
Common Mode Voltage (including measurement value)	10V Range: $\pm 10.5\text{V}$ 1V Range: $\pm 6.5\text{V}$
Common Mode Rejection	dc: 77 dB @ 10°C-40°C 50/60 Hz: 60 dB @ 10°C-40°C
Normal Mode Rejection	Internally Synchronized Mode: 20 dB (50/60 Hz ± 0.3 Hz) Externally Synchronized Mode: 50 dB (45 Hz to 65 Hz) 45 dB (360 Hz to 520 Hz) Asynchronous Mode: 0 dB
Input Protection	50V rms without side effects Fuse-resistor protected to 240V rms (400V peak)
Automatic Self-Calibration	Performed approximately every 17 seconds. Requires 10 msec. May be disabled by user software.

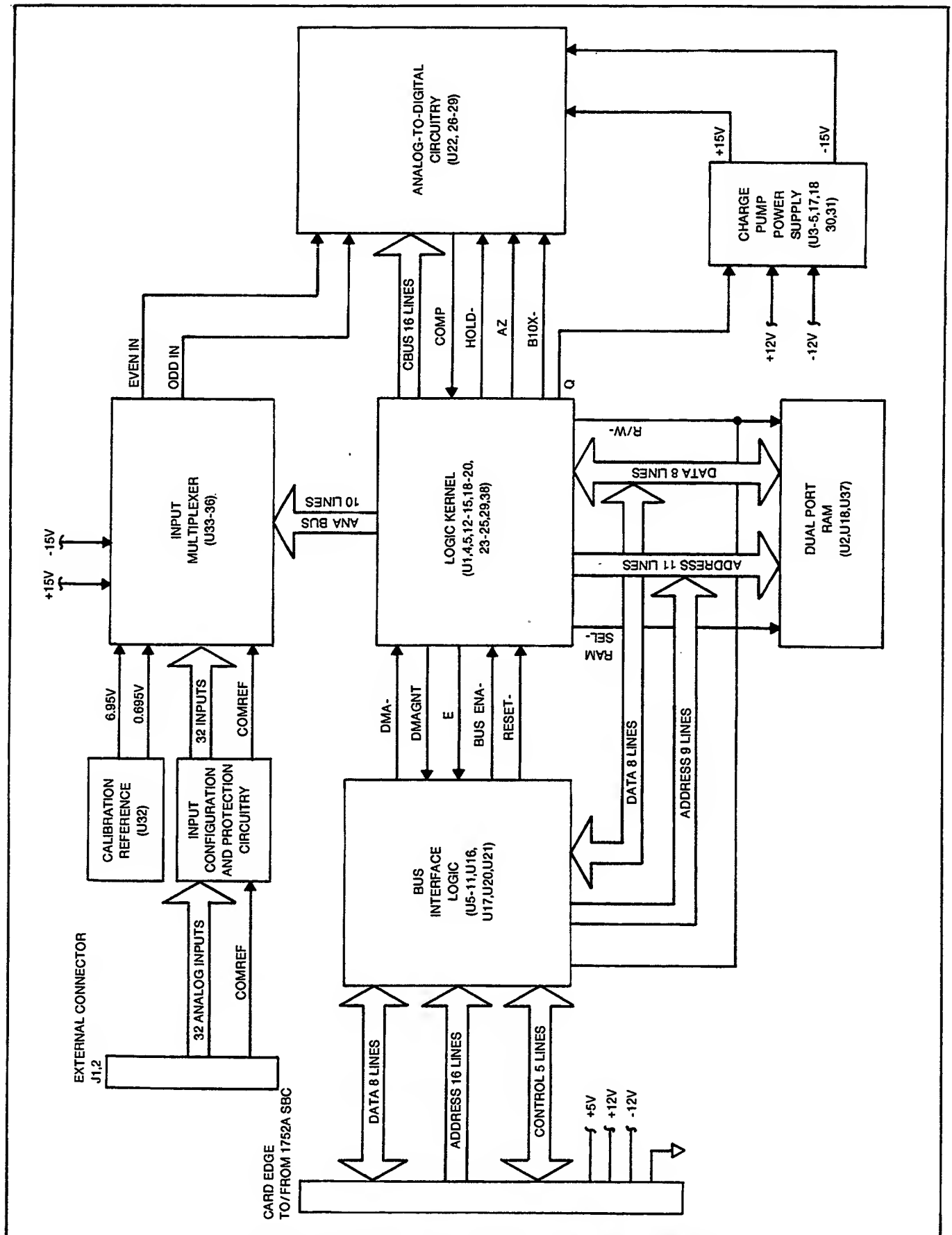


Figure 010-1. Analog Measurement Processor Block Diagram

OPTION 1752A-010
ANALOG MEASUREMENT PROCESSOR

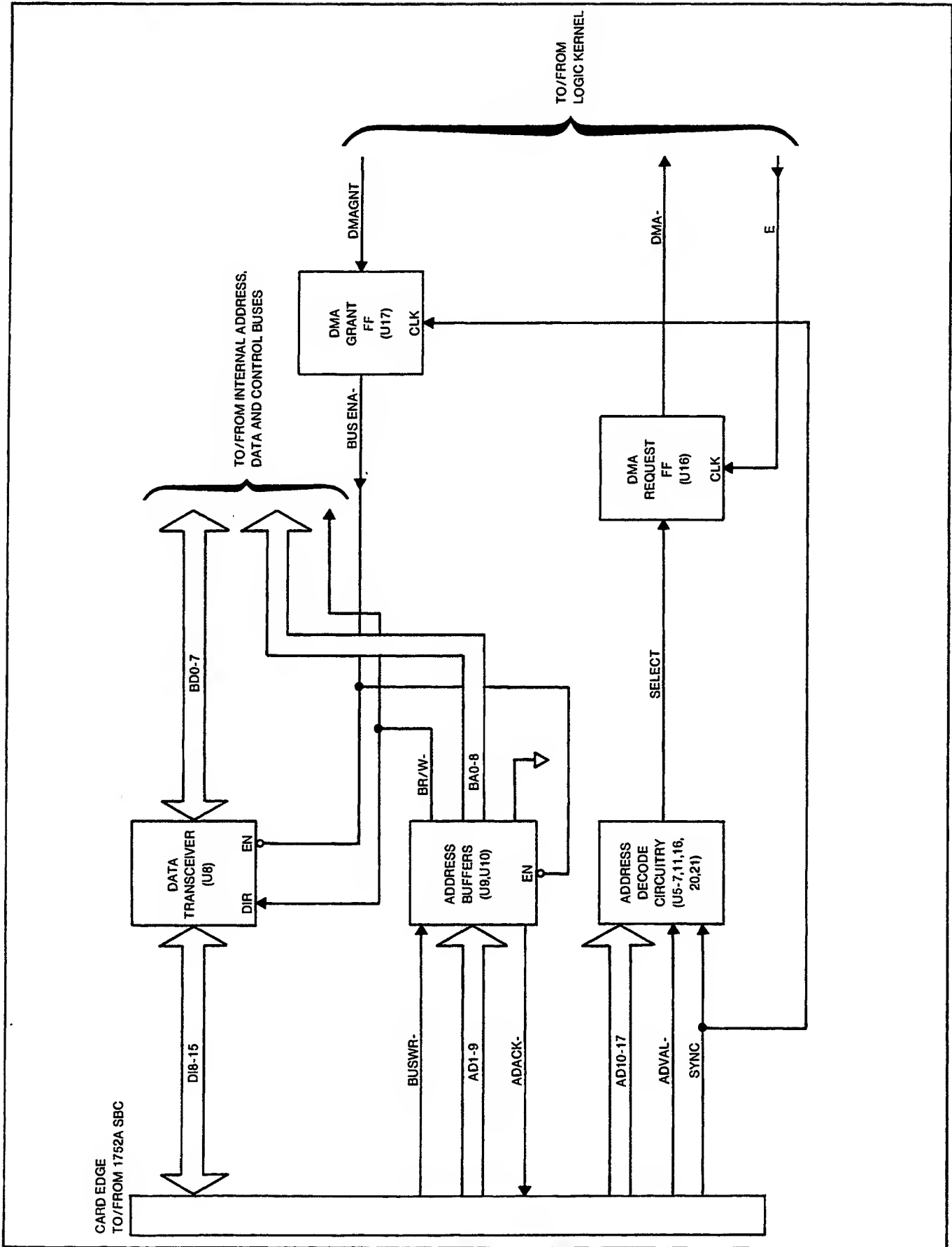


Figure 010-2. Bus Interface Logic Block Diagram

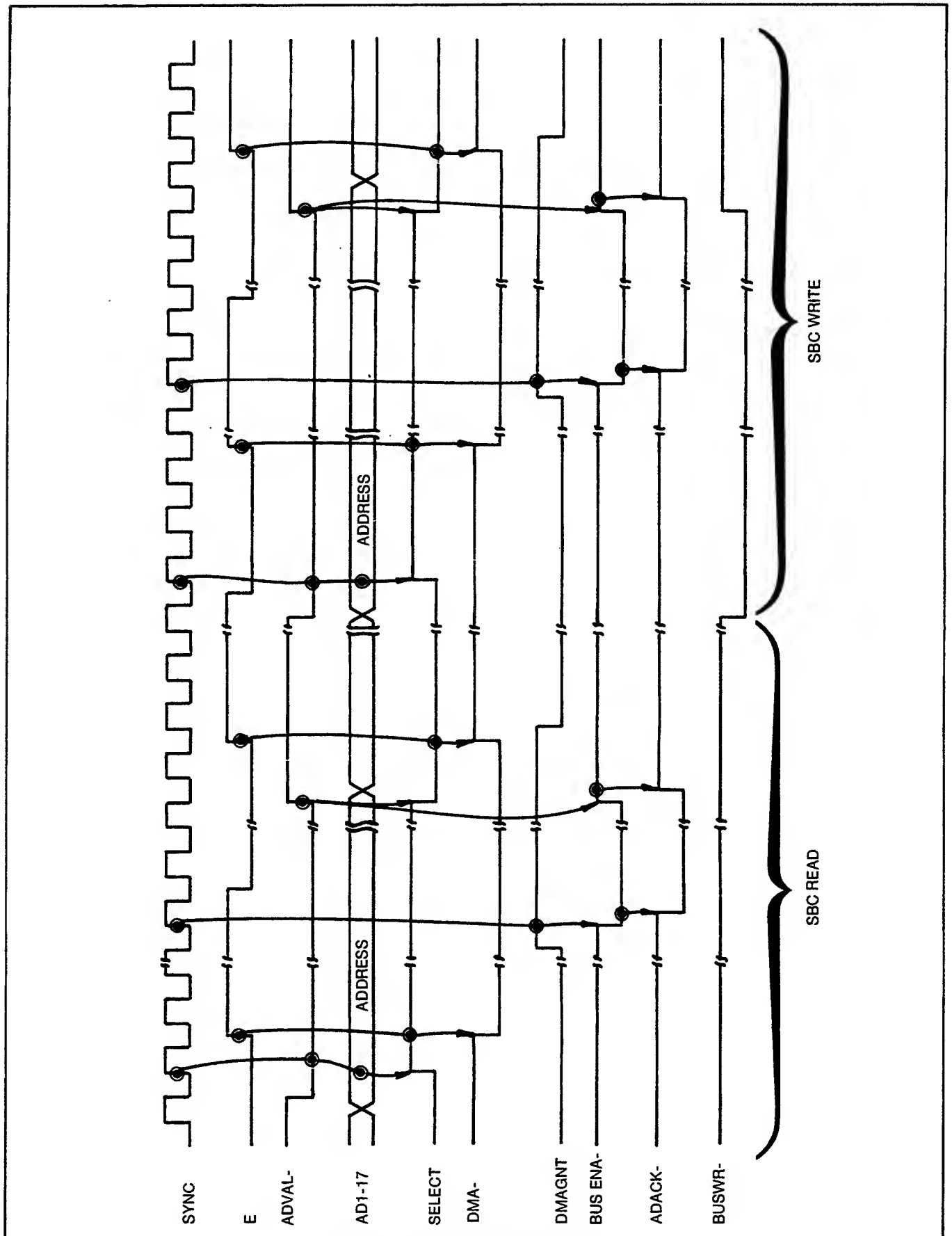


Figure 010-3. Bus Interface Timing

After the next rising edge of the E clock from the microprocessor in the Analog Measurement Processor, the Direct Memory Access (DMA-) signal is asserted low. The low DMA state signals the microprocessor that the SBC requests a Direct Memory Access Cycle.

At the end of the current memory cycle, the microprocessor tri-states its address, data and control buses and enters a DMA Grant state. Gate U20 detects the DMA Grant state and asserts the DMAGNT signal high. After the next rising edge of SYNC, Bus Enable (BUS ENA-) is driven low, enabling the Address and Data buffers. This drives the Address Acknowledge (ADACK-) signal low, allowing the SBC to continue with its read/write operation.

Address buffers (U9 and U10) allow the system address lines AD1 through AD9 to propagate to the Dual Port RAM. This allows the SBC to access the lower 512 bytes of memory. In addition, Address buffer U9 buffers the Bus Write (BUSWR-) signal, which sets up the direction of data flow through the Data Transceiver (U8) and provides the R/W- signal to the dual port RAM. Data is passed to/from the dual port RAM through the Data Transceivers over the system data lines DI8 through DI5.

When the SBC has finished its access to the Analog Measurement Processor, it de-asserts ADVAL- high, causing the Address decode circuitry to de-assert the SELECT signal low. The BUS ENA- signal is also driven high, disconnecting the system bus from the Analog Measurement Processor. After the next rising edge of the E clock from the Analog Measurement Processor's microprocessor, the DMA- signal is de-asserted high. This allows the microprocessor to regain control over its address, data and control buses and continue with normal operation.

010-8. LOGIC KERNEL

The Analog Measurement Processor's logic kernel consists of a 6809 microprocessor (U14), a 2K-by-8 Ram (U2), a 2K-by-8 Electrically Erasable Prom (U1), a Peripheral Interface Adapter (U15), two eight bit latches (U12 and U13), and a Phase-Locked Frequency Multiplier circuit (U24, U25, and U29).

The Peripheral Interface Adapter chip (PIA) acts as an interface between the microprocessor and the Analog-to-Digital and Input Multiplexer circuitry. Control signals are provided by the 20 bits of read/writable I/O in the PIA. One 16-bit timer provides the AZ timing required by the A/D circuitry. In internal synchronization mode, another 16-bit timer provides the HOLD-timing required by the A/D circuitry. The 16-bit timers also provide timing information to the microprocessor via interrupts.

In external synchronization mode, the HOLD-timing for the A/D circuitry is provided by the Phase-Locked Frequency Multiplier circuit. The Line Ref. Input is passed through a comparator (U29) and input to a Digital Phase-Locked Loop (PLL). The VCO output of the PLL is passed through a binary counter (U25), which divides the VCO frequency by 2 or 16 depending on the jumper setting of JPR2. (If jumpered for 50/60 Hz operation, the signal is divided by 16.)

The output of the binary counter is then fed back to the COMP IN input to the PLL. Consequently, when the PLL is locked and the frequencies of the REF IN and COMP IN signals are equal, the VCO output is either 2 or 16 times the frequency of the Line Ref Input signal. The VCO output of the PLL is then multiplexed to the HOLD- line of the A/D circuitry by U23.

010-9. CHARGE PUMP POWER SUPPLIES

Each Analog Measurement Processor contains a charge pump power supply to convert the $\pm 12\text{V}$ system supplies to the $\pm 15\text{V}$ supplies required by the A/D circuitry. Each supply is regulated by a linear regulator to within $\pm 0.6\text{V}$ of its nominal value at a typical load current of 70 mA.

The 2 MHz E clock from the microprocessor in the Analog Measurement Processor is divided by a binary counter (U3) to create a 7.8 kHz drive signal. Flip-flop U17 and external gating (U4, U5, and U18) use this drive signal to create non-overlapping drive signals of opposite polarity for transistor switches Q1 and Q4. Consequently, when Q1 is turned on, Q4 is turned off, and vice versa. They are never on at the same time.

When transistor Q1 is turned off, the gate of FET Q2 is pulled down to -12V, turning Q2 off. At the same time, Q4 is turned on, causing the gate of Q3 to be pulled to approximately 0.3V, turning Q3 on. Consequently, the common connection of C28 and C29 is pulled to a -12V potential. This causes C28 to charge to approximately 11V due to the diode clamp CR3.

When Q1 is subsequently turned on and Q4 turned off, FET Q2 is turned on and FET Q3 is turned off, pulling the common connection of C28 and C29 to a ground potential. This 12V swing at the negative end of C28 causes the positive end of C28 to swing 12V. Due to the 11V charge on C28, this voltage swing results in a 23V potential that forward biases diode CR4, allowing C28 to charge output capacitors C30 and C32. After C30 and C32 are charged, CR4 becomes back-biased, preventing any further current flow to C28.

Output capacitors C31 and C33 are charged in a similar manner by C29, diodes CR5 and CR6, and the switching of FETs Q2 and Q3.

The voltage present on the charge pump output capacitors (C30 through C33) varies but is nominally 22V. Linear voltage regulators U30 and U31 reduce the output to provide the positive and negative 15V supplies.

010-10. INPUT CONFIGURATION AND PROTECTION CIRCUITRY

Inputs to the Analog Measurement Processor are user-configurable as voltage or current inputs. The schematic in Section 5 of this manual shows all channels configured as voltage inputs. To configure a current input, the jumpers are positioned to place a 15 ohm shunt across a channel pair. Current is determined by measuring the voltage drop across the shunt.

Inputs to the Analog Measurement Processor are passed through Input Protection circuitry to protect the Analog Measurement Processor from high voltages that may be present. Protection is provided to 50 Vrms without any side effects, with fuse-resistor protection to 240 Vrms. The protection circuit consists of a 10 Kohm fusible resistor and two FETs configured as diodes. One FET is connected to the PLSCLMP line to clamp the input to approximately +13V. The other FET is connected to the NEGCLMP line to clamp the input to approximately -13V. If an input is too positive or negative, a large current is drawn through one of the protection FETs, causing the fusible resistor to blow open.

010-11. INPUT MULTIPLEXER CIRCUITRY

The Input Multiplexer circuitry consists of two 16-input single-ended analog multiplexers and two 4-input differential analog multiplexers. These components multiplex several inputs onto the EVENIN and ODDIN inputs to the A/D circuitry.

Refer to Figure 010-4 for a block diagram of the input multiplexer circuitry. When the Analog Measurement Processor is making a single-ended measurement on an even-numbered channel, the Even Channel Multiplexer (U35) is enabled. Control bits M0 through M3 from the Logic Kernel select one of 16 even-numbered input channels to be multiplexed onto the EVENIN line to the A/D circuitry. At the same time, the Reference Multiplexer (U34) is enabled. Control bits T0 and T1 route the COMREF input to the Analog Measurement Processor onto the ODDIN line to the A/D circuitry. Consequently, the voltage difference between the EVENIN line and the ODDIN line is equal to the voltage present at the even-numbered input referenced to COMREF.

Single-ended measurements on odd-numbered channels are made in a similar manner. The Odd Channel Multiplexer (U36) is enabled, causing one of 16 odd-numbered input channels to be multiplexed onto the ODDIN line. The COMREF input to the Analog

Measurement Processor is multiplexed onto the EVENIN line by the Reference Multiplexer. Thus, the voltage difference between the ODDIN line and the EVENIN line is equal to the voltage present at the odd-numbered input referenced to COMREF.

During differential measurements, both the Even Channel and Odd Channel Multiplexers are enabled and the Reference Multiplexer is disabled. Control bits M0 through M3 select one of 16 channel pairs to be multiplexed onto the EVENIN and ODDIN lines. Consequently, differential measurements can be made only between two consecutive channels.

The Calibration Multiplexer shown in Figure 010-4 is enabled during Analog Measurement Processor self-calibration cycles. It routes the on-board 6.95V and 0.695V references onto the EVENIN and ODDIN lines. For the calibration sequence, refer to paragraph 010-13.

010-12. ANALOG-TO-DIGITAL CIRCUITRY

The Analog-to-Digital (A/D) circuitry is a 16-bit, successive approximation A/D. It consists of a differencing amplifier with switchable gain, auto-zero circuitry, a track/hold amplifier, a digital-to-analog converter, and a comparator.

Refer to the block diagram of the A/D circuitry shown in Figure 010-5. The voltages on the EVENIN lines and the ODDIN lines are fed into a difference amplifier whose gain is switchable from approximately 0.99 to 9.9. If the B10X- signal from the logic kernel is high, FET Q5 is turned off, and the gain of the buffer is 0.99. If B10X- is low, FET Q5 is turned on and the gain of the buffer is 9.9. The higher gain is used when making measurements in the 1V range to increase the resolution of the A/D circuitry.

The output of the differencing amplifier is capacitively coupled to a track/hold amplifier through capacitor C37. This capacitor allows auto-zeroing of the difference amplifier to cancel the effects of voltage offsets present in the amplifier. To auto-zero the input amplifier, EVENIN and ODDIN are connected to analog ground through the input multiplexer circuitry. In addition, one end of the auto-zero capacitor is connected the analog ground through FET Q6. At the end of the auto-zero period, capacitor C37 is charged to a voltage equal to the offset voltage present at the output of the difference amplifier. When the input to be measured is subsequently switched into the A/D circuitry, FET Q6 is turned off, releasing the auto-zero capacitor from analog ground. The input to the track/hold amplifier is equal to the output of the difference amplifier minus the charge on the auto-zero capacitor (i.e., the amplifier offset).

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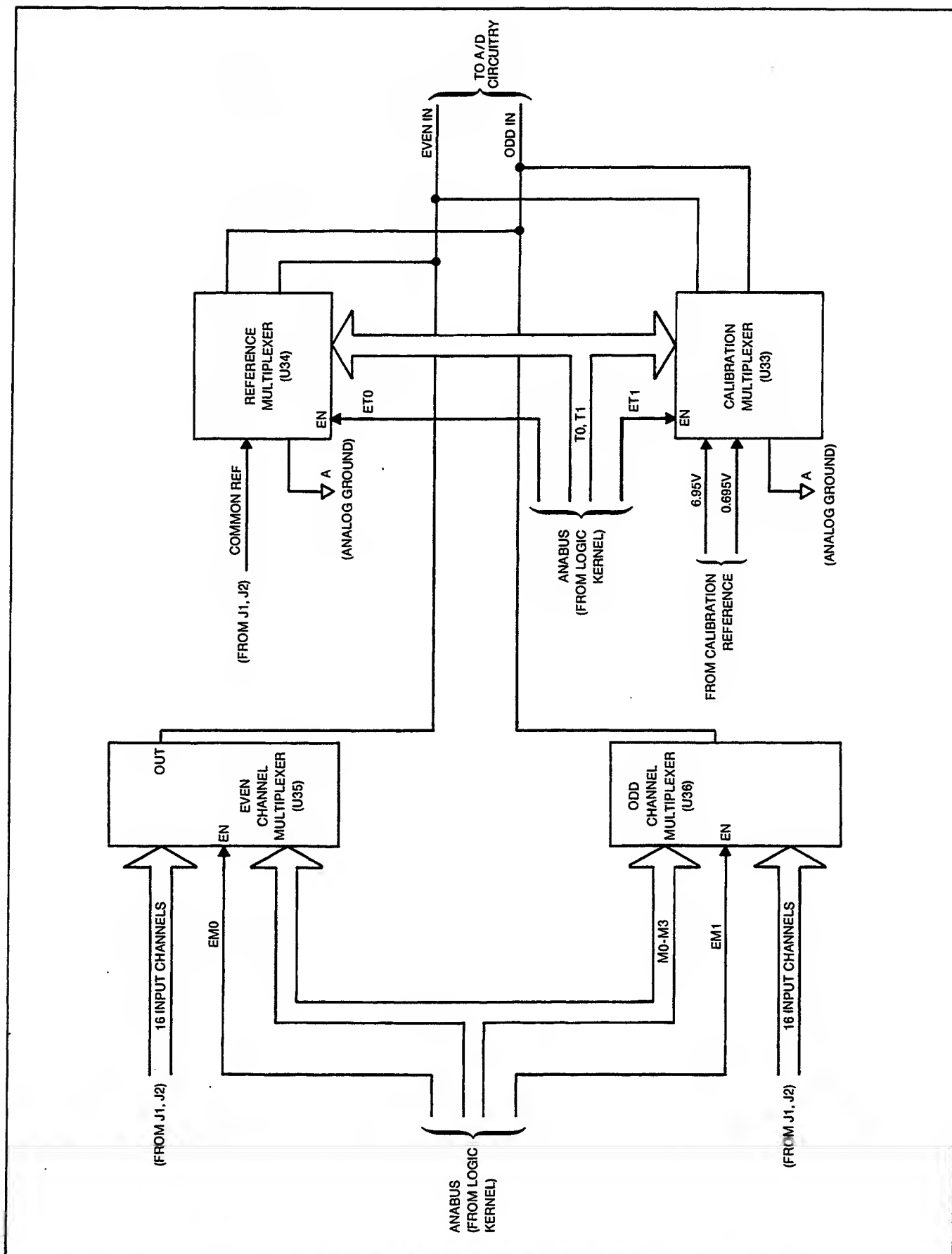


Figure 010-4. Input Multiplexor Circuitry

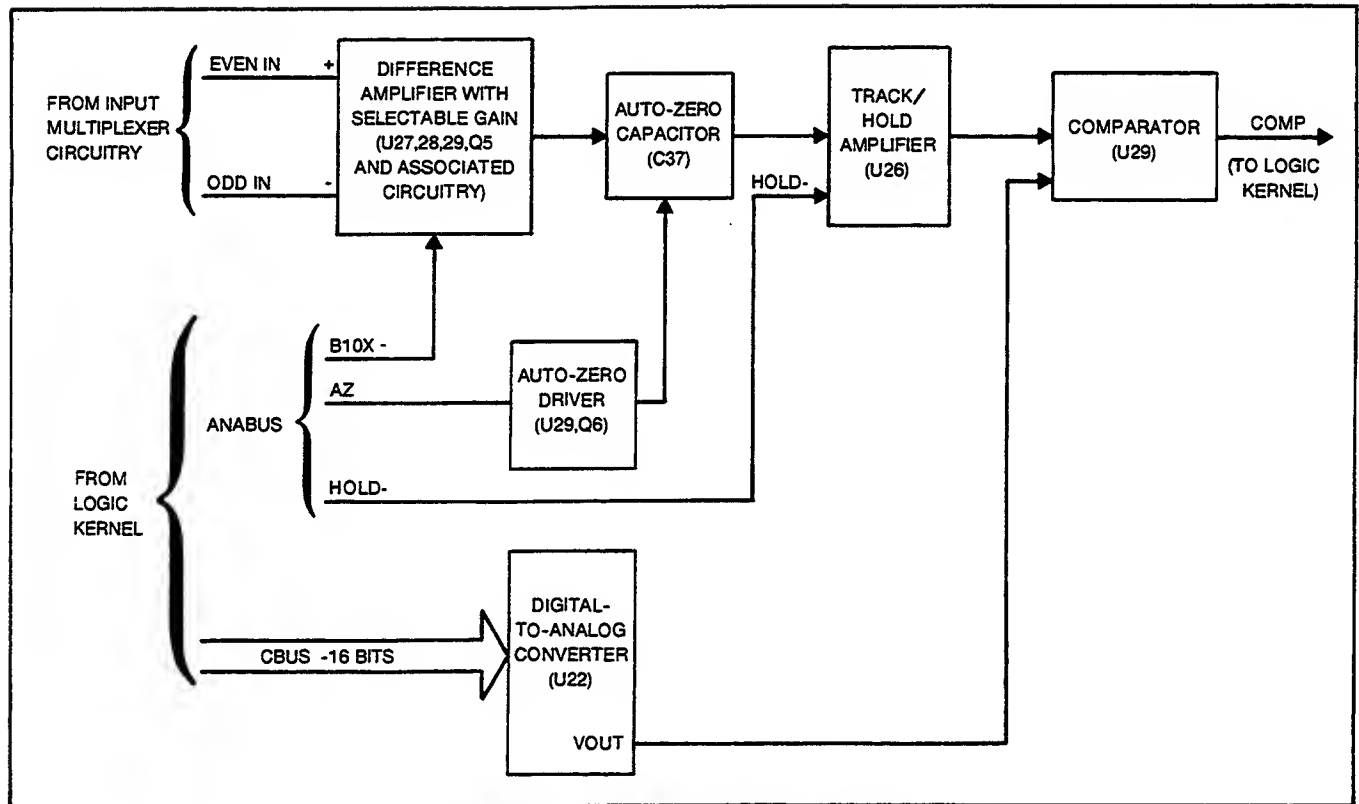


Figure 010-5. Analog-to-Digital Circuitry

The track/hold amplifier (U26) is usually operating in the tracking mode. When it is time to digitize the signal, the HOLD- signal from the logic kernel is pulled low, causing the track/hold amplifier to sample the voltage at its input and hold it. This helps eliminate digitization errors caused by AC components in the measurement input.

Comparator U29 compares the output of the Digital-to-Analog Converter (U22) to the sampled voltage present at the output of the track/hold amplifier. When the voltage from the Digital-to-Analog Converter (DAC) exceeds the sampled voltage, the comparator pulls COMP to approximately -0.7V, which is fed back to the Logic Kernel. The COMP signal is used by the Logic Kernel for the successive approximation algorithm used in digitizing the input.

010-13. Self-Calibration Sequence

At the initiation of scanning, and at approximately 17-second intervals thereafter, the Analog Measurement Processor suspends input channel scanning and executes a self-calibration cycle. This cycle compensates for any gain and offset drift that may be present in the internal A/D circuitry.

The calibration cycle consists of five parts: zero correction, gain correction for positive and negative inputs in the 10 volt range, and gain correction for positive and negative inputs in the 1 volt range.

Zero correction is obtained by connecting the EVENIN and ODDIN inputs to the A/D circuitry to analog ground through the Input Multiplexer circuitry. The Analog Measurement Processor then takes four readings and divides the sum of the readings by four to obtain an OFFSET value.

Gain correction for each range and polarity is accomplished by taking readings of the on-board calibration references and comparing them to expected readings for the references. The expected readings for the references are entered into non-volatile EEPROM memory during calibration of the Analog Measurement Processor. Refer to the paragraphs on calibration for more information.

To obtain the gain correction factors for positive inputs in the 10V and 1V ranges, the EVENIN input to the A/D circuitry is connected to the 6.95V and 0.695V references through the Input Multiplexer circuitry. The ODDIN input is connected to analog ground. Four readings of each of the references are averaged and compared to the expected readings to compute the gain correction factors.

Gain correction factors for negative inputs in the 10V and 1V ranges are obtained in a similar manner with the ODDIN input to the A/D circuitry connected to the 6.95V and 0.695V references.

After a self-calibration cycle, the Analog Measurement Processor performs corrections on all future readings

using the zero and gain corrections obtained. For each reading, the Analog Measurement Processor subtracts the OFFSET value. It then multiplies the result by the gain correction factor that corresponds to the range and polarity of the input. The resulting value is the reading that is passed to the user.

010-14. Measurement Sequence

010-15. SINGLE-ENDED MEASUREMENT TIMING

For the following discussion, refer to Figure 010-6 and the schematic diagram in Section 5. At the start of every measurement, the Analog Measurement Processor's A/D circuitry is auto-zeroed. When auto-zeroing, the logic kernel drives ET0 high and T1 and T2 low. This causes the EVENIN and ODDIN inputs to the A/D circuitry to be grounded through the input multiplexer circuitry. In addition, the AZ signal from the logic kernel is driven high, causing one end of the auto-zero capacitor (C37) to be grounded.

During the auto-zero period the logic kernel also selects the desired range for the input through the B10X- signal and sets the track/hold amplifier to the tracking mode by driving HOLD- high. (B10X- is low for readings in the 1V range.)

At the end of the auto-zero period, the AZ signal from the control logic is driven low, releasing the auto-zero capacitor from ground. The desired input is then switched into the A/D circuitry. For single-ended measurements, the logic kernel drives either EM0 or EM1 high depending on the channel being measured. EM0 is driven high for even-numbered channels and EM1 is driven high for odd-numbered channels. Control bits M0 through M3 are set to the appropriate binary value for the channel being measured.

In addition, T1 and T0 are set to the appropriate levels by the logic kernel in order to supply the ground reference required for single-ended measurements to the A/D circuitry. For even-numbered channels, T1 is driven high and T0 is driven low, causing the ground reference to be routed to the ODDIN input to the A/D circuitry. For odd-numbered channels, T1 is driven low and T0 is driven high, causing the ground reference to be routed to the EVENIN input.

After the A/D circuitry has settled, the logic kernel drives HOLD- low, causing the track/hold amplifier to sample the input and hold it. The logic kernel then digitizes the signal using a successive approximation technique. The technique involves sending 16-bit values to the Digital-To-Analog converter chip and comparing the output of the Digital-To-Analog converter to the sampled input. When the output of the DAC is greater than the sampled

input, COMP goes low, signaling the logic kernel to reduce the voltage output of the DAC.

010-16. DIFFERENTIAL MEASUREMENT TIMING

For the following discussion, refer to Figure 010-7 and the schematic diagram in Section 5. At the beginning of every measurement, the A/D circuitry on the Analog Measurement Processor is auto-zeroed in an identical manner to single-ended measurements. (See Single-Ended Measurement Timing.)

At the end of the auto-zero period, the AZ signal is driven low, releasing the auto-zero capacitor from ground. The desired input is then switched into the A/D circuitry. For differential measurements, ET0 is driven low, and EM0 and EM1 are driven high. M0 through M3 are set by the Logic Kernel to the appropriate binary value for the pair of channels being measured.

After the A/D circuitry has had time to settle, the Logic Kernel drives HOLD- low and digitizes the input in an identical manner to single-ended measurements.

010-17. MAINTENANCE

WARNING

THE 1752A CONTAINS HIGH VOLTAGES. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE 1752A. TURN OFF THE INSTRUMENT AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

The following paragraphs describe maintenance procedures for the Analog Measurement Processor. These procedures include calibration, hardware setup, performance testing, and troubleshooting. See Table 3-1 in Section 3 for a list of required equipment for testing and troubleshooting.

010-18. Calibration

To ensure accuracy, the Analog Measurement Processor should be calibrated every 90 days. To calibrate the 1752A, use the calibration program shipped with the 1752A System Disk in conjunction with the following instructions.

The Analog Measurement Processor is calibrated by running the calibration program (CAL) on the 1752A System Disk. The program prompts you to measure two on-board reference voltages, which are nominally 6.95V and 0.695V, and enter your measured voltage readings using the 1752A keyboard. The calibration program stores these readings in nonvolatile memory, to be used during self-calibration cycles.

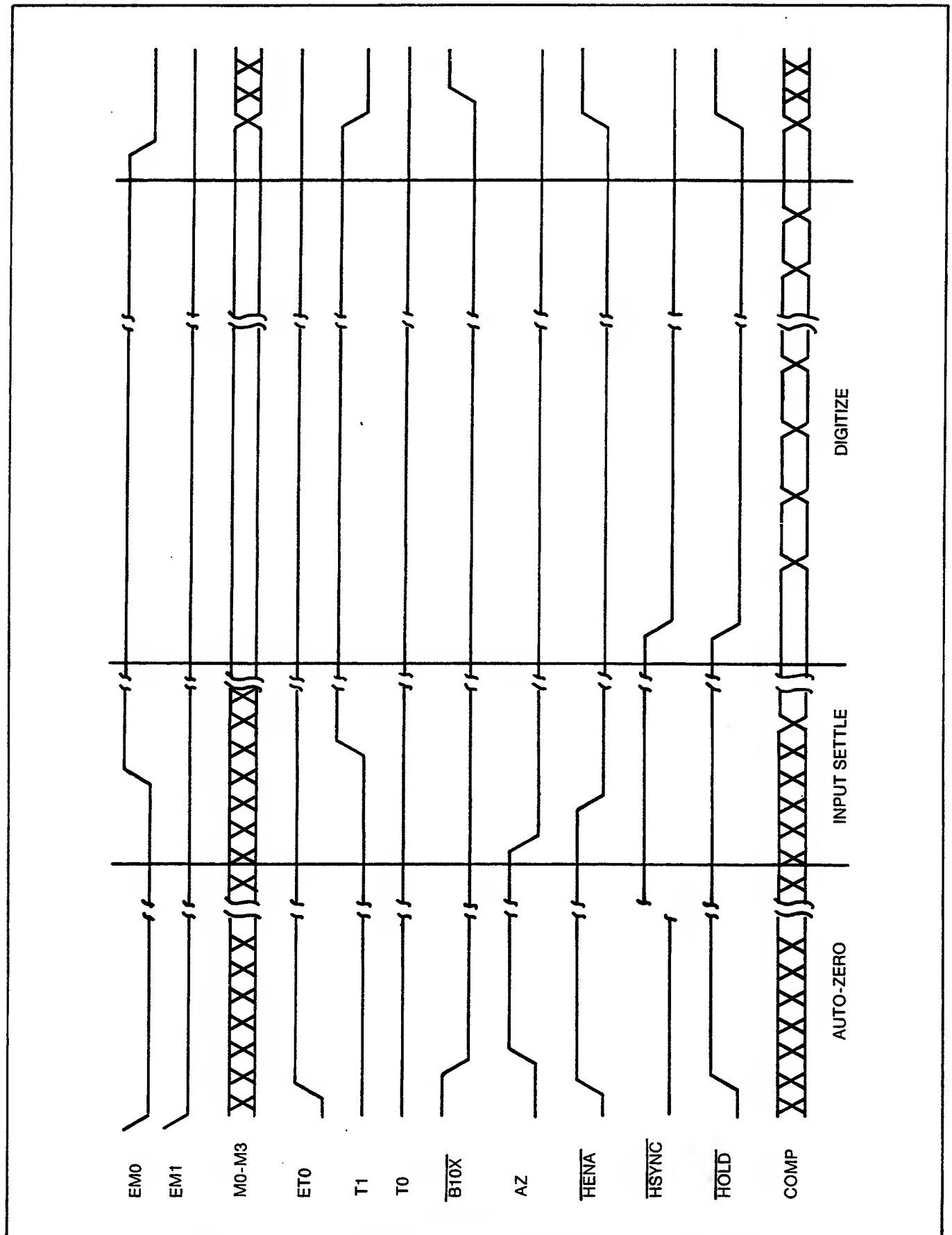


Figure 010-6. Single-Ended Measurement on an Even-Numbered Channel

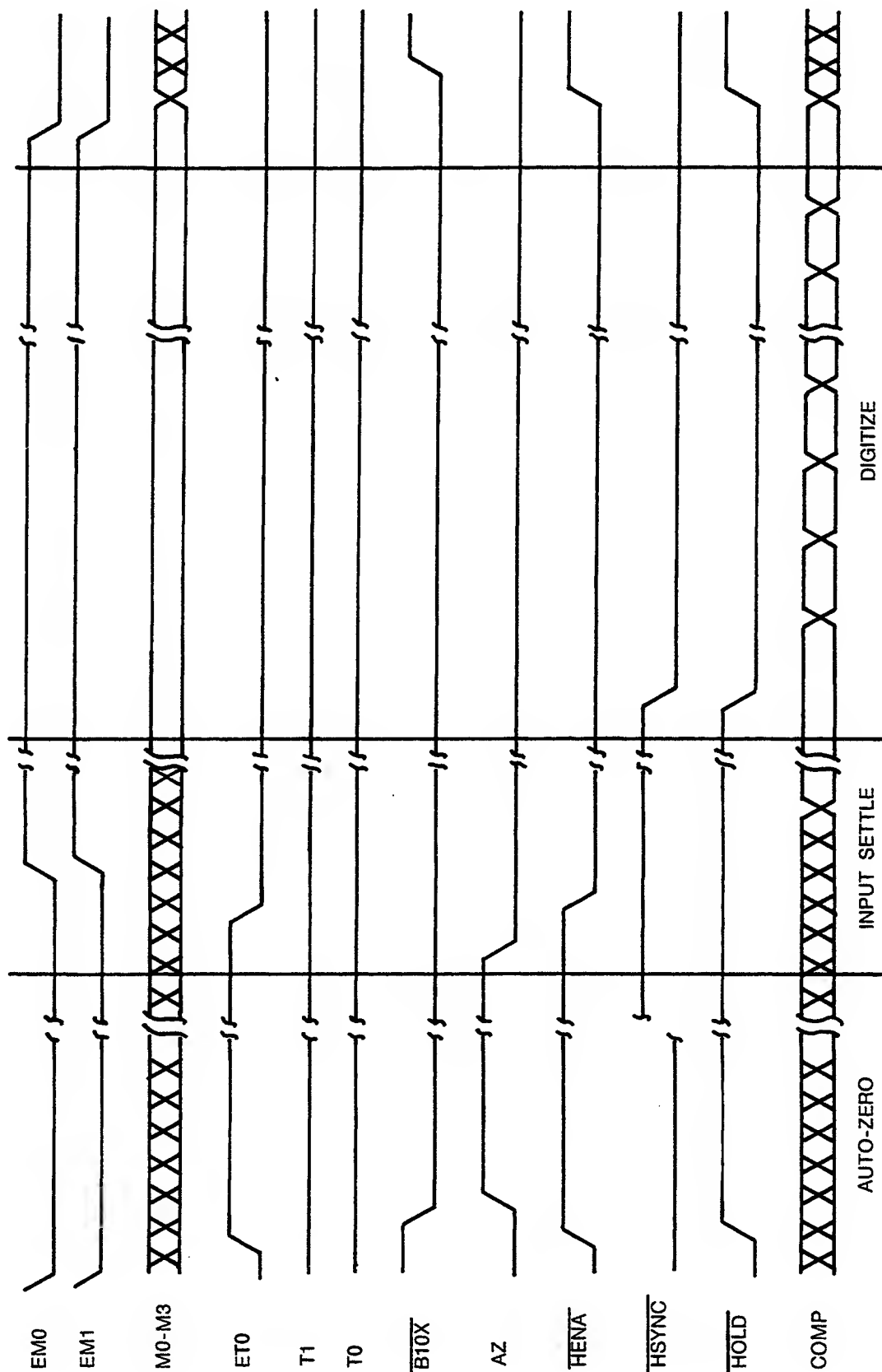


Figure 010-7. Differential Measurement Timing

When you enter the voltage readings, the calibration program checks the values. If the values are out of tolerance, the program will reject the values and an error message will appear. If you are correctly entering the value of the reference and the error message still appears, the board's reference is out of tolerance and needs to be repaired. In this case, refer to the 1752A Service Manual, Section 3, or call your local Fluke Service Center.

Before attempting to calibrate the Analog Measurement Processor, you must first enable writing to nonvolatile memory on the board. Refer to the paragraph on the Calibration Procedure for more information. Failure to enable writing to memory will cause an error message to appear on the screen when the calibration program is run.

Once the board is calibrated, you must remember to write-protect the nonvolatile memory. Failure to do so allows firmware on the board to be altered, causing the board to malfunction.

010-19. REQUIRED EQUIPMENT

The following equipment is required to calibrate the Analog Measurement Processor:

- 1752A Data Acquisition and Control System

- 1752A System Disk
- Fluke 8840A Digital Multimeter (DMM) or equivalent 5½ digit DMM

010-20. CALIBRATION PROCEDURE

To calibrate the Analog Measurement Processor, proceed as follows:

1. Switch the 1752A power off.
2. Remove the Analog Measurement Processor from the 1752A.
3. Enable writing to the board's nonvolatile memory as follows:
 - a. Close the write-enable switch (segment 1 of Address Selection Switch S1).
 - b. Place any one of the voltage/current configuration jumpers over the write-enable pins (JPR36). JPR36 is located just above Switch S1. Refer to Figure 010-8 for calibration jumper locations.

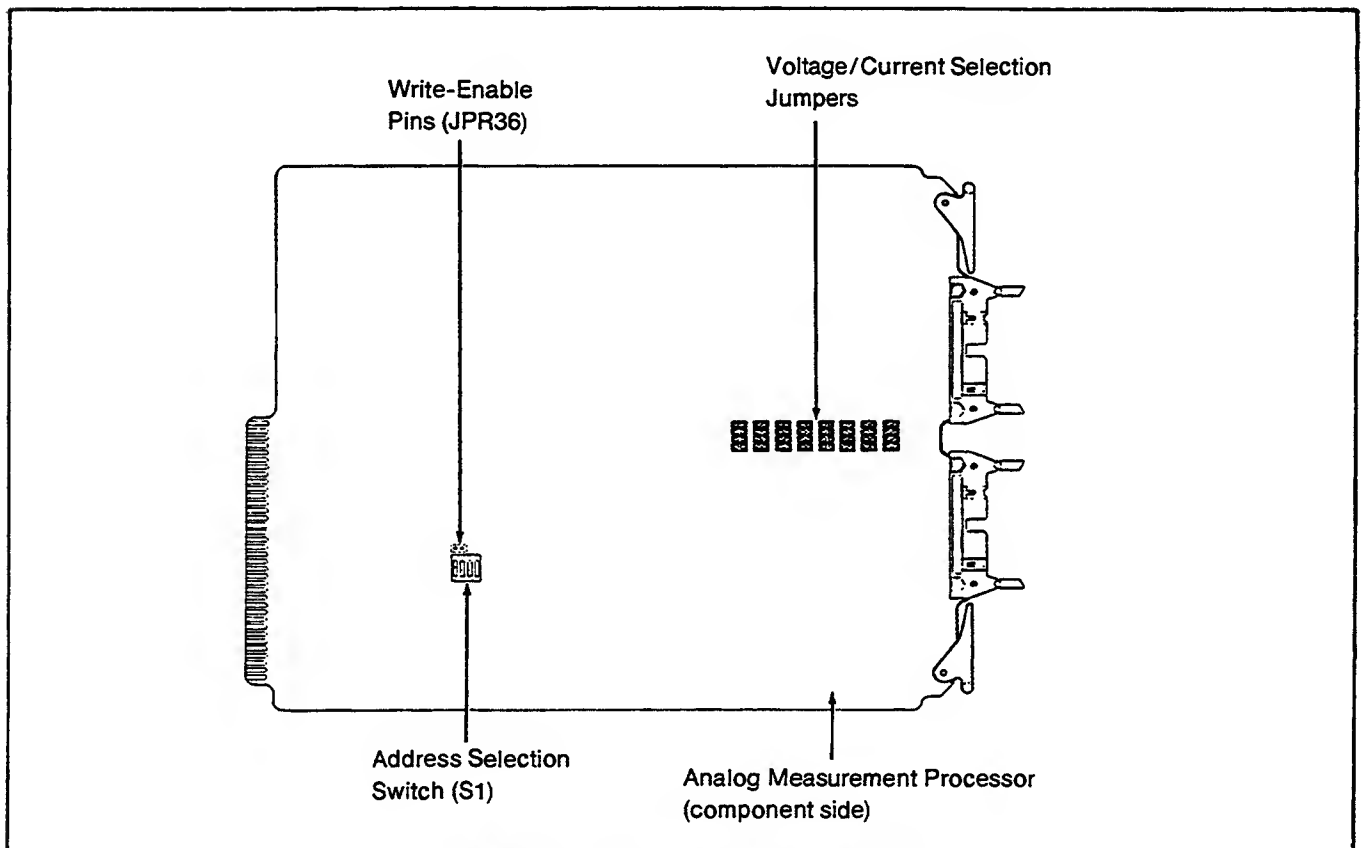


Figure 010-8. Calibration Jumper Location

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4. Place the Analog Measurement Processor back into the 1752A.
5. Switch the Digital Multimeter (DMM) power on. Set up the DMM to measure dc voltage in the 20V range.
6. Insert the 1752A System Disk into the 1752A and switch the power on.
7. After the System Disk has loaded, return to FDOS by typing <CTRL>/p. Type "cal" at the FDOS prompt, followed by a RETURN.
8. At the program prompt enter the board address (0 through 3) of the module being calibrated, followed by a RETURN.
9. Connect the + input lead of the DMM to TP2 and the - input lead to TP3. Refer to Figure 010-9 for test point locations. Using the 1752A keyboard, enter the reading of the DMM to the nearest 100 μ V following the 6.95V reference prompt.
10. Place the DMM in the 2V range. Connect the + input lead of the DMM to TP1 and the - input

lead to TP3. Using the 1752A keyboard, enter the reading of the DMM to the nearest 10 μ V following the 0.695V reference prompt.

11. Switch the 1752A power off.
12. Remove the Analog Measurement Processor.
13. Protect the board's nonvolatile memory as follows:
 - a. Open the write-enable switch (segment 1 of Address Selection Switch S1).
 - b. Remove the jumper from the write-enable pins (JPR36) and return the jumper to its original location with the other voltage/current configuration jumpers.

CAUTION

Failure to open the write-enable switch and return the jumper to its original location may cause the respective channel to malfunction and/or allow the board's firmware to be altered.

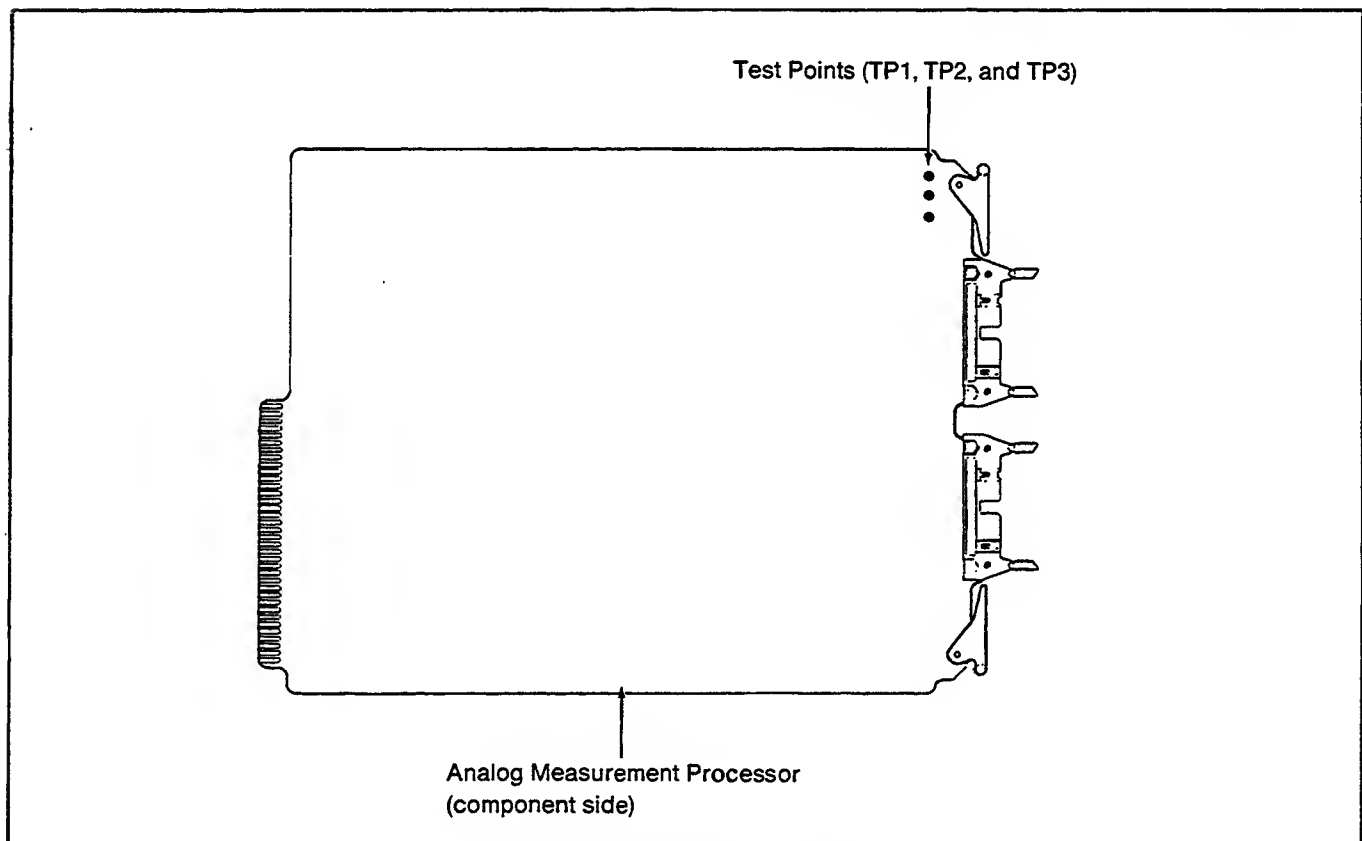


Figure 010-9. Test Point Locations

14. Reinstall the Analog Measurement Processor in the 1752A. This completes the calibration procedure.

010-21. HARDWARE SETUP

There are four user-adjustable hardware settings on the Analog Measurement Processor: voltage/current selection (each channel is configured to take voltage or current readings); the board address; external calibration write-enable/disable; and external sync signal frequency range. The settings are configured at the factory as follows:

- All channels are configured for voltage measurement.
- The board address is set to zero.
- Calibration is write-disabled.
- External sync frequency range is 45-65 Hz.

To change or check the settings on a board that is already installed in the 1752A, remove the board as described in Section 3. To change or check the settings on a board that is not yet installed, proceed to the paragraph on Setting the Board Address.

010-22. SETTING THE BOARD ADDRESS

Each Analog Measurement Processor has a board address which is set by Address Switch S1. The board address determines channel numbers of the board's 32 analog input channels.

Before installing an Analog Measurement Processor, check the board address as set by segments 3 and 4 of the Address Switch. Refer to Figure 010-10 for the Address Switch location and selections.

The first Analog Measurement Processor in your system should have board address 0. The second board should have address 1, the third board address 2, and the fourth board address 3. Verify that switch segments 3 and 4 are set for the correct board address.

A 1752A system can have up to four Analog Measurement Processors. Input channels are labeled consecutively from 0 to 127, corresponding to the 128 input channels available in a system with four Analog Measurement Processors. The channels are assigned in blocks of 32.

010-23. Configuring Channels For Voltage Or Current Readings

The Analog Measurement Processor is shipped from the factory with all channels configured as voltage inputs.

Each analog input channel can be configured with jumpers to be in either voltage or current input mode.

Since current readings are differential, current configuration requires that two consecutive channels be configured.

To change a pair of channels from voltage to current, move the two jumpers for the channels from the horizontal position to the vertical position, covering the same four pins. Refer to Figure 010-11 for voltage/current jumper configurations. Even-channel numbers are silk-screened on the circuit board to identify the pair of channels being configured. To change a channel back to voltage mode, simply reverse this procedure.

010-24. Selecting External Sync Frequency Range

Jumper 2 (JPR2), located between components U24 and U25 on the circuit board, selects the acceptable frequency range for externally synchronized input scanning. Orient the board as shown in Figure 010-12. To select the 45 to 65 Hz range, place the jumper over the center and left-most pins. To select the 360 to 520 Hz range, place the shorting block over the center and right-most pins.

010-25. PERFORMANCE TEST

The System Diagnostic Software verifies proper operation of a large portion of the Analog Measurement Processor circuitry without the need for external inputs. While this software detects many of the errors seen by factory technicians, additional tests are required to thoroughly test the option. This section presents additional performance test procedures.

In the following paragraphs, the lowest 16 channels of the Analog Measurement Processor under test are referred to as channels 0-15, and the highest 16 channels are referred to as channels 16-31.

The following equipment is required to complete the performance test: a Fluke Y1750 Termination Block with Cable, a DC Calibrator (Fluke 343A or equivalent), and the 1752A System Diagnostic Disk.

1. Switch the 1752A and DC Calibrator power off.
2. Using the Y1750 Termination block with cable, connect the high (+) output calibrator terminal of the calibrator to channels 0-15 of the Analog Measurement Processor. Refer to Figure 010-13 for connector pinouts.
3. Connect the low (-) output terminal of the calibrator to the COMMON REFERENCE

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and POWER GROUND inputs of the Analog Measurement Processor. Use two separate wires from the calibrator to the Y1750 termination block for this connection.

4. Insert the System Diagnostic Disk into the 1752A and switch the 1752A power on.
5. Switch the calibrator power on.
6. After the System Diagnostic Software has loaded, run ADTST under the Analog Measurement Processor subtest menu. Refer to Section 3 of this manual for information on the System Diagnostic Software.

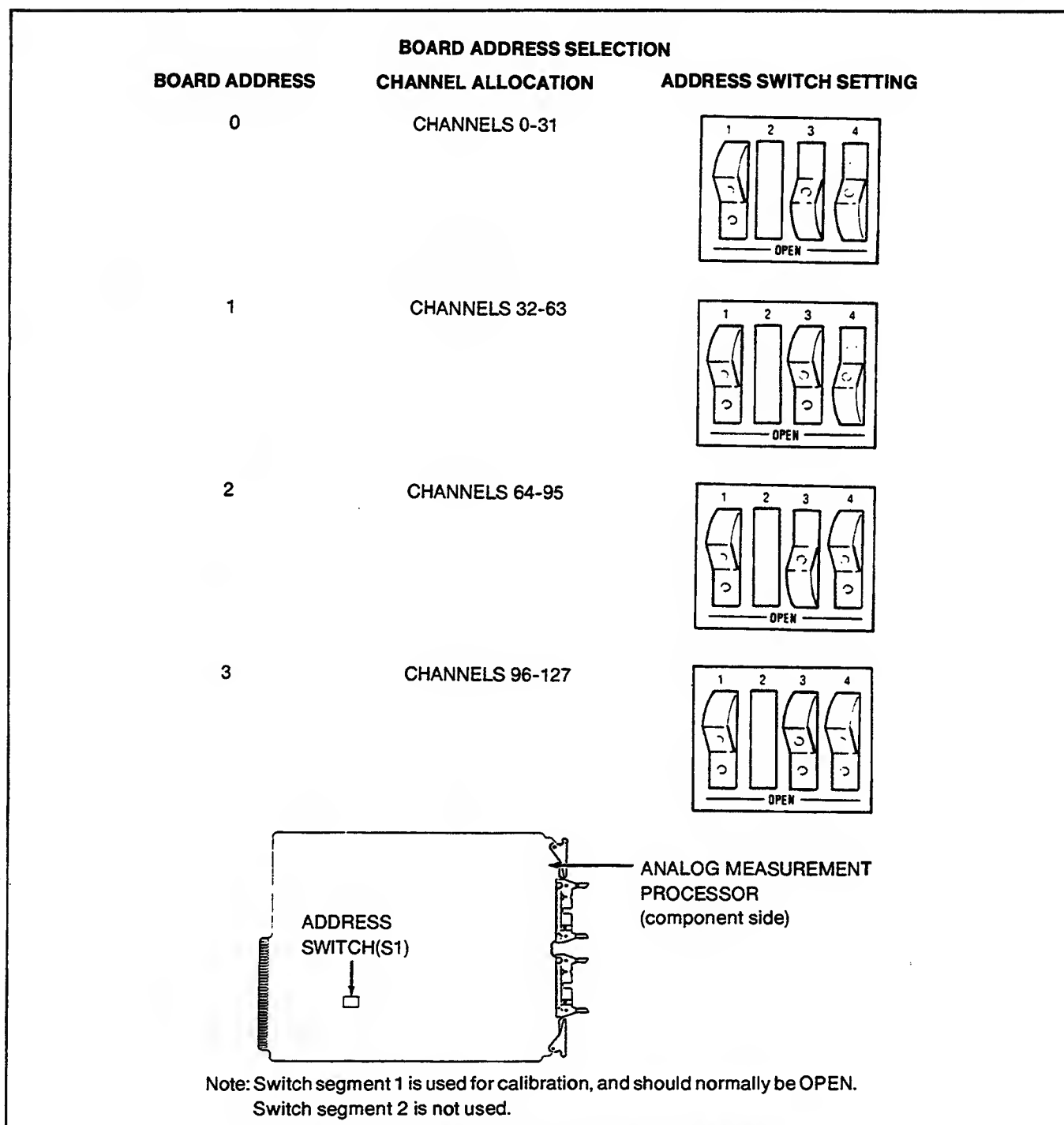


Figure 010-10. Board Address Location and Selection

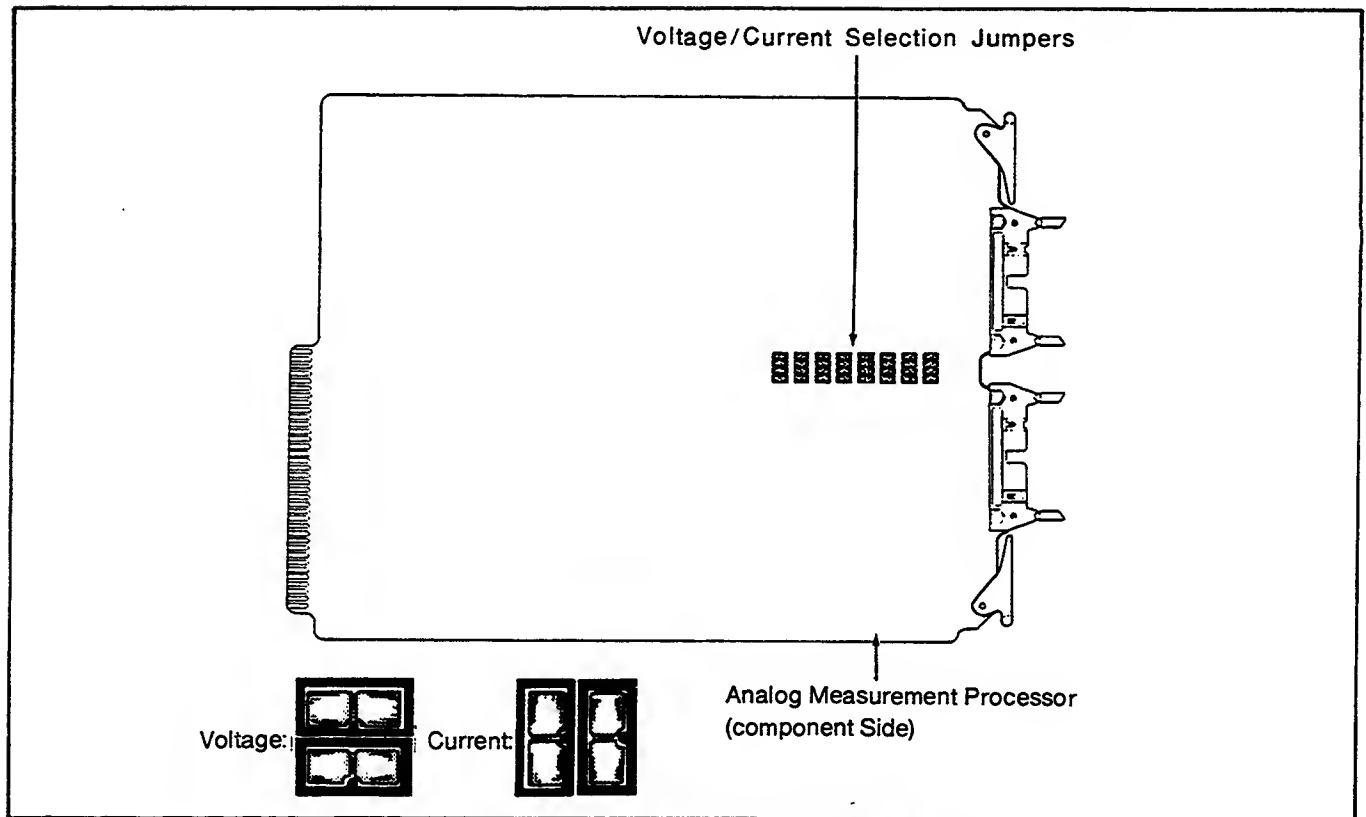


Figure 010-11. Voltage/Current Selection

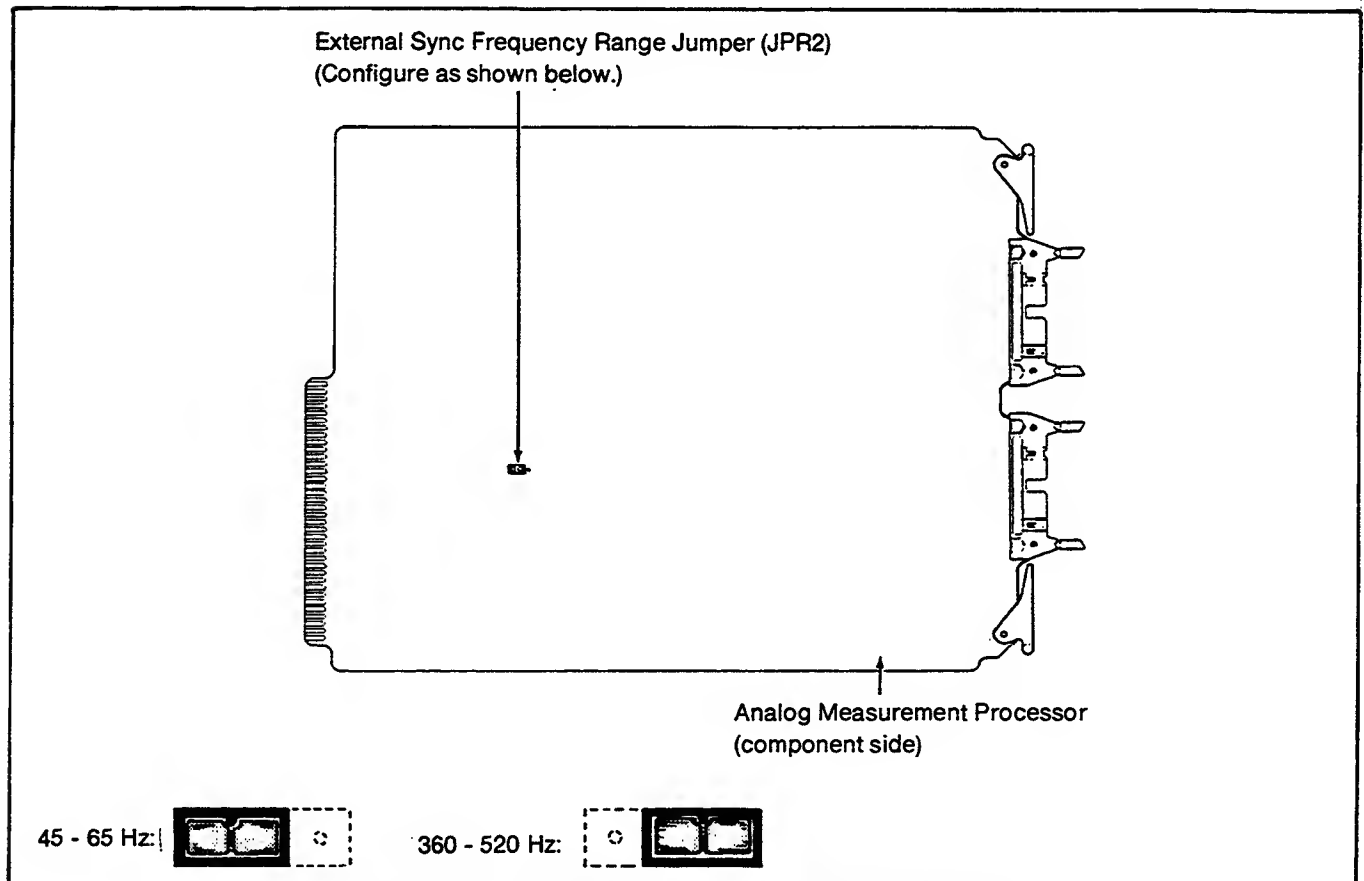
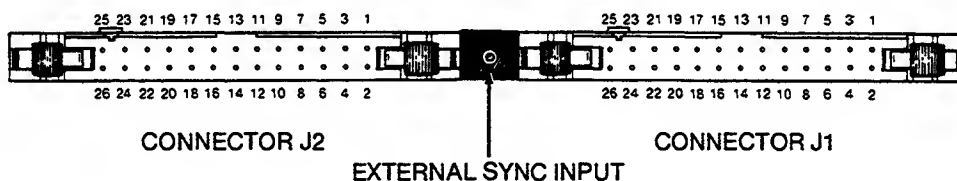


Figure 010-12. External Sync Frequency Range Selection

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INPUT CONNECTORS



INPUT CONNECTOR PIN ASSIGNMENTS

PIN NUMBER (CONNECTOR J1)	CHANNEL NO.	PIN NUMBER (CONNECTOR J2)	CHANNEL NO.
1	0	1	16
2	1	2	17
3	(Signal Ground)	3	(Signal Ground)
4	2	4	18
5	3	5	19
6	(Signal Ground)	6	(Signal Ground)
7	4	7	20
8	5	8	21
9	(Signal Ground)	9	(Signal Ground)
10	6	10	22
11	7	11	23
12	(Signal Ground)	12	(Signal Ground)
13	8	13	24
14	9	14	25
15	(Signal Ground)	15	(Signal Ground)
16	10	16	26
17	11	17	27
18	(Signal Ground)	18	(Signal Ground)
19	12	19	28
20	13	20	29
21	(Signal Ground)	21	(Signal Ground)
22	14	22	30
23	15	23	31
24	(Signal Ground)	24	(Signal Ground)
25	(Not Used)	25	(Not Used)
26	(Power Ground)	26	(Power Ground)
Notes Signal grounds are connected together internally. Channel numbers are shown for board address 0.			

Figure 010-13. Input Connector Pin Assignments

7. After ADTST is running, use the Touch-Sense buttons on the screen to increment or decrement the board being addressed by the program to match the board address of the module being tested.
8. Press the SCAN menu button.
9. Output -10V from the calibrator and verify that channels 0-15 are reading within $-10V \pm 3.24 \text{ mV}$.
10. Set the calibrator output to 0V.
11. Press the CHAN menu button. Using the buttons presented on the 1752A screen, program channels 0-15 with the following channel parameters:

MODE - SNGL
ENABLE - READ
RANGE - 1V
FILTER - 1
12. Press the SCAN menu button.
13. Output -1V to 1V from the calibrator in 0.2V increments. At each voltage increment, verify that channels 0-15 are reading within the accuracy specifications of $\pm(0.02\%$ of input $+248 \mu\text{V}$).
14. Move the input cable from connector J1 to connector J2.
15. Output 10V from the calibrator and verify that channels 16-31 are reading within $10.0V \pm 3.24\text{mV}$.

010-26. TROUBLESHOOTING

System Diagnostic software is provided with the 1752A to aid in identifying faulty modules. The software contains subtests for specific functions of the -010 option. The System Diagnostic consists of an EEPROM Checksum Test, RAM Test, Calibrate Routine, Phase-locked Loop Test, Open Tests, Ground Tests, Isolation Tests, and ADTST. For more information on the System Diagnostic tests, see Section 3.

If an error is encountered by the System Diagnostic during the execution of a test, an entry is made in an error log. IF STOP ON FAIL was selected from the Main Menu, an error message will be displayed on the screen. If an error condition exists, first verify that the module is faulty and then replace it. (If the System Diagnostic will not load and run, see Section 3, Troubleshooting.)

If a board is failed by the System Diagnostic Software, the following troubleshooting procedures may be used to isolate the failure. Due to the great number of possible problems, only the most common problems encountered by factory technicians are discussed. If the failure encountered is not discussed in this section, contact the nearest Fluke Service Center. (See Section 4.)

Component-level troubleshooting is recommended only when it is not possible to replace a defective module. If you attempt to repair a module, you will need, at a minimum, the following equipment: a multi-trace oscilloscope, a $5\frac{1}{2}$ digit multimeter, a logic probe and a quantity of replacement components. Most chips are soldered into the circuit board, so it will be necessary to unsolder components in order to swap them.

CAUTION

Extreme care should be used when removing and replacing components to avoid irreparable damage to the printed circuit boards.

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

SYMPTOM 1:

System Diagnostic returns the following error: option is faulty, missing or improperly configured. Or, while running a BASIC program, one of the following error messages appears: Analog Input Channel Not Installed, or Analog Measurement Processor Not Installed.

POSSIBLE CAUSE:

Bus interface logic is faulty.

ACTIONS:

- Verify that the address switches are correctly set for the corresponding board address.
- Run RAM Test in loop mode. RAM Test is located under the Analog Measurement subtest menu.
- Look for logic activity at U14, pin 33 (active low). If logic activity is not present at U14, the error is caused by the Address Decoding Logic (U5, U6, U7, U11, U16, U20, U21).
- Look for logic activity at U9, pin 5 (active low). If logic activity is not present at pin 5, the error is caused by the Bus Grant Circuitry (U9, U14, U17, U20).

SYMPTOM 2:

While running a BASIC program, the module returns a calibration error.

POSSIBLE CAUSES:

- Option is out of calibration.
- +15V and/or -15V charge pump supply is faulty.
- Input amplifier circuitry is faulty.
- Digital-to-analog converter circuitry is faulty.
- Analog-to-digital comparator is faulty.

ACTIONS:

- Calibrate the module to verify that the module is calibrated correctly.
- Measure the +15V and -15V charge pump supplies and verify that each supply is within $\pm 0.6V$ of its nominal value.
- Measure the 0.695V and 6.95V voltage references and verify that they are within $\pm 0.040V$ and $\pm 0.35V$, respectively.
- Using ADTST under the Analog Measurement Processor subtest menu, program all channels to be skipped and verify the following:
 - a. Verify that the input to U26, pin 3 toggles between approximately +7V and -7V. Probable cause for failure lies in the calibration circuitry (U32, U33, U34, Z5, and associated circuitry), or the input amplifier (U27, U28, U29, and associated circuitry).
 - b. Verify that the voltage at U26, pin 5 follows the same increase and decrease voltage pattern of U26, pin 3. Possible cause for failure includes U15 or U26.
 - c. Verify that the Digital-to-Analog Converter Output (U22, pin 17) toggles between +7 and -7V. Possible cause for failure includes U12, U13, U19, and U22.
 - d. Verify that the output toggles at U29, pin 14.

SYMPTOM 3:

One or two single-ended channel readings on the module are inaccurate, while the rest of the channels are within specification.

ACTIONS:

- The inaccurate channel reading is probably caused by either the protection circuitry or the input multiplexer of the inaccurate channel. For example, if the reading for channel 0 is inaccurate, the problem is most likely caused by the circuit failure of R46, Q14, Q16, or U35.

SYMPTOM 4:

All single-ended channel readings are inaccurate with the inaccuracy proportional to the input voltage.

POSSIBLE CAUSE:

- Option is out of calibration.

ACTIONS:

- Calibrate the module to verify that the module is calibrated correctly.

SYMPTOM 5:

Even-numbered single-ended channel readings are inaccurate.

POSSIBLE CAUSE:

- Even channel input multiplexer is faulty.
- Reference multiplexer is faulty.

ACTIONS:

- Replace U35.
- Replace U34.

SYMPTOM 6:

Odd-numbered single-ended channel readings are inaccurate.

POSSIBLE CAUSE:

- Odd channel input multiplexer is faulty.
- Reference multiplexer is faulty.

ACTIONS:

- Replace U36.
- Replace U34.

Option 1752A-011 Analog Output Module

011-1. INTRODUCTION

The Analog Output module allows the 1752A Data Acquisition and Control System to send programmable voltages or currents to external control points, under the control of a BASIC program or BASIC commands. The module gives the 1752A the ability to control many kinds of devices and processes.

The module has four fully-isolated addressable output channels. By setting jumpers on the module, you can configure each output channel to output either voltage or current. When the jumpers are changed, the channel must be recalibrated using the calibration procedure provided at the end of this section. (The module can also be calibrated at a Fluke Technical Service Centers, see Section 4 for locations.)

Output voltages from the Analog Output module are programmable over a -10.2375V to $+10.2375\text{V}$ range, with a resolution of 2.5 mV . Current from the module can be programmed over a 0 to 20.475 mA range, with a resolution of $5\text{ }\mu\text{A}$. Each channel is isolated from the digital common and the other channels on the board (maximum 30V common mode).

Each Analog Output module is assigned a unique board address by setting switches on the module. The board address determines the channel numbers for the four outputs. An address selection procedure is provided in the paragraph on Hardware Setup, later in this section.

The Analog Output module is controlled by subroutines that can be called from programs written in BASIC. The subroutines are collected together in the Analog I/O Library (AIOLIB), which is supplied on the 1752A System Disk.

011-2. SPECIFICATIONS

For Analog Output module specifications, see Table 011-1.

011-3. THEORY OF OPERATION

011-4. Introduction

This section presents a functional and circuit description of the 1752A-011 Analog Output Module. These descriptions are supported by Figure 011-1 and the schematic diagrams in Section 5.

011-5. Functional Description

As shown in Figure 011-1, the 1752A-011 Analog Output module consists of four voltage or current output channels. Communication between the 1752A Single-Board Computer (SBC) and the Analog Output module occurs through the bus interface and control circuitry.

Each of the four channels in the Analog Output module has a unique read/write register located in the bus interface and control circuit. When a particular channel is addressed and output level data is written to the associated register, the information is then sent serially through four optical isolator circuits to each of the four digital-to-analog (D/A) converters (one per channel). Although the output level data is sent to all of the D/A converters, only the addressed converter latches the data.

The addressed D/A converter uses the output level data to produce the appropriate analog signal at the external connector. The appropriate mode (voltage or current output) is individually selected for each channel by means of jumper connections at the channel output.

In addition to an optically isolated serial communications circuit, each output channel also contains an isolated power supply. The power supply circuit provides isolated

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positive and negative 15V dc power outputs derived from the positive 5V dc logic power.

011-6. Circuit Description

011-7. BUS INTERFACE AND CONTROL CIRCUIT

The 1752A Single-Board Computer communicates with the Analog Output module through the bus interface and control circuit using memory mapped I/O operations. Each Analog Output module responds at four sequential word addresses, one for each channel, as decoded by the address buffer and decoder circuit. Up to 32 Analog Output modules may be installed in one system.

Refer to Figure 011-2 for a block diagram of the bus interface and control circuitry. Address decode circuitry (U62 through U64, U74 through U76, U51) in the bus interface and control block decodes the highest 15 bits of the 18-bit ARGUS bus address. If the address received falls within the address range set through the switch (S1), and if the ARGUS Address Valid signal (ADVAL) is asserted (low), the address decode circuit asserts the Buffer Decode Enable (BDEN) signal to a logic 1. The BDEN signal high state then drives the Address Acknowledge signal (ADACK) line to a logic 0 through Q5. At the end of the memory cycle, ADVAL, BDEN and ADACK are de-asserted.

Table 011-1. Analog Output Module Specifications

Number of Channels:	Four per module
System Capacity:	Two modules (eight channels) per 1752A 32 modules (128 channels) when using 1702A extender chassis
Configuration:	Each channel user-configurable for voltage or current. (Note: When changing configuration, the channel must be recalibrated.)
Update Rate:	1000 updates/sec
Slew Rate:	1.0V/ μ sec
Voltage Configuration	
Range:	$\pm 10.2375V$
Resolution:	2.5 mV
Maximum Source Current:	± 5 mA
Capacitive Load:	Will drive up to 10,000 pF without instability
Output Protection:	All outputs are short-circuit protected
Current Configuration	
Range:	0 to 20.475 mA
Resolution:	5 μA
Maximum Load:	750 ohms
Maximum External Voltage:	$\pm 24V$
Compliance Voltage:	15V
Accuracy:	0.1% of full scale (90 days, 18°C to 28°C)
Isolation:	Outputs are isolated from each other and from ground up to 30V dc
Compatible Connectors:	Fluke Option 2400A-110 Screw Terminal Connector or 2400A-111 Solder Pin Connector
Mounting:	Plugs into the 1752A chassis
Weight:	1.4 kg (3 lbs)

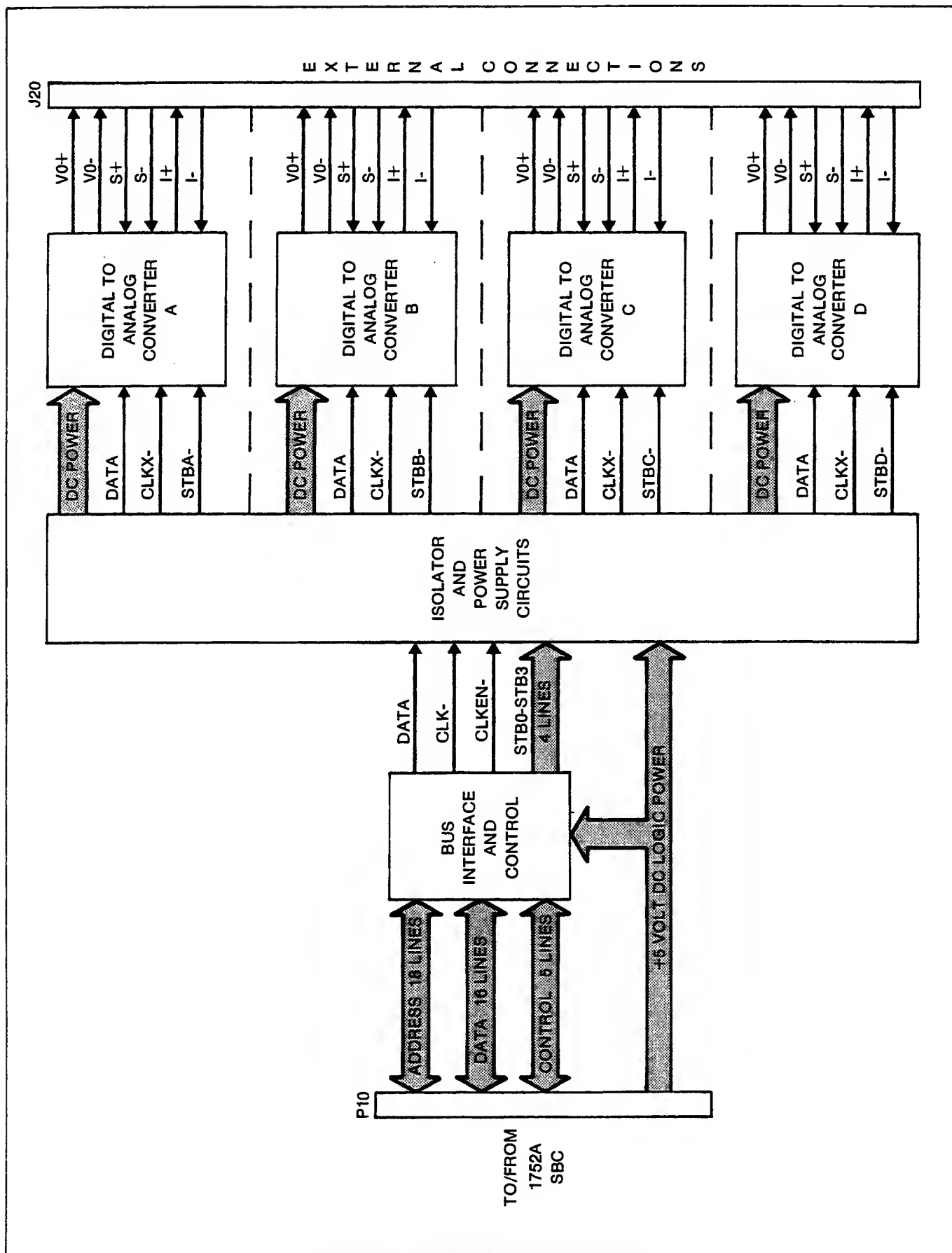


Figure 011-1. Analog Output Block Diagram

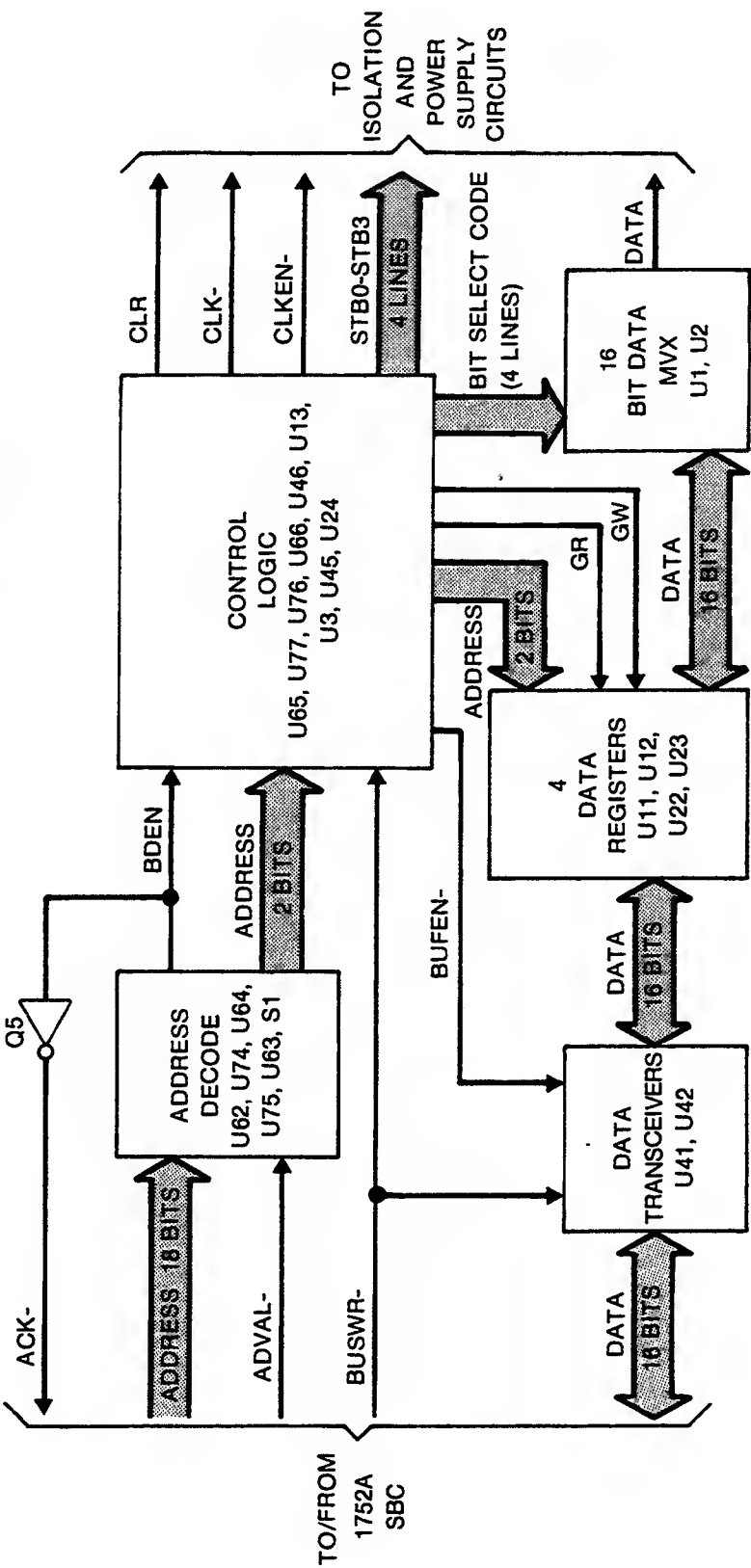


Figure 011-2. Bus Interface and Control Block Diagram

The Bus Write (BUSWR-) signal from the SBC determines whether data is written to or read from the data registers (U11, U12, U22, U23) through data transceivers U41 and U42. When an Analog Output read cycle occurs, BUSWR- is held high by the SBC, setting up the transceivers to allow the data registers to drive the ARGUS bus data lines to the SBC. When an Analog Output write cycle occurs, BUSWR- is driven low by the SBC setting up the transceivers to allow data from the ARGUS bus to drive the inputs to the data registers. Address bits A1 and A2 select one of four output channel registers to be read from or written to.

Figure 011-3 illustrates register read/write signal timing. An analog output read cycle occurs when the BUSWR- signal is held high by the SBC. As shown in the figure, when BDEN (generated in the address decode logic) and BUSWR- are both a logic 1, the Register Read (GR) and the Register Write (GW) signals generated in the control logic are set to a logic 0 and a logic 1 respectively, allowing a register read operation to occur. A logic 1 on

the BDEN and BUSWR- signals is also used in the control logic to drive the BUFEN- signal low, allowing data from the selected data register to be placed on the ARGUS Bus to be read by the SBC. The SBC reads the data bus just prior to setting ADVAL- high.

An Analog Output write cycle occurs when the BUSWR- signal is driven low by the SBC. The SBC can then write 16 bits of new output level data into one of the four output channel registers. As shown in Figure 011-3, when BDEN is at a logic 1 and BUSWR- is at a logic 0, the Register Read (GR) signal generated in the control logic goes to a logic 1. After the next rising edge of the SYNC signal from the SBC, the Register Write (GW) and BUFEN- signals are driven low by the control logic, allowing a register write operation to occur. One SYNC cycle later, the control logic sets the GW signal to a logic 1, latching the data on the ARGUS Bus into the addressed output channel register. One SYNC cycle after the control logic sets GW to a logic 1, BUFEN- is set to a logic 1, disabling the data transceivers. When BDEN goes to a logic 0, the write cycle is completed.

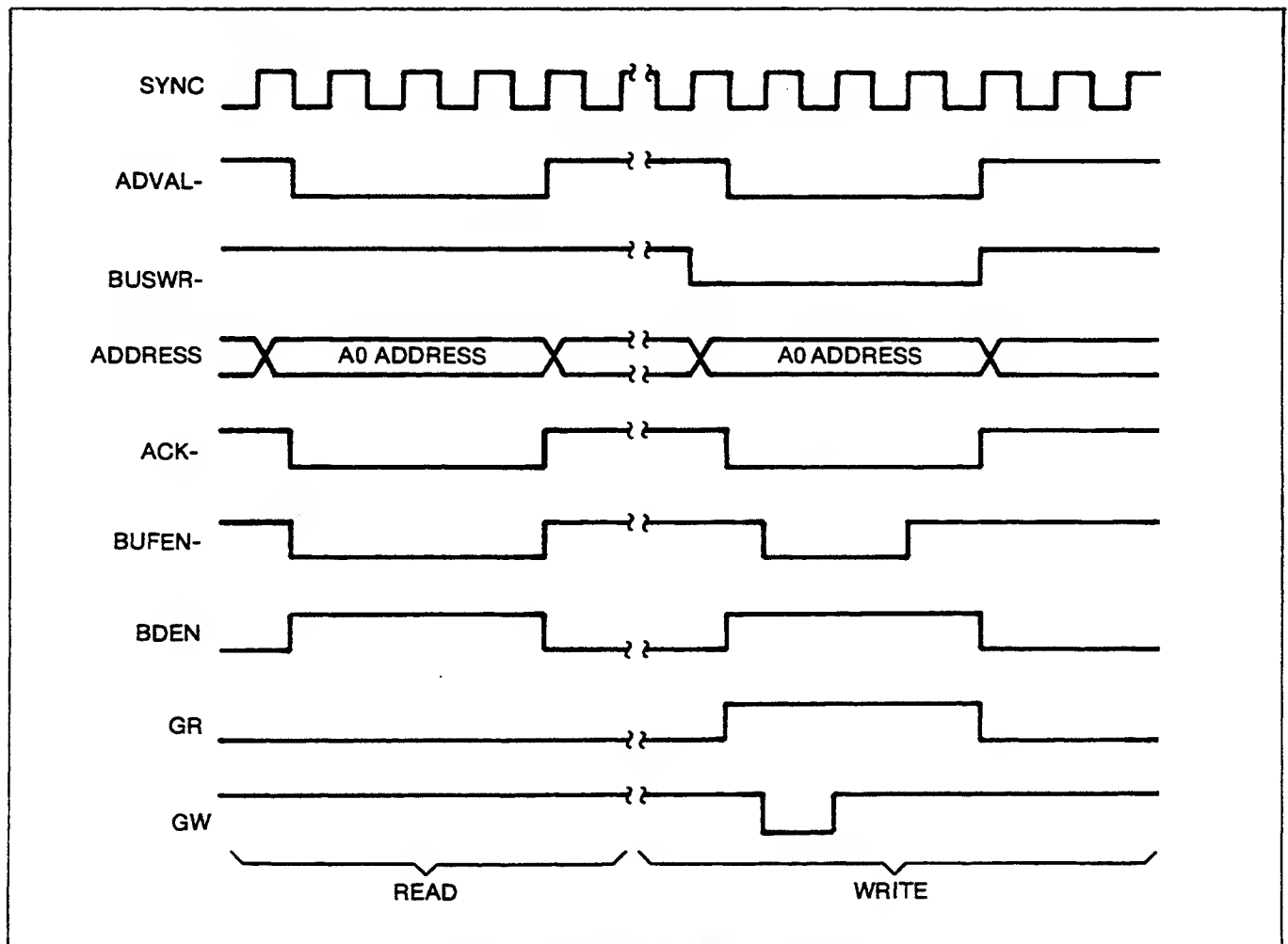


Figure 011-3. Register Read/Write Timing

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After new data has been written into the addressed register, the control logic transfers that data to the proper D/A converter. Figure 011-4 illustrates serial data transfer timing. When GR goes to a logic 1 as a result of an Analog Output write cycle, the control logic is reset, and the control timing signal (CLK) is initialized to a logic 1. At the same time, the enable signal (CLKEN) is set to a logic 0. A logic 1 GR signal also resets a 16-bit data multiplexer (U1, U2) to select bit 15. As a result, data is transferred serially in sequence starting with bit 15 and going to bit 0 during the next 16 clock cycles.

When GR returns to logic 0 following the write operation, the serial data transfer begins. The data bit to be transferred is multiplexed onto the DATA line at each CLK transition from logic 0 to logic 1. Latched address bits A1 and A2 are used by the control logic to generate a logic 1 level on the proper Strobe (STB) line after all 16 bits have been serially transferred.

011-8. ISOLATION AND POWER SUPPLY CIRCUIT

Four individual dc-to-dc power supplies provide isolated power for each of the four Analog Output module channels. Refer to Figure 011-5 for a block diagram of the Isolation and Power Supply circuitry. A control and drive circuit (U77, U78, U25, Q1 through Q4) drives four separate transformer primary windings, (one for each channel) in parallel. Power for the supplies is derived from the positive 5V dc logic power supply. Control for the transformer drive circuit is based on the System

Clock (SYNC-) signal. The protection circuit (U44) in the isolated power supply contains a mono-stable multi-vibrator that disables the transformer drive transistors if no SYNC transitions have occurred for 3 μ secs.

Through a series of gates, two transistor drive circuits are switched on and off by non-overlapping waveforms to generate a 46.875 kHz transformer drive signal. The inverter outputs are rectified into positive and negative 26V dc supplies, then regulated to positive and negative 15V dc supplies. The 26V dc unregulated supply is also available for use as the current source on Analog Output modules configured for current mode operation.

Each output channel includes three optically isolated communication paths used to transfer data from data registers to the D/A converter circuit. The three signals transferred are DATA, CLK-, and STB.

The CLK- and CLKEN- signals from the control logic are gated together within the isolator drive circuit (U45, Q6) to produce a common clock (CLKX-) signal. The CLKX- signal is presented to all four channels during data transfer. Serial data from the 16-bit data multiplexer is transferred over the DATA line and presented to all four channels. At the end of the data transfer, the STB signal that corresponds to the addressed channel is pulsed to a logic 1, and the new output level data is latched by the addressed channel. STB will remain inactive on the other three channels.

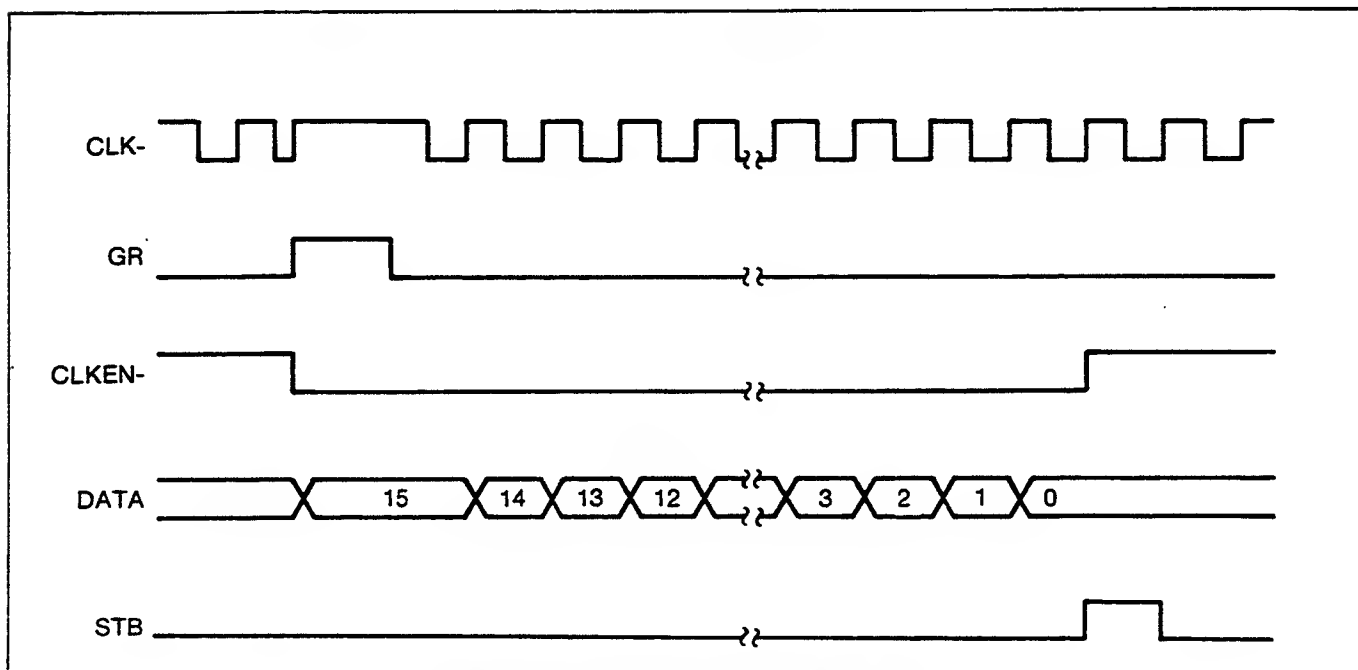


Figure 011-4. Serial Data Transfer Timing

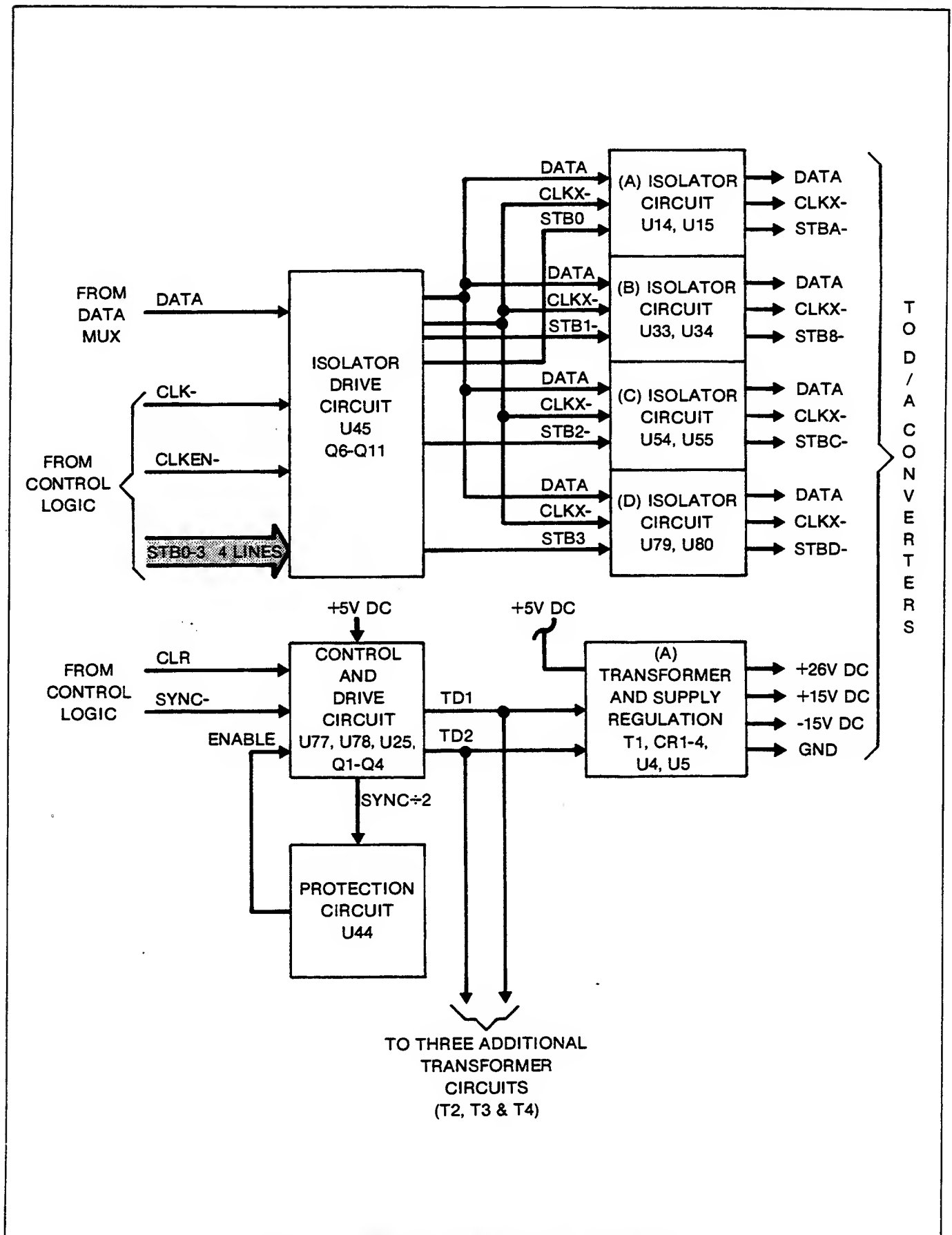


Figure 011-5. Isolation and Power Supply Block Diagram

011-9. DIGITAL-TO-ANALOG CONVERTER CIRCUIT

Refer to Figure 011-6 for a block diagram of the Digital-to-Analog Converter Circuit. Each D/A Converter Circuit contains a serial-in/parallel-out (SIPO) shift register and a 12-bit D/A converter. Serial data from the isolator circuit is clocked into the shift register by the CLKX-signal, most significant bit first. After 16 data bits have been shifted into the SIPO register, and the channel is being addressed, the STBX- signal from the isolator circuit goes to a logic 0, which latches the data into the parallel outputs of the SIPO register. When STBX- goes to a logic 1, the parallel outputs of the SIPO register are enabled, allowing the new data to propagate to the D/A converter chip.

A power-on-reset circuit resets the D/A converter circuit. On power-up of the system or on temporary interruption of the system power, the power-on-reset circuit drives the output enable signal to the serial-in/parallel-out shift register low, tri-stating its outputs. Due to pull-down resistors on the inputs of the D/A converter chip, the output of the channel is consequently set to zero volts/amps. After the system supplies have reached an acceptable level, this circuit outputs a logic 1 enable signal after new data is written to the channel, enabling the outputs of the SIPO register. The outputs remain enabled until another power interruption occurs.

A reference voltage for the D/A converter is generated from the -15V isolated power supply output. A 6.2V zener diode in the voltage reference circuit drops the voltage to -6.2V for input to a non-inverting amplifier. The amplifier output provides a nominal -10.24V reference voltage to the D/A converter, which determines the full-scale D/A converter output.

011-10. VOLTAGE MODE OPERATION

The Analog Output module is configured for voltage output operation when the jumpers are installed in the positions marked. When properly configured, the D/A converter chip's output is buffered by an inverting amplifier, then routed to an analog switch circuit. The output of the analog switch circuit then drives two unity gain, non-inverting output stages available for each channel: Voltage Out Positive (VO+) and Voltage Out Negative (VO-). If the required output is positive, the VO- output is driven to ground by grounding the input of that stage through the analog switch circuit. The VO+ output is then driven to a voltage representative of the digital data received by the D/A converter.

If a negative output is required, the VO+ output is driven to ground by grounding the input to that stage through the analog switch circuit. The VO- output is then driven to a positive voltage representative of the digital data

received. The VO+ output, in this case, would be more negative than the VO- output. The Sense (S+ and S-) inputs provide an optional means of sensing the output voltage at the load to maintain voltage accuracy.

011-11. CURRENT MODE OPERATION

The Analog Output module is configured for current mode operation when the jumpers are installed in the positions marked I. During current mode operation, the D/A converter chip's output is buffered by an inverting amplifier. The amplifier's output is loaded by a precision 4:1 resistive divider whose center point provides input to the VO+ unity-gain output stage. Due to the jumpers installed, the output stage drives a current pass transistor that controls the current flowing through the load. A 100 Ω precision resistor in the current Sense (S+) line senses the current flow and develops a voltage to be used as negative feedback for the VO+ output stage. Current for the load is supplied from the unregulated +26V dc supply for the output channel.

011-12. CALIBRATION

To obtain specified accuracy, the following calibration procedures should be performed every 90 days and whenever the mode of a channel is changed from voltage mode to current mode or from current mode to voltage mode. There are separate procedures for voltage mode and current mode; be sure to use the appropriate procedure.

Calibration service is available from Fluke Technical Service Centers if you do not choose to calibrate the 1752A-011 option yourself. See Section 4 for a list of Fluke Sales and Service Centers.

011-13. Required Equipment

The following equipment is required to calibrate a channel on the Analog Output module: a digital multimeter (DMM), an extender PCB, a 100 Ω precision resistor (Fluke Y2202), and an I/O Connector Option (Fluke Option 2400A-110 or 2400A-111).

011-14. Voltage Mode Calibration

Once you have changed a channel to voltage mode, or after 90 days of operation, calibrate each voltage output channel using the following steps:

1. Switch the 1752A power off.
2. Remove the Analog Output module. Install a PCB extender in the slot, and install the Analog Output module on the extender.
3. Switch on the 1752A power and insert the 1752A System Disk. The booting-up sequence sets all analog outputs to zero.

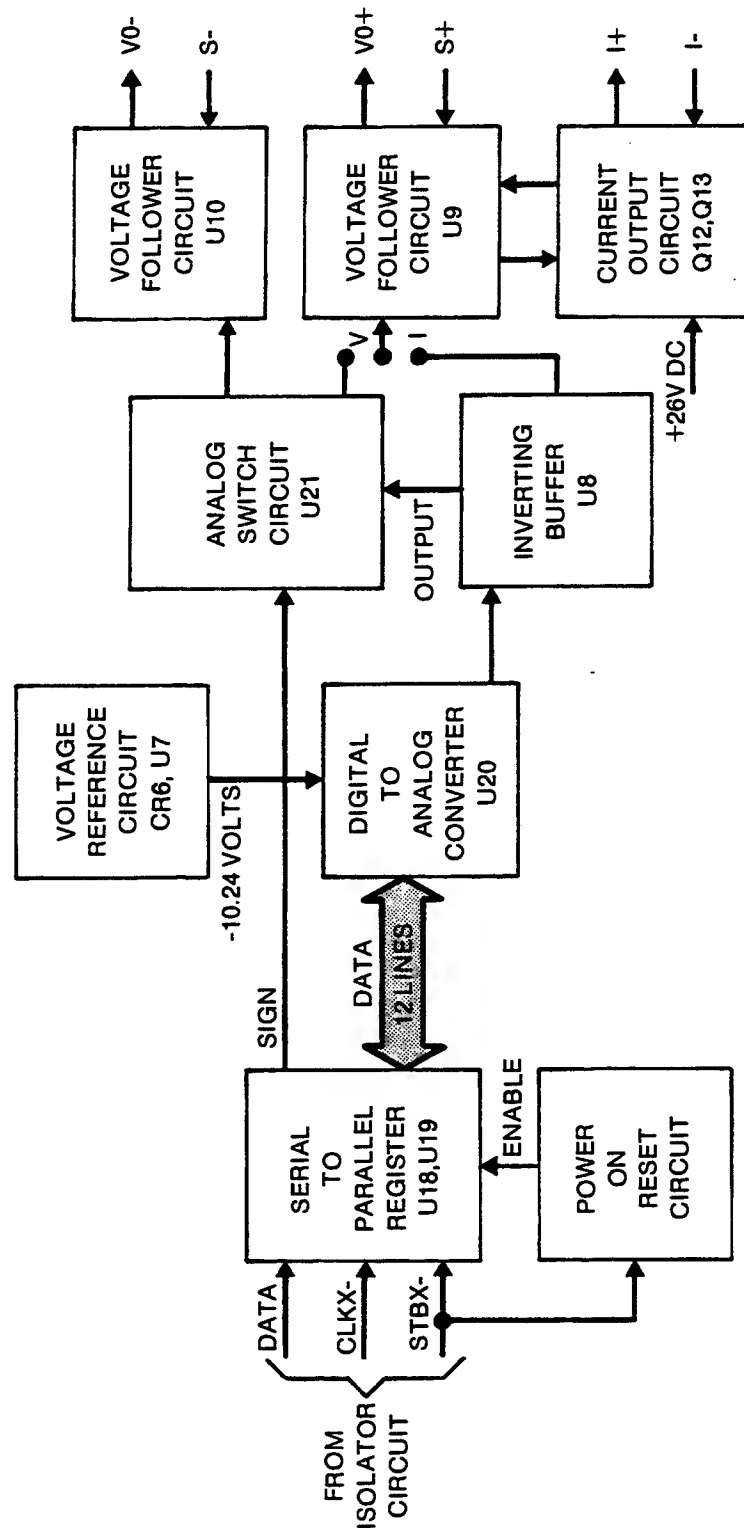


Figure 011-6. Digital-to-Analog Converter Circuit Block Diagram

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4. Allow a 20-minute warm-up period before continuing this procedure.
5. Connect the digital multimeter (DMM) input leads to the appropriate ZERO test points listed in Table 011-2 for the channel being calibrated (refer to Figure 011-7 for calibration potentiometers and test points). Adjust the corresponding ZERO potentiometer for a DMM indication of $0.00 \text{ mV} \pm 0.05 \text{ mV}$.
6. Move the DMM connections to the VO- and VO+ output pins listed in Table 011-3 for the channel being calibrated. Adjust the corre-

sponding OFFSET potentiometer for a DMM indication of $0.00 \text{ mV} \pm 0.1 \text{ mV}$.

7. From BASIC, enter the following immediate mode program steps, following each with the RETURN key, to set the channel output to 10.0V. This sample command assumes that channel 3 is being calibrated:

LINK "AIOLIB"
 AOVLTG(3%,10.0)

8. Adjust the appropriate FULL SCALE potentiometer listed in Table 011-3 to obtain a DMM indication of $10.000\text{V} \pm 0.001\text{V}$.

Table 011-2. Zero Test Points and Adjustment Potentiometers

CHANNEL	+ METER CONNECTION	-METER CONNECTION	POTENTIOMETER
A	J20, PIN 33 (TP27A)	J20, PIN 48 (TP26A)	R25
B	J20, PIN 11 (TP27B)	J20, PIN 44 (TP26B)	R49
C	J20, PIN 6 (TP27C)	J20, PIN 40 (TP26C)	R73
D	J20, PIN 34 (TP27D)	J20, PIN 36 (TP26D)	R97

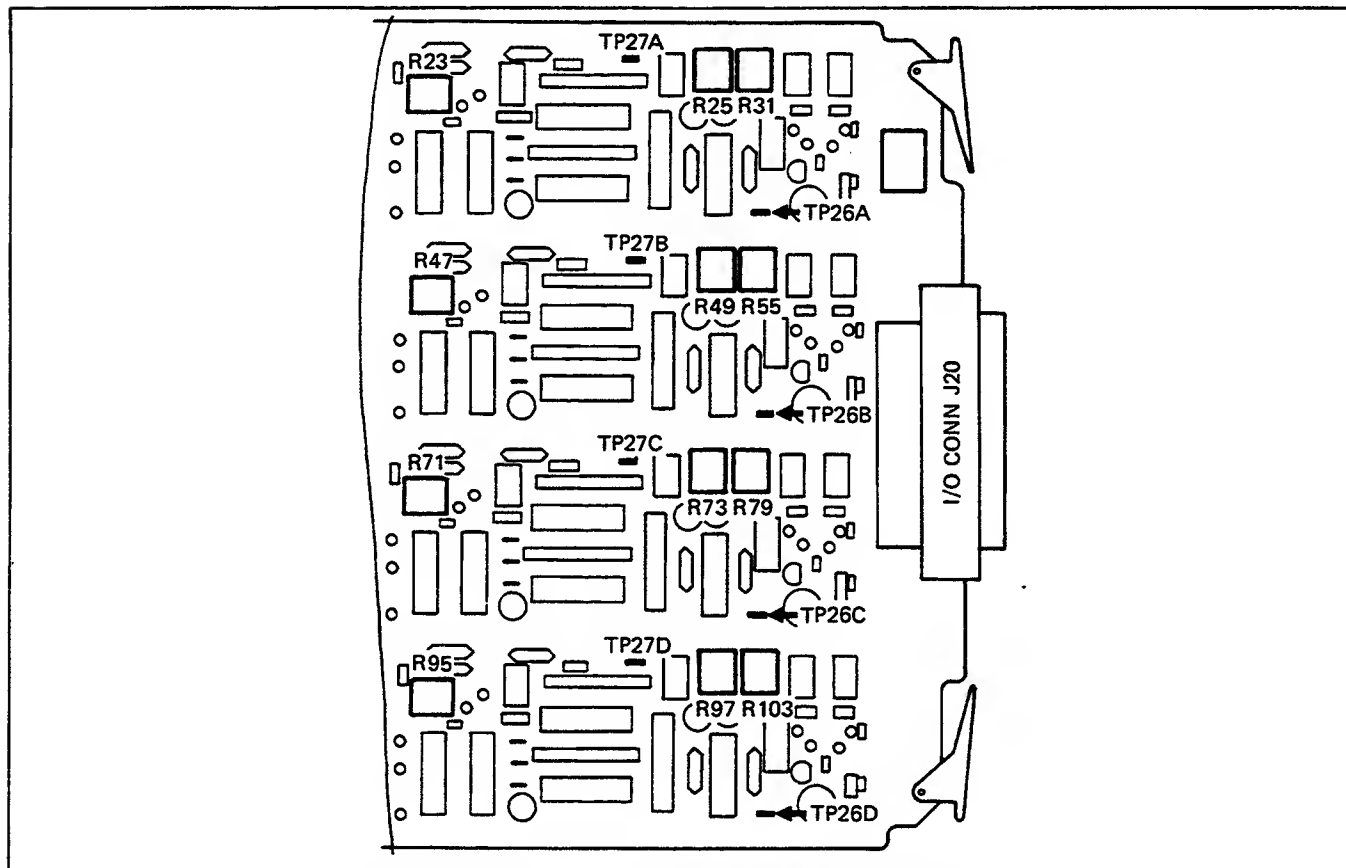


Figure 011-7. Calibration Potentiometers and Test Points

9. Enter the following step (assuming channel 3 is being calibrated), followed by the RETURN key:

AOVLTG(3%,-10.0)

10. Verify that the indication on the DMM is -10.000V, +0.001V.
11. Repeat steps 5 through 10 for the remaining voltage output channels on the assembly. If no other calibration or testing is required, return the 1752A to normal service.

011-15. Current Mode Calibration

Once you have changed a channel to current mode, or at the end of 90 days of operation, calibrate each current output channel using the following steps:

1. Switch the 1752A power off.
2. Remove the Analog Output module. Install a PCB extender in the chassis slot, and install the Analog Output module on the extender.
3. Switch the 1752A power on and insert the 1752A System Disk. The booting-up sequence resets all Analog Outputs to zero.
4. Allow a 20-minute warm-up period before continuing with this procedure.
5. Connect the DMM to the appropriate ZERO test points listed in Table 011-2 for the channel being calibrated.

6. Adjust the corresponding ZERO potentiometer to obtain a DMM indication of $0.00 \text{ mV} \pm 0.05 \text{ mV}$.

7. Select the 200 mV range on the DMM, and connect the DMM to S+ and S- terminals on the Y2022 Voltage Divider. Connect the V+ and V- terminals of the Y2022 to the appropriate I+ and I- pins for the channel being calibrated as listed in Table 011-4.

8. Assuming that the channel being calibrated is channel 3, enter the following immediate mode steps in BASIC, following each step with the RETURN key:

LINK "AIOLIB"
AOCRNT(3%,0.0)

9. Adjust the appropriate OFFSET potentiometer listed in Table 011-4 for a DMM indication of $200 \mu\text{V} \pm 100 \mu\text{V}$. The $200 \mu\text{V}$ indication corresponds to an output current of $2 \mu\text{A}$.

10. Select the 2V range on the DMM.

11. Set the output to 19 mA by entering the following immediate mode commands, followed by the RETURN key (again, assuming that the channel under test is 3):

AOCRNT(3%,0.019)

12. Adjust the FULL SCALE potentiometer for the channel being calibrated for a DMM indication of $1.9\text{V} \pm 0.0001\text{V}$. The 1.9V indication corresponds to 19 mA current output.

Table 011-3. Voltage Test Points and Potentiometers

CHANNEL	POTENTIOMETER		OUTPUT CONNECTIONS
	OFFSET	FULL SCALE	
A	R31	R23	J20, PIN 49 (VO-) : J20, PIN 50 (VO+)
B	R55	R47	J20, PIN 13 (VO-) : J20, PIN 12 (VO+)
C	R79	R71	J20, PIN 8 (VO-) : J20, PIN 7 (VO+)
D	R103	R95	J20, PIN 2 (VO-) : J20, PIN 1 (VO+)

Table 011-4. Current Test Points and Potentiometers

CHANNEL	POTENTIOMETER		OUTPUT CONNECTIONS
	OFFSET	FULL SCALE	
A	R31	R23	J20, PIN 16 (I-) : J20, PIN 17 (I+)
B	R55	R47	J20, PIN 27 (I-) : J20, PIN 10 (I+)
C	R79	R71	J20, PIN 22 (I-) : J20, PIN 5 (I+)
D	R103	R95	J20, PIN 20 (I-) : J20, PIN 35 (I+)

13. Repeat steps 5 through 12 for the remaining current output channels on the assembly. If no other calibration or testing is to be performed, return the 1752A to normal service.

011-16. MAINTENANCE

WARNING

THE 1752A CONTAINS LETHAL VOLTAGES. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE 1752A. TURN OFF THE INSTRUMENT AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

The following paragraphs describe maintenance procedures for the Analog Output module. These procedures include hardware setup, performance testing, and troubleshooting.

011-17. Hardware Setup

If the Analog Output module is ordered at the same time as the 1752A mainframe, the module is installed in the instrument chassis at the factory. If the Analog Output module is ordered at a later time, the board address and the configuration of each output channel must be checked and changed if necessary. To install or remove a board, see the instructions in Section 3. To change or check the settings on a board that is not installed, follow the instructions in the following paragraphs.

011-18. Board Address Selection

You can build a system with up to 32 boards, assigning a board address to each module. The 1752A-011 has four addressable output channels, labeled consecutively from 0 to 127. The board addresses correspond to the channel numbers as follows:

Board address 0 = output channels 0 through 3
Board address 1 = output channels 4 through 7
Board address 2 = output channels 8 through 11

Board address 29 = output channels 116 through 119
Board address 30 = output channels 120 through 123
Board address 31 = output channels 124 through 127

The address is assigned by setting the Address Switch on the module. Figure 011-8 shows the location and switch positions of the Address Switch. Normally, assign board address 0 to the first Analog Output module in the system, and address 1 to the second Analog Output module. The switch settings for each board address are shown in Table 011-5.

011-19. Voltage/Current Configuration

Unless specified otherwise, all four channels of the Analog Output module are configured as voltage outputs when shipped from the factory. Normally, a channel is reconfigured by Fluke service personnel, however, with access to the required equipment, you can reconfigure the board yourself.

To determine the configuration of each channel, examine the assembly. Looking at the component side of the printed circuit board, locate the jumpers. (See Figure 011-9.) Compare jumper locations to the detailed sections of the figure to identify the proper channel configuration.

Move the jumpers to match those in Figure 011-9. Once the output configuration of a channel is changed (from voltage to current or current to voltage), the channel must be recalibrated to obtain the 0.1% accuracy listed in the specifications. See the paragraphs on Calibration for more information.

011-20. Performance Tests

The System Diagnostic software contains Analog Output Loopback Tests to thoroughly verify the operation of any Analog Output channel. To run these tests requires that the 1752A be configured with an Analog Measurement Processor (Option 1752A-010).

Customers who do not have an Analog Measurement Processor should follow the additional performance test procedure presented in this paragraph. The procedure is divided into two parts: the voltage mode performance test and the current mode performance test. You should match the procedure to the configuration of the channel under test.

The following equipment is required to complete the performance test: a Fluke 8840 Digital Multimeter (or equivalent), the 1752A System Diagnostic Disk, and a 2400A-110 Screw Terminal Connector, or 2400A-111 Solder Pin Connector.

011-21. VOLTAGE MODE PERFORMANCE TEST

Perform the following procedure to test the performance of any Analog Output channel configured in voltage mode.

1. Switch the 1752A power off.
2. Connect either a Screw Terminal connector (2400A-110) or a Solder Pin connector (2400A-111) to the Analog Output option.
3. Connect the high (+) input of the Digital Multimeter (DMM) to the corresponding +

- Voltage Output connector pin of the channel under test. Refer to Table 011-6 for connector pinouts.
4. Connect the low (-) input of the DMM to the corresponding Low Voltage Output connector pin of the channel under test.
 5. Insert the System Diagnostic Disk into the 1752A and switch the power on.
 6. After the System Diagnostic Software has loaded, verify that the DMM indicates a $0.0V \pm 0.005V$ DC reading.
 7. Run DATST under the Analog Output subtest menu. Refer to Section 3 of this manual for information on DATST.
 8. While DATST is running, increment or decrement the channel addressed by the program to match the channel under test.
 9. Press the VOLTAGE and CONSTANT OUTPUT menu buttons.
 10. Using the calculator keypad presented on the 1752A screen, output 10.0V and verify that the DMM has a $10.0V \pm 0.005V$ DC reading.
 11. Repeat step 9.
 12. Using the calculator keypad presented on the 1752A screen, output -10.0V and verify that the DMM has a $-10.0V \pm 0.005V$ DC reading.

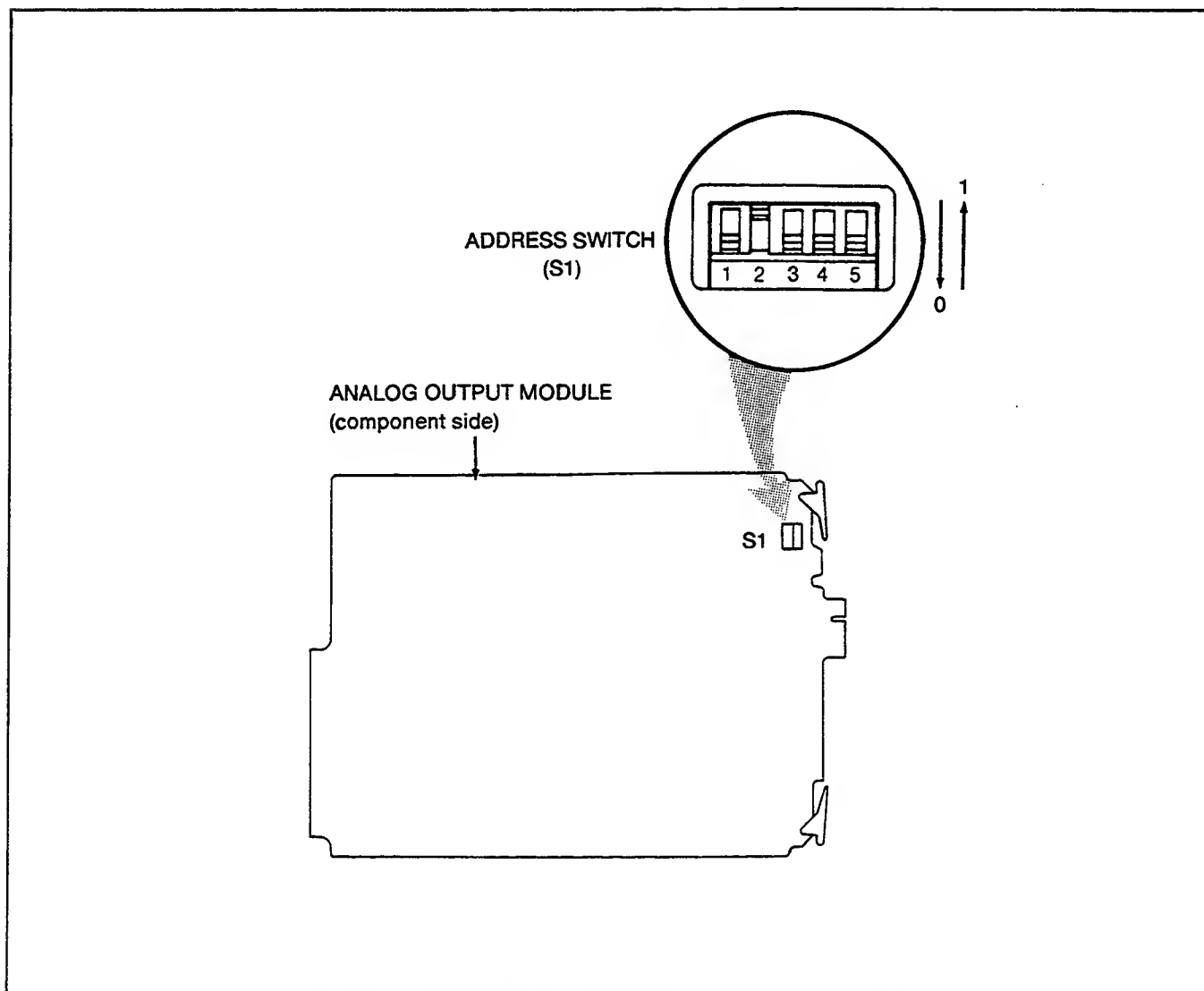


Figure 011-8. Board Address Switch Location and Settings

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Table 011-5. Current/Voltage Analog Output Switch Settings

S1 SWITCH SETTING = X X X X X LEFT = ONE, RIGHT = ZERO									
Card Number	Switch Segments					Analog Output channels (A, B, C, D) assigned:			
	B5	B4	B3	B2	B1	A	B	C	D
0	0	0	0	0	0	0	1	2	3
1	0	0	0	0	1	4	5	6	7
2	0	0	0	1	0	8	9	10	11
3	0	0	0	1	1	12	13	14	15
4	0	0	1	0	0	16	17	18	19
5	0	0	1	0	1	20	21	22	23
6	0	0	1	1	0	24	25	26	27
7	0	0	1	1	1	28	29	30	31
8	0	1	0	0	0	32	33	34	35
9	0	1	0	0	1	36	37	38	39
10	0	1	0	1	0	40	41	42	43
11	0	1	0	1	1	44	45	46	47
12	0	1	1	0	0	48	49	50	51
13	0	1	1	0	1	52	53	54	55
14	0	1	1	1	0	56	57	58	59
15	0	1	1	1	1	60	61	62	63
16	1	0	0	0	0	64	65	66	67
17	1	0	0	0	1	68	69	70	71
18	1	0	0	1	0	72	73	74	75
19	1	0	0	1	1	76	77	78	79
20	1	0	1	0	0	80	81	82	83
21	1	0	1	0	1	84	85	86	87
22	1	0	1	1	0	88	89	90	91
23	1	0	1	1	1	92	93	94	95
24	1	1	0	0	0	96	97	98	99
25	1	1	0	0	1	100	101	102	103
26	1	1	0	1	0	104	105	106	107
27	1	1	0	1	1	108	109	110	111
28	1	1	1	0	0	112	113	114	115
29	1	1	1	0	1	116	117	118	119
30	1	1	1	1	0	120	121	122	123
31	1	1	1	1	1	124	125	126	127

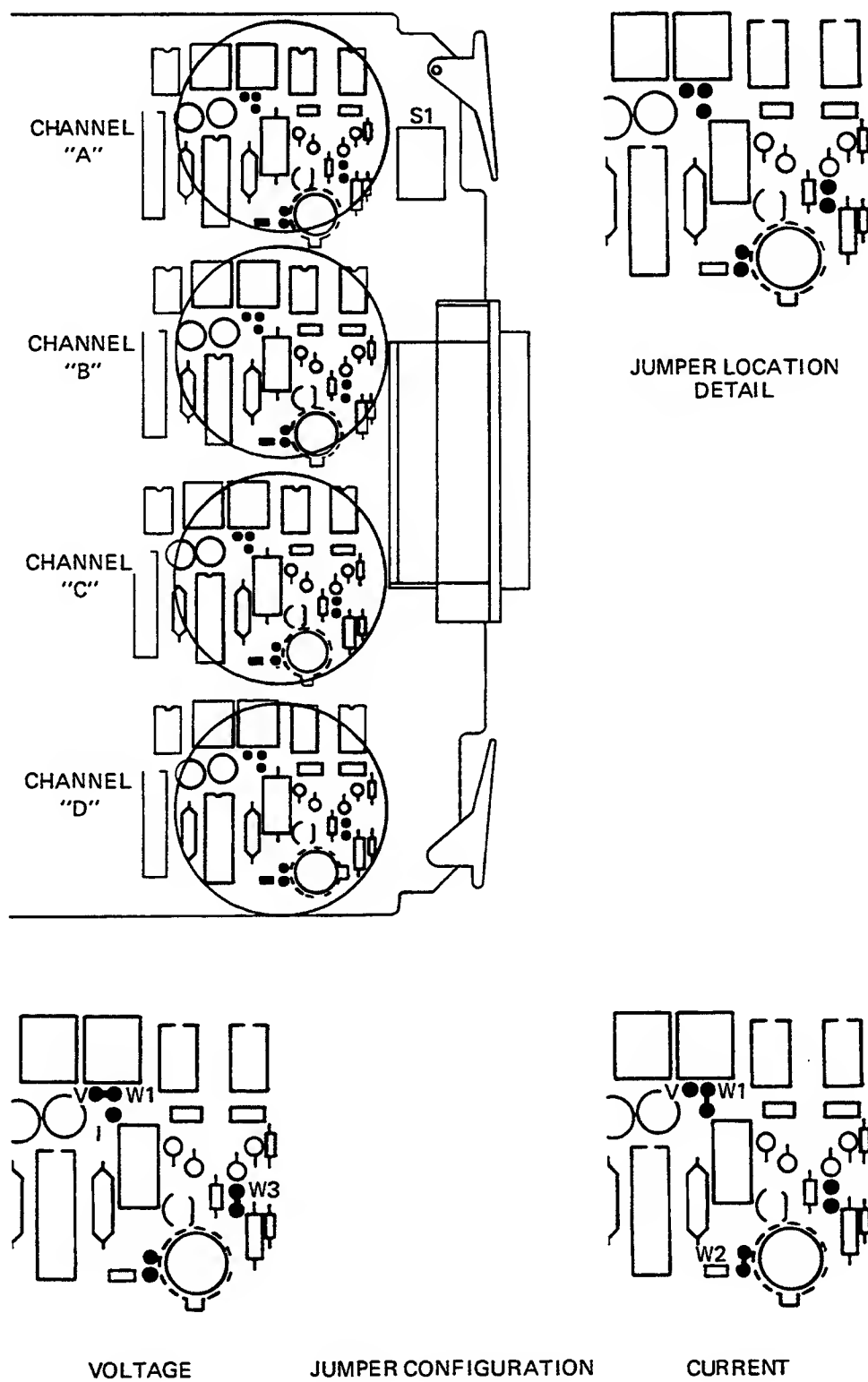


Figure 011-9. Output Jumper Locations

OPTION 1752A-011
ANALOG OUTPUT MODULE

Table 011-6. Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
50	+ Voltage Output A	22	- Current Output C
49	- Voltage Output A	40	Test Point 26C
32	+ Voltage Sense A	41	Test Point 26C
31	- Voltage Sense A	6	Test Point 27C
17	+ Current Output A	9	Not Used
16	- Current Output A	1	+ Voltage Output D
47	Test Point 26A	2	- Voltage Output D
48	Test Point 26A	19	- Voltage Sense D
33	Test Point 27A	18	- Voltage Sense D
3	Not Used	35	+ Current Output D
12	+ Voltage Output B	20	- Current Output D
13	- Voltage Output B	36	Test Point 26D
28	+ Voltage Sense B	37	Test Point 26D
29	- Voltage Sense B	34	Test Point 27D
10	+ Current Output B	14	Not Used
27	- Current Output B	15	Not Used
44	Test Point 26B	21	Not Used
45	Test Point 26B	25	Not Used
11	Test Point 27B	26	Not Used
4	Not Used	30	Not Used
7	+ Voltage Output C	38	Not Used
8	- Voltage Output C	39	Not Used
23	- Voltage Sense C	42	Not Used
24	- Voltage Sense C	43	Not Used
5	- Current Output C	46	Not Used

011-22. CURRENT MODE PERFORMANCE TEST

Perform the following procedure to test the performance of any Analog Output channel configured in current mode.

1. Switch the 1752A power off.
2. Connect either a Screw Terminal connector (2400A-110) or a Solder Pin connector (2400A-111) to the Analog Output option.
3. Set-up the Digital Multimeter (DMM) to measure current.
4. Connect the high (+) input of the DMM to the corresponding + Current Output connector pin of the channel under test. Refer to Table 011-6 for connector pinouts.
5. Connect the common (-) input of the DMM to the corresponding - Current Output connector pin of the channel under test.
6. Insert the 1752A System Diagnostic Disk into the 1752A and switch the power on.

7. After the System Diagnostic Software has loaded, verify that the DMM indicates a $5\ \mu\text{A} \pm 2.5\ \mu\text{A}$ reading.
8. Run DATST under the Analog Output subtest menu. Refer to Section 3 of this manual for information on DATST.
9. While DATST is running, increment or decrement the channel being addressed by the program to match the channel under test.
10. Press the CURRENT and CONSTANT OUTPUT menu buttons.
11. Using the calculator keypad on the test menu, output 20.0 mA and verify that the DMM has a $20\ \text{mA} \pm 20\ \mu\text{A}$ reading.

011-23. Troubleshooting

System Diagnostic software is provided with the 1752A to aid in identifying faulty modules. The software contains subtests for specific functions of the -011 option. The System Diagnostic consists of a Register R/W Test, Voltage and Current Loopback Tests for Channels 0 through 3, and DATST. For more information on the System Diagnostic tests, see Section 3.

If an error is encountered by the System Diagnostic during the execution of a test, an entry is made in an error log. IF STOP ON FAIL was selected from the Main Menu, an error message will be displayed on the screen. On an error condition, first verify that the module is faulty and then replace it. (If the System Diagnostic will not load and run, see Section 3, Troubleshooting.)

If the ports or board are failed by System Diagnostic Software, the following troubleshooting procedures may be used to isolate the failure. Due to the great number of possible problems, only the most common problems encountered by factory technicians are discussed. If the problem encountered is not discussed in this section, contact the nearest Fluke Sales and Service Center. (See Section 4.)

Component-level troubleshooting is recommended only when it is not possible to replace a defective module. If you attempt to repair a module, you will need, at a minimum, the following equipment: a multi-trace oscilloscope, a $5\frac{1}{2}$ digit multimeter, a logic probe and a quantity of replacement components. Most chips are soldered into the circuit board, so it will be necessary to unsolder components in order to swap them.

The component-level troubleshooting information that follows is divided into four major sections. Each section

describes a common symptom that may be exhibited by your 1752A. Each section is further divided into lists of possible cause(s) and suggested action(s). Suggested actions are presented in the order that they should be performed, and each action is dependent on the previous step. To use the troubleshooting information, you should first locate the applicable symptom, read the list of possible causes, and perform each action in the order presented, without skipping any steps.

CAUTION

Extreme care should be used when removing and replacing components to avoid irreparable damage to the printed circuit boards.

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

SYMPTOM 1:

System Diagnostic software returns the error message: Option is faulty, missing or improperly configured. Or, while running a BASIC program, the following error is returned: analog output channel is not installed.

POSSIBLE CAUSE:

- Address decode logic is faulty.

ACTIONS:

- Verify that the address switches are set correctly for the board address being tested. Refer to paragraph 011-18 for correct address switch settings.
- Run the System Diagnostic Register R/W Test in Loop Mode. Verify that TP60 toggles high. If logic activity is not present, the error is most likely due to the malfunctioning of one or more of the following: U62, U63, U64, U74, U75, or U76.
- Remove all options in the 1752A. While running the Register R/W Test in Loop Mode, check that the Q5 collector pulses low. If logic activity is not present, replace Q5.

SYMPTOM 2:

A channel configured for voltage mode operation is inaccurate.

POSSIBLE CAUSES:

- The channel is configured improperly.
- The channel is out of calibration.

OPTION 1752A-011
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- The channel's +15V or -15V power supply is faulty.
- The channel's interface bus data register is faulty.
- The channel's isolator circuit is malfunctioning.
- The channel's digital-to-analog converter circuitry is faulty.

ACTIONS:

- Verify that the channel is configured properly. Refer to paragraph 011-19 for configuration procedures.
- Calibrate the channel under test. Refer to the earlier paragraphs on calibration for voltage mode calibration procedures.
- Measure the channel's +15V and -15V supplies and verify that each supply voltage reading is $\pm 0.6V$ of the corresponding nominal value.

If the +15V supply is out of tolerance, measure the positive voltage regulator input. For example, if troubleshooting channel A, measure the input to U4, pin 1. If the regulator input measures approximately 26V dc or more, replace the regulator. Otherwise, the problem lies in the power supply drive circuitry (Q1, Q2, Q3, Q4, U25, U77, U78, U44).

If the -15V supply is out of tolerance, measure the negative voltage regulator input. For example, if troubleshooting channel B, measure the input to U27, pin 1. If the input measures approximately -26V dc or less, replace the regulator. Otherwise, the problem lies in the power supply drive circuitry (Q1, Q2, Q3, Q4, U25, U77, U78, U44).

- Run the Register R/W Test under the Analog Output Subtest menu. If the test fails, the bus interface logic is faulty. See Symptom 4 for more troubleshooting information.
- While running the Register R/W Test in Loop Mode, verify logic activity on the DATA, CLK and Strobe lines on the isolated side of the test channel. For example, if troubleshooting channel C, verify logic activity on TP23C, TP24C, and TP25C. Lack of activity is most likely due to a malfunction of the opto-isolators for the channel under test (U54 or U55 for channel C). Failure could also be due to a malfunction in the control logic (U3, U13, U24, U45, U46, U65, U66, U76, or U77) or the data multiplexers (U1, U2).

- Run DATST under the Analog Output Subtest menu. Output 0.0V and verify that pins 4 through 15 of the digital-to-analog converter are at a TTL low for the channel under test. For example, if testing Channel A, verify that pins 4 through 15 are low at U20.

While running DATST, output 10.2375V and verify that pins 4 through 15 of the digital-to-analog converter are at a TTL high for the channel under test.

Failure of either test could be due to the malfunction of the serial to parallel shift registers for the channel under test (U18 or U19 for channel A).

- While running DATST, output 10.2375V and measure the voltage on pin 18 of the digital-to-analog converter for the channel under test. For example, test point TP27B for channel B. Verify that the pin's voltage reads $10.2375V \pm 5\text{ mV}$. Failure could be caused by the malfunctioning of the following: the digital-to-analog inverting buffer, the digital-to-analog chip, or the voltage reference circuit for the channel under test (U30, U39 or U29 for channel B).
- If the option passes all the above procedures, the malfunction is most likely due to faulty output buffers or the failure of the analog switch for the channel under test. (U9, U10 or U21 for channel A).

SYMPTOM 3:

A channel configured for current mode operation is inaccurate.

POSSIBLE CAUSES:

- The channel is configured improperly.
- The channel is out of calibration.
- The channel's +15V or -15V power supply is faulty.
- The channel's interface bus data register is faulty.
- The channel's isolator circuit is malfunctioning.
- The channel's digital-to-analog converter circuitry is faulty.

ACTIONS:

- Verify that the channel is configured properly. Refer to paragraph 011-19 for configuration procedures.

- Calibrate the channel under test. Refer to the earlier paragraphs on calibration for current mode calibration procedures.
- Measure the channel's +15V and -15V supplies and verify that each supply voltage reading is $\pm 0.6V$ of the corresponding nominal value.

If the +15V supply is out of tolerance, measure the positive voltage regulator input. For example, if troubleshooting channel A, measure the input to U4, pin 1. If the input measures approximately 26V dc or more, replace the regulator. Otherwise, the problem lies in the power supply drive circuitry (Q1, Q2, Q3, Q4, U25, U77, U78, U44).

If the -15V supply is out of tolerance, measure the negative voltage regulator input. For example, if troubleshooting channel B, measure the input to U27, pin 1. If the input measures approximately -26V dc or less, replace it. Otherwise, the problem lies in the power supply drive circuitry (Q1, Q2, Q3, Q4, U25, U77, U78, U44).

- Run the Register R/W Test under the Analog Output Subtest menu. If the board fails the test, the bus interface logic is faulty. See Symptom 4 for more troubleshooting information.
- While running the Register R/W test, verify logic activity on the DATA, CLK and Strobe lines on the isolated side of the test channel. For example, if troubleshooting channel C, verify activity on TP23C, TP24C, and TP25C. Lack of activity is most likely due to a malfunction in the opto-isolators for the channel under test (U54 or U55 for channel C). Failure could also be due to a malfunction in the control logic (U3, U13, U24, U45, U46, U65, U66, U76, or U77) or the data multiplexers (U1, U2).
- Run DATST under the Analog Output Subtest menu. Output 0 mA and verify that pins 4 through 15 of the digital-to-analog converter are at a TTL low for the channel under test. For example, while testing channel A, verify that pins 4 through 15 of U20 are at a TTL low.

While running DATST, output 20.475 mA and verify that pins 4 through 15 of the digital-to-analog converter are at a TTL high for the channel under test.

Failure of either test could be due to the malfunction of the serial to parallel shift registers for the channel under test (U18 or U19 for channel A).

- While running DATST, output 20.475 mA and measure the voltage at pin 18 of the digital-to-analog converter for the channel under test (TP27B for channel B). Verify that the voltage reads $10.2375V \pm 5 \text{ mV}$. Failure could be due to the malfunctioning of the following: the digital-to-analog inverting buffer, the digital-to-analog chip, or the voltage reference circuit for the channel under test (U30, U39, or U29 for channel B).
- If the option passes all the above procedures, the malfunction is most likely due to a faulty VO+ output buffer or the current sensing circuit for the channel under test (U9, Q12, or Q13 and the associated circuitry for channel A).

SYMPTOM 4:

Option fails the System Diagnostic's Register R/ W test.

POSSIBLE CAUSES:

- Bus data transceivers U41 or U42 are faulty.
- Control logic U43, U46, U65, U66, U76, or U77 is malfunctioning.
- Data registers U11, U12, U22, or U23 are faulty.

ACTIONS:

- Run the Register R/ W test and note the failure.
- If the System Diagnostic test reports that a couple of data bits are bad for all four channels, the fault is most likely due to a malfunction in the data bus transceivers (U41 or U42). Locate the transceiver associated with the bad bit(s) and replace it. U41 drives data bits 8-15 and U42 drives data bits 0-7.

The fault could also be due to the malfunctioning of the data register associated with the bad data bit(s).

- If the System Diagnostic test reports that all of the data bits are bad for all four channels, the fault is most likely due to a malfunction in the control logic (U43, U46, U65, U66, U76, or U77). Run the Register R/ W Test in Loop Mode and verify logic activity on TP64, TP65, TP66, and TP67 and replace any malfunctioning chips.

Option 1752A-012 Counter/Totalizer

012-1. INTRODUCTION

The 1752A-012 Counter/Totalizer is a plug-in module that measures frequency or time, or totalizes with a gateable bidirectional totalizer. The different modes of operation are selected under software control.

The Counter/Totalizer provides the following inputs: two frequency and time measurement inputs, two gating inputs, one trigger input, and four totalizer inputs. All of the measurement inputs may include switch closures or logic levels except the analog input for frequency and time measurement; these inputs are not isolated from the 1752A or ground. The analog input for frequency and time measurement may be a periodic analog signal; this input is isolated from the 1752A and ground.

The Counter/Totalizer also provides an output, which indicates an overflow condition. This output is a logic level and is not isolated from the 1752A or ground.

Several features of the Counter/Totalizer module provide for system synchronization. These features include:

external triggering, single versus continuous measurement cycling, pre-settable bidirectional two-quadrant gateable totalizing, logic-level gating, start-stop gating, and start-stop time measurement.

The Counter/Totalizer mounts in option slots 4 or 5 in the 1752A chassis. The 12-contact, screw-terminal connector attached to the module connects to all nine inputs, one output, an isolated common, and a non-isolated common. Specifications for the Counter/Totalizer option are presented in Section 1.

NOTE

For additional details regarding external input connections, input timing requirements, and input signal logic levels, refer to the 1752A Data Acquisition and Control Manual, Section 5.

012-2. SPECIFICATIONS

See Table 012-1 for Counter/Totalizer specifications.

Table 012-1. Counter/Totalizer Specifications

SYSTEM CAPACITY	1 Counter/Totalizer Module (1 Channel) per 1752A, maximum 32 Counter/Totalizer Modules (32 Channels) with 1702A.
NONISOLATED INPUTS	TTL Input, Gate 1, Gate 2, Trigger, <u>Count Up</u> , <u>Count Down</u> , Up / <u>Down</u> , <u>Count</u> , Common (Nonisolated).
ISOLATED INPUTS	Analog Input and Common (Isolated). These inputs are isolated in common from the 1752A and/or ground, up to 30V and 1.0 volt/microsecond maximum slew rate.

Table 012-1. Counter/Totalizer Specifications (cont)

INPUT LOGIC

Nonisolated Inputs Pull-up resistors are installed to allow contact closures and logic levels as inputs.

Isolated Inputs (Analog Input) Any periodic analog signal that satisfies signal level, frequency, duty cycle, and isolation requirements is allowed.

LOGIC LEVELS All nonisolated inputs are low power Schottky inputs with static protection and a minimum of 400 mV of hysteresis. 0V to 0.5V for input low, 2.0V to 7V for input high.

OVERFLOW OUTPUT

Output Isolation The Overflow output is not isolated from the 1752A or ground.

Output Circuitry Open - collector TTL output.

Maximum Sink Current 40 mA.

Output Voltage

AT 40 mA SINK CURRENT 0.7V max

AT 16 mA SINK CURRENT 0.4V max

Maximum OFF-State Voltage 30V

TTL Compatibility The output can drive up to six standard TTL loads or up to twelve low-power Schottky loads. An external pull-up resistor is not required.

FREQUENCY MEASUREMENTS

Inputs TTL Input, Analog Input, Trigger

Range

NONISOLATED INPUT 0 to 900 kHz

ISOLATED INPUT 10 Hz to 200 kHz

Gate Times

1 3.277 ms

2 26.21 ms

3 209.7 ms

4 3.355 sec

Resolution

1 305.2 Hz

2 38.15 Hz

3 4.768 Hz

4 0.2980 Hz

Accuracy ± 1 count $\pm .005\%$ of resolution (timebase accuracy)

TIME MEASUREMENTS

Inputs TTL Input, Analog Input, Gate 1, Gate 2, Trigger

Range

NONISOLATED INPUT

Fast Rate 1.2 μ s to 6.7s (all)

Slow Rate 819 μ s to 3.82 hr (G1, G2 only)

ISOLATED INPUT 2.5 μ s to 50 ms pulse width or 5 μ s to 100ms period

Table 012-1. Counter/Totalizer Specifications (cont)

Frequency Counted

FAST RATE 2.5 MHz (all)
SLOW RATE 1.221 kHz (G1, G2 only)

Resolution

FAST RATE 400 ns (all)
SLOW RATE 819 μ s (G1, G2 only)

Accuracy ± 1 count $\pm .005\%$ of reading (timebase accuracy)
 \pm trigger error of signal on isolated input

TOTALIZE

Count Inputs Count Up, Count Down, Count, Up / Down

Gate Inputs Gate 1, Gate 2

Range DC to 900 kHz

Capacity -8,388,608 to +8,388,607

ANALOG INPUT SENSITIVITY

Sinewave

10 Hz to 100 kHz 50 mV rms
100 kHz to 200 kHz 100 mV rms

Pulse 150 mV with minimum pulse width of 2.5 μ s. 5% < duty cycle < 95%.

ANALOG INPUT IMPEDANCE

Nonlimiting 10 megohm, ≤ 50 pF

Limiting 1.2 megohm in parallel with 47 pF

TIMEBASE

Frequency 10.000 MHz

Accuracy ± 50 ppm

NONISOLATED INPUT TIMING See timing diagram

Trigger Input

TRIGGERABLE MODES Frequency, Time

PULSE WIDTH (Tpw) 100 ns min.

Input Debouncing

INDIVIDUALLY

DEBOUNCEABLE INPUTS

(SWITCH SELECTABLE) Count, Count Up, Count Down, Gate 1, Gate 2

INPUT PULSE WIDTH TO

CHANGE STATE (Tip) 15 ms min.

BOUNCE PULSE WIDTH (Tbp) . 10 ms max.

Measurement Input Timing

(All Debouncers Off)

APPLICABLE INPUTS TTL Input, Gate 1, Gate 2, Count, Count Up, Count Down, Trigger

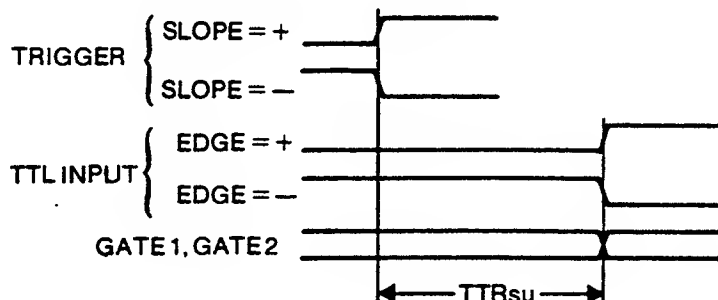
INPUT PULSE WIDTH

EXCEPT TRIGGER (Tpw) 500 ns min.

Table 012-1. Counter/Totalizer Specifications (cont)

TRIGGER SET-UP TIME IN TIME MODES (TTRsu)	1.0 μ s minimum to guarantee that the period or time interval immediately following the trigger is the one measured.
GATE 1- TO -GATE 2 OR GATE 2- TO -GATE 1 SEPARATION (TGGsep)	500 ns minimum to guarantee that the positive edge of one input is recognized as occurring before the other.
GATE TO COUNT OR COUNT TO GATE SEPARATION (TGCsep)	1.0 μ s minimum to guarantee that count pulses are totalized after the gate enables the totalizer and not before, and that count pulses are totalized before the gate disables the totalizer and not after.
UP/DOWN INPUT STABLE SET-UP (TDsu)	0 ns minimum prior to Count.
UP/DOWN INPUT STABLE HOLD (TDhid)	1.0 μ s minimum after Count.
POWER CONSUMPTION	12 watts typical per PCB assembly added to the system.
WEIGHT	0.4 kg (1.0 lb)

TTRsu = Trigger Set-up Time



Tpw = Input Pulse Width

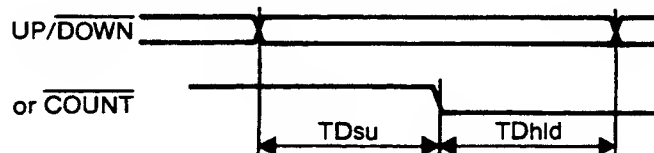


TGGsep = Gate to Gate Separation



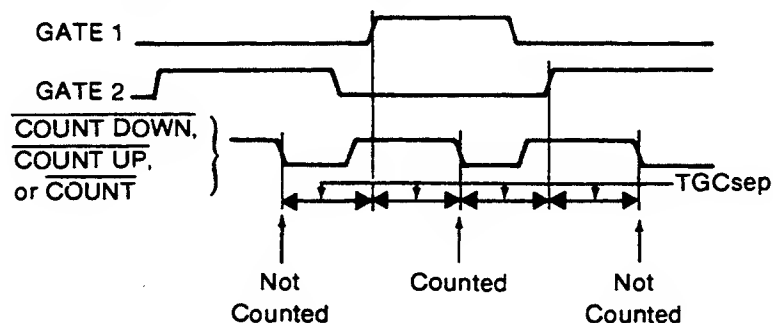
Table 012-1. Counter/Totalizer Specifications (cont)

T_{Dsu} = Up/Down Set-up Time
 T_{Dhd} = Up/Down Hold Time

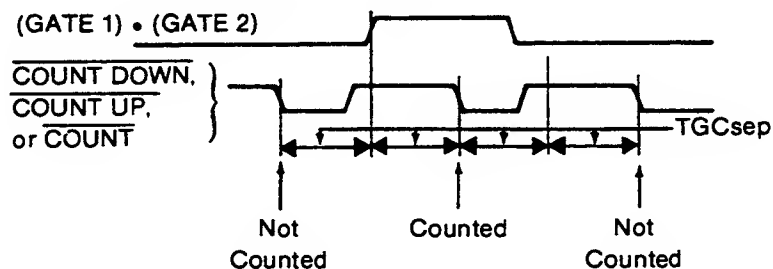


T_{GCsep} = Gate to Count/Count to Gate Separation

Case 1 : GATE = G1 TO G2



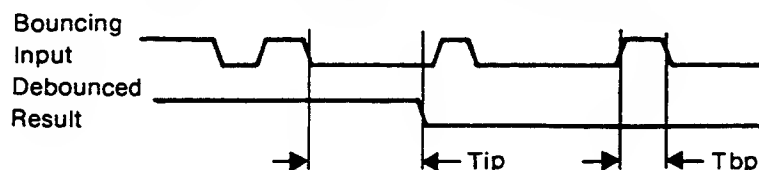
Case 2 : GATE = G1 AND G2



T_{bp} = Bounce Pulse Width

T_{ip} = Change State Pulse Width

(shown for a high-to-low input transition, invert signals for corresponding low-to-high timing).



012-3. THEORY OF OPERATION

012-4. Introduction

This section presents a functional and circuit description of the 1752A-012 Counter/Totalizer. The descriptions are supported by Figure 012-1 and the schematic diagrams in Section 5.

012-5. Functional Description

The Counter/Totalizer operates in any one of three basic modes under direction of the 1752A Single Board Computer. The operating modes are: Totalizing, Time Measurement and Frequency Measurement. The following paragraphs describe each of these modes.

012-6. Totalizing Mode

When totalizing, the control signal (STORE) is constantly asserted high, commanding the storage logic to store the contents of the counter chain in the measurement storage register. The counter chain contains the totalizer value and counts in the direction determined by the up/down count resolver when enabled by the counter-enable multiplexer. If the counter chain overflows or underflows during operation, the OVERFLOW- output is driven low and an overflow status is returned to the user.

The counter enable multiplexer enables the counter chain whenever the up/down count resolver asserts the CET1- signal low and the input multiplexer is gating the totalizer on. (CET3- is asserted low.) The up/down count resolver asserts CET1- low for one clock cycle to allow the counter chain to increment or decrement one count if it receives a logic high level on either the UP COUNT or DOWN COUNT signals. UP COUNT is asserted high when the COUNT UP- input is pulled low, or when the COUNT- input is pulled low and UP/DOWN- is pulled high. DOWN COUNT is asserted high when the COUNT DOWN- input is pulled low, or when the COUNT- input is pulled low and UP/DOWN- is pulled low.

012-7. TOTALIZER GATING

The input multiplexer asserts CET3- low to gate the totalizer on and allow the counter chain to totalize inputs (see Totalizing Mode). Assertion of the CET3- signal by the input multiplexer is dependent on the mode of totalizer gating as described in the following paragraphs.

If external gating is disabled by the user, the input multiplexer asserts CET3- low continuously, regardless of the GATE 1 and GATE 2 inputs.

If GATE 1 -to- GATE 2 totalizer gating is selected, the input multiplexer uses the output of the start-stop state

machine as the totalizer gating signal (CET3-). The start-stop state machine uses the GATE 1 as the start input and GATE 2 as the stop input.

If GATE 1 -AND- GATE 2 totalizer gating is selected, the input multiplexer uses the logical AND of GATE 1 and GATE 2 as the totalizer gating signal. If GATE 1 and GATE 2 are both high, CET3- is asserted low; otherwise CET3- is high.

012-8. Time Measurement Mode

The Counter/Totalizer can make time measurements using a fast rate clock (freq = 2.5 MHz) for time intervals up to 6.7 seconds or a slow rate clock (freq = 1.22 kHz) for time intervals up to 3.82 hours. Slow rate measurements can be made on the GATE 1 and GATE 2 inputs only. Both measurement types are described in the following paragraphs.

012-9. FAST RATE TIME MEASUREMENTS

When making fast rate time measurements, the counter enable multiplexer uses the CET2- output of the mode-control logic as the enabling signal for the counter chain. When the mode-control logic asserts CET2- low, the counter chain is enabled. During this time, the counter chain is incremented by the 2.5 MHz on-board clock, or every 400 nsec. When the mode-control logic sets CET2- high, the counter enable multiplexer disables the counter. The count in the counter chain is proportional to the measured time interval (measured time = 400 nsec x number of counts).

The mode-control logic controls the time interval measurement through its output CET2-. The input to the mode-control logic is provided by the input multiplexer, which selects any one of the following inputs: the TTL input, the Analog Input, the GATE 1 -to- GATE 2 input (the output of the start/stop state machine), or the GATE 1 -AND- GATE 2 input. When enabled by the measurement cycling logic, the mode-control logic clears the counter chain and monitors the input from the input multiplexer. When the mode-control logic detects the beginning of a time interval, it asserts CET2- low. At the end of the interval, the mode-control logic de-asserts CET2- high, and signals the measurement cycling logic that the time measurement is complete and is ready for storage.

012-10. SLOW RATE TIME MEASUREMENTS

When making slow rate time measurements, the counter enable multiplexer enables the counter chain whenever the up/down count resolver asserts the CET1- signal low and the mode-control logic asserts CET2- low.

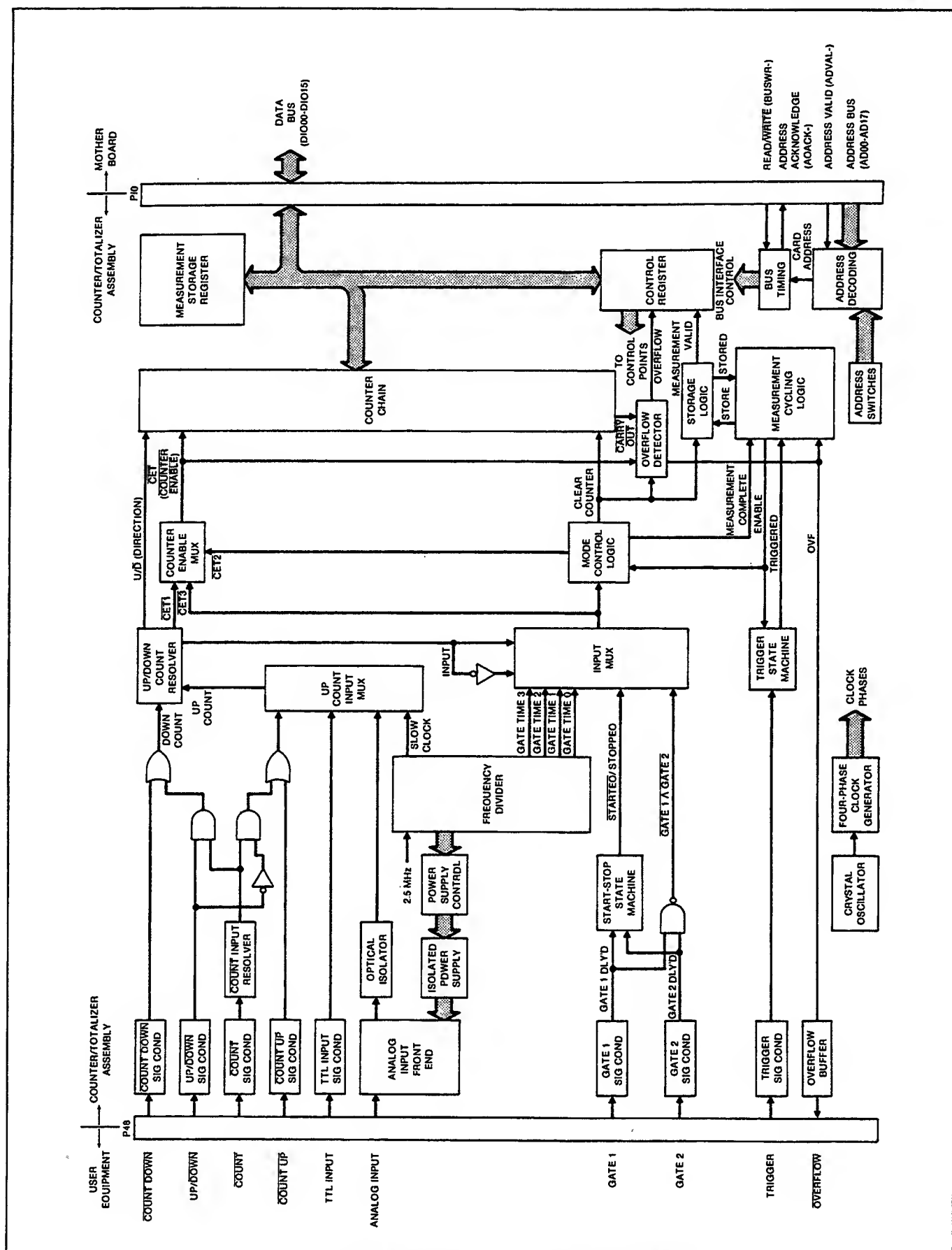


Figure 012-1. Option 1752A-012 Functional Block Diagram

The input to the up/down count resolver is provided by an output tap of the frequency divider (frequency = 1.22 kHz) through the up count input multiplexer. Whenever the up/down count resolver detects a rising edge on its input (the slow rate clock), it asserts CET1- low for one clock cycle to allow the counter chain to increment by one count. Thus, the counter chain increments by one count every rising edge of the slow rate clock (or every 819 μ sec) if CET2- is asserted low by the mode-control logic.

The mode-control logic enables the counter chain to count slow rate clock pulses through its output CET2-. The input multiplexer selects either the GATE 1 -to- GATE 2 or the GATE 1 -AND- GATE 2 signals as the input to the mode control logic. When enabled by the measurement cycling logic, the mode control logic clears the counter chain and monitors the input from the input multiplexer. When the mode-control logic detects the beginning of an interval, it asserts CET2- low. At the end of the interval, the mode-control logic drives CET2- high. The count present in the counter chain is proportional to the measured time interval (measured time = number of counts \times 819 μ sec). The mode-control logic then signals the measurement cycling logic that the time measurement is complete and ready for storage.

012-11. Frequency Measurement Mode

When making frequency measurements, the counter enable multiplexer enables the counter chain whenever the up/down count resolver asserts the CET1- signal low and the mode-control logic asserts CET2- low.

The input to the up/down count resolver is provided by the up/count input multiplexer, which selects either the ANALOG or the TTL input for measurement. Whenever the up/down count resolver detects a rising edge on its input (either the ANALOG or TTL input), it asserts CET1- low for one clock cycle to allow the counter chain to increment by one count if CET2- is asserted low by the mode-control logic.

The mode-control logic enables the counter chain to count rising edges on the ANALOG or the TTL input through its output CET2-. The input to the mode control logic is provided by the input multiplexer, which selects from one of four output taps of the frequency divider (GATE TIME 0-3). When enabled by the measurement cycling logic, the mode-control logic clears the counter chain and monitors the input from the input multiplexer. When the mode control logic detects the beginning of a GATE TIME, it asserts CET2- low. At the end of the GATE TIME, the mode-control logic drives CET2- high. The count present in the counter chain is proportional to the measured frequency (measured freq = number of counts \times 1/GATE TIME). The mode-control logic then

signals the measurement cycling logic that the measurement is complete and ready for storage.

012-12. Measurement Cycling

The measurement cycling and mode-control logic are not used when the Counter/Totalizer is in the Totalizing Mode. For the remaining modes (Time and Frequency), the operation of the mode-control logic is slaved to the measurement cycling logic.

At the beginning of a measurement cycle, the measurement cycling logic waits for the trigger state machine to detect a trigger signal if external triggering has been enabled by the user. If the external trigger is disabled, the measurement cycling logic does not wait. The measurement cycling logic then enables the mode-control logic and waits for the measurement to be complete. When the mode-control logic signals that the measurement is complete, the measurement cycling logic disables the mode-control logic and commands the storage logic to store the contents of the counter chain in the measurement storage register.

When the storage logic has successfully stored the measurement, it notifies the bus interface and the measurement cycling logic that a new measurement has been stored. If the single measurement mode is selected by the user, the measurement cycling logic then stops and starts the next measurement only after being re-armed by the bus interface. However, if the continuous measurement mode has been selected, the measurement cycling logic immediately begins the next measurement cycle.

012-13. Circuit Description

012-14. CONTROL REGISTER

The bus interface controls Counter/Totalizer functions by writing to the memory-mapped control register. Devices U28, U33, U40, and U47 comprise the control register. D-type flip-flops U28 and U40 store the control bits. Tri-state buffers U33 and U47 are used to read back the measurement status and the control bits. The control bits are listed in Table 012-2, and are explained further in later paragraphs.

012-15. ADDRESS DECODING, ADDRESS SWITCHES

Each one of up to 32 counter/totalizer assemblies in a system occupies two adjacent 16-bit words in memory-mapped I/O space. A set of five switches selects the assembly number in the range of 0 to 31. Assembly 0 occupies addresses 3F280-3F282, Assembly 1 occupies 3F284-3F286, up through Assembly 31 which occupies 3F2FC-3F2FE. When the assembly recognizes a valid address as its own, the CARD ADDRESS output of the address decoding block goes high for the duration of the memory cycle.

Table 012-2. Control Bit Functions

CONTROL BIT	FUNCTION
<u>-ANALOG</u>	Up Count Input Multiplexer Control
<u>-GATING</u>	Input Multiplexer Control
<u>-HOLD</u>	Card Enable Control
<u>-SINGLE/CONT</u>	Measurement Cycling Logic Control
<u>-TRIG ENABLE</u>	Measurement Cycling Logic Control
SLOPE	Trigger State Machine Control
STORE ENABLE	Storage Logic Control
<u>-MEASUREMENT VALID RESET</u>	Storage Logic Control
<u>-OVERFLOW RESET</u>	Overflow Detector Control
G0-G2	Input Multiplexer Control
M0-M2	Mode Control

The bus interface consists of 40 readable and 40 writable bits in 32 bits of address space. Each assembly utilizes two 24-bit overlays, or pages, in addition to 8 bits of common space, to achieve an actual 56 bits of memory space in the 32 bits of allotted address space. Overlay selection is accomplished by writing to the Overlay Select bit, which resides in the common 8-bit area. The overlay selected becomes active starting with the next memory cycle.

012-16. BUS TIMING

Since the Counter/Totalizer and the 1752A Single-Board Computer are run by separate time bases, the two systems run asynchronously with respect to each other. The bus timing block re-synchronizes the two systems during bus interface activity. Refer to Figure 012-2 for Bus Timing. If CARD ADDRESS is low, the bus timing logic is held in the reset state. When CARD ADDRESS goes high, indicating either a bus read or write, Flip-flop A is set on the next 01 clock phase. The BUS IDLE signal then goes low, disabling the counter chain from driving the internal data bus and disabling measurement storage. The bus read or write is then allowed to proceed. In the case of a bus write cycle, the write operation is performed before the board pulls the Address Acknowledge (ADACK-) line low.

012-17. MEASUREMENT STORAGE REGISTER

Three flip-flops (U22, U29, and U34) make up the 24-bit measurement storage register. Controlled by the storage logic, completed measurements are transferred directly from the 24-bit counter chain to the measurement storage register during 01. The stored measurement can then be read while the board is taking the next measurement.

012-18. COUNTER CHAIN

Six 4-bit up/down synchronous counters (U1, U8, U9, U15, U16, and U23) comprise the 24-bit bidirectional counter chain. If the CET- input to the counter chain is low during 04, the counter chain will increment if Up/Down (U/D-) is high and decrement if it is low. If CLEAR COUNTER- is low during 04, the counter chain is synchronously reset to all zeroes. If STORE ENABLE and BUS IDLE are both high, the tri-state output buffers of the counter chain are enabled onto the internal data bus. This condition exists whenever measurements are stored.

Pre-setting the totalizer BUS WRITE to the low-order 16 bits of the counter chain forces the LOAD LO-input low. Pre-setting BUS WRITE to the high-order 8 bits of the counter chain forces the LOAD HI-input low. (Note that BUS IDLE is low, so that the counter chain tri-state buffers are disabled.) The preset occurs synchronously during 04. Counting is disabled whenever HOLD- is low. The low HOLD signal does not affect the count in the chain, and is the means for suspending totalizing via the bus interface.

012-19. OVERFLOW DETECTOR

If, during 03, the counter chain is enabled to count (when CET- is low) during the next 04 and there is a carry out from the most significant bit, then an overflow is imminent. In this event, the overflow detector will reset the Overflow (OVF-) flip-flop (U35, pin 9) and OVF will go high. Note that OVF is stored as the Overflow status in the Overflow flip-flop (U35, pin 13) simultaneously with

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storing the measurement in the measurement storage register. Also note that CLEAR COUNTER- clears OVF.

012-20. STORAGE LOGIC

The storage logic is essentially a slave to the STORE signal. If STORE is high, the storage logic attempts to store the counter chain (24-bit) value in the measurement storage register during 01. If either STORE ENABLE or BUS IDLE is low, the storage logic is unable to store the counter chain value and waits until both signals are high. After measurement storage, the storage logic sets both the MEASUREMENT VALID flip-flop (U35, pin 7) and the STORED flip-flop (U35, pin 4), which are input to the bus interface and measurement cycling logic respectively. The CLEAR COUNTER-signal resets the STORED flip-flop during 04. This reset occurs whenever a new measurement is initiated by the measurement cycling logic.

012-21. MEASUREMENT CYCLING LOGIC

Operation of the counter is dependent on the measurement cycling logic. (The measurement cycling logic performs no function in the Totalizing Mode.) The following sequence is implemented by the measurement cycling logic:

1. Wait for trigger, if enabled.
2. Enable the mode-control logic, and wait for the measurement to complete.
3. Store the measurement.
4. Wait for software re-arming (single measurement mode only).
5. Go back to step 1.

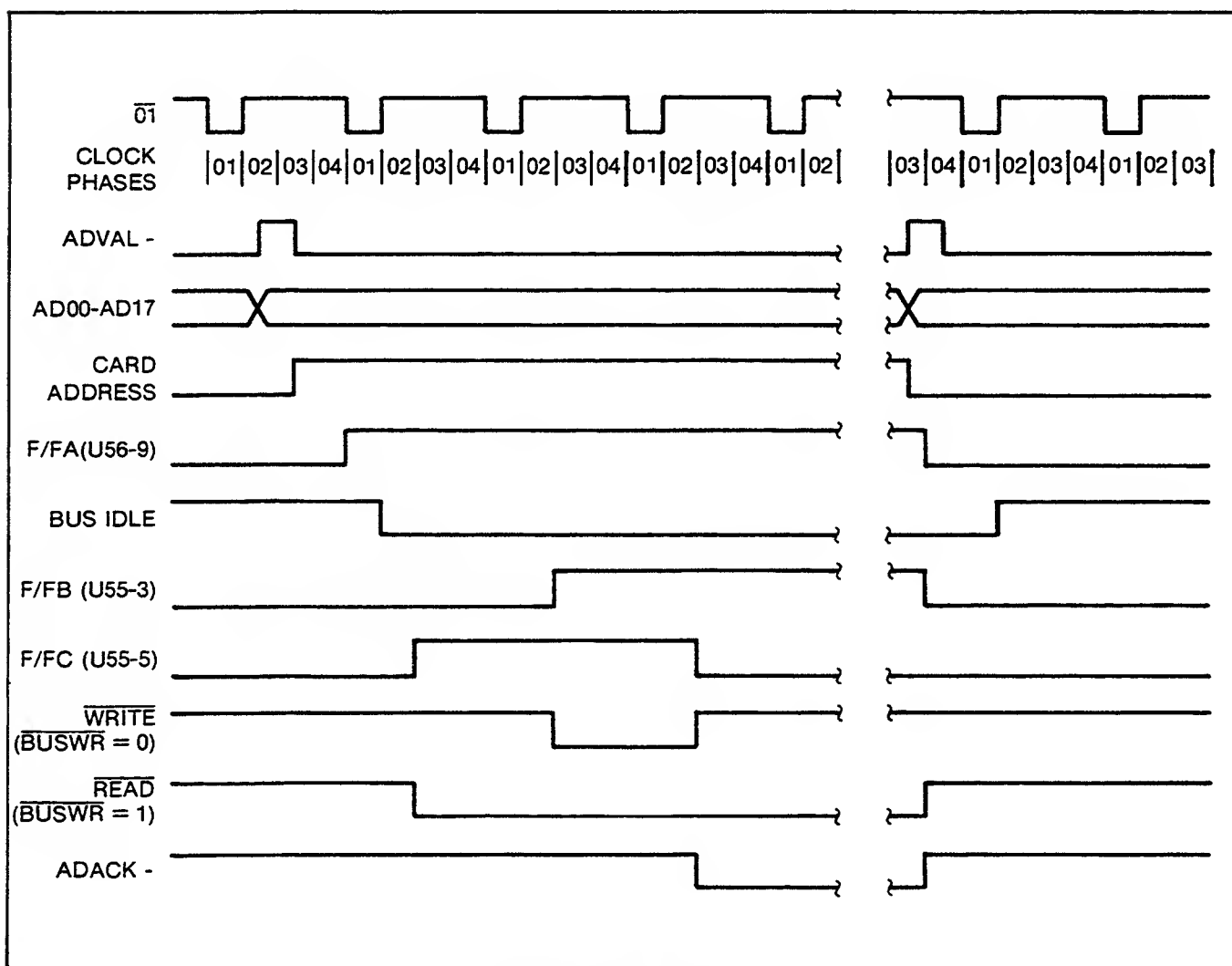


Figure 012-2. Bus Timing

Setting HOLD- low via the bus interface resets the measurement cycling logic. (Refer to Figure 012-3.) When HOLD- goes high, the logic begins as described in step 1. Both Flip-flop L (U3, pin 3) and Flip-flop M (U3, pin 5) are in the zero state. If TRIG ENABLE- is low, they will remain in the zero state until TRIGGERED goes high, which will cause Flip-flop M to go to the one state. If TRIG ENABLE- is high, Flip-flop M goes to the one state immediately, independent of the TRIGGERED input.

At step 2, Flip-flop L is a zero and Flip-flop M is a one. Note that the ENABLE output is the AND of Flip-flop L-, Flip-flop M, and the control input TOTALIZE-. Thus, if the board is not totalizing, the ENABLE output will go high. Until either the MEASUREMENT COMPLETE or OVF inputs go high, Flip-flop L will remain zero and Flip-flop M will remain one. When either the MEASUREMENT COMPLETE or OVF inputs go high, Flip-flop L goes to the one state, causing ENABLE to go low.

At step 3, Flip-flop L and Flip-flop M are both one. Note that the ENABLE output has gone low and the STORE output has gone high. Also note that if the control input TOTALIZE is a one, the STORE output is forced high permanently. Flip-Flop M will go to a zero after the STORED input goes high.

At step 4, Flip-Flop L is a one and Flip-Flop M is a zero. If the control input Single/Continuous (SINGLE-/CONT) is a zero they remain in that state until both are reset by HOLD- going low. If SINGLE-/CONT is a one, Flip-Flop L will go to a zero. This transition (step 5) takes the logic back to step 1.

012-22. MODE-CONTROL LOGIC

The measurement cycling logic controls the mode-control logic through its output ENABLE. Refer to Figure 012-4. If the ENABLE input is low, the mode-control logic is held in the reset state. In addition, outputs CET2- and CLEAR COUNTER- are forced high and MEASUREMENT COMPLETE is forced low. The operation of the mode-control logic is determined by control bit M1. Control bits M0 through M2 determine the fundamental mode of operation of the assembly. (See Table 012-3.)

Mode-control logic operation begins when ENABLE goes high. The CLEAR COUNTER- output goes low immediately, and goes high when Flip-Flop P (U66, pin 3) goes high. CET3- is the input to the mode-control logic. The CET2-output goes low when the mode-control logic detects a rising edge if M1 = 1, or a falling edge if M1 = 0. When the mode-control logic detects the next rising edge, the CET2- and MEASUREMENT COMPLETE outputs go high. When ENABLE goes low again, Flip-Flop N (U37, pin 3), Flip-Flop O (U37, pin 5), Flip-Flop

P (U66, pin 3), and MEASUREMENT COMPLETE all go low, initiating a new measurement.

012-23. COUNTER-ENABLE MULTIPLEXER

The counter chain is enabled by different conditions depending on the operating mode selected. The counter-enable multiplexer (U18) performs part of this task, and is controlled by bits M0 through M2. The counter enable multiplexer output CET- is a function of inputs CET1-, CET2-, and CET3- as indicated in Table 012-4.

For the time interval modes (falling edge to rising edge and rising edge to rising edge), counter enabling is controlled by the mode-control logic only. For time interval-slow rate and frequency modes, counter enabling is controlled by both the mode-control logic and the up/down count resolver. In the time interval-slow rate mode, the mode-control logic detects the time interval, while the up/down count resolver provides the slow-rate clock. (The slow-rate clock drives CET1- low for one clock cycle every 819.2 usec.) In the Frequency Mode, the mode-control logic detects the gate time (treating it as a time interval) and the up/down count resolver detects positive transitions of the input being measured.

In the Totalizing Mode, counter enabling is controlled by both the up/down count resolver and the input multiplexer. The up/down count resolver detects external commands to increment or decrement, while the input multiplexer selects the mode of totalizer gating.

012-24. INPUT MULTIPLEXER

The input multiplexer (U11) routes one of eight input signals, or logic low, onto the output CET3-. Selection is accomplished with control inputs G0 through G2 and GATING-. If GATING- is high, the output CET3- is low. If GATING- is low, then G0 through G2 control CET3- selection. Table 012-5 lists the sources of the CET3-output for different configurations of control inputs G0 through G2 and the different operating modes.

012-25. UP/DOWN COUNT RESOLVER

The up/down count resolver consists of an up count resolver and a down count resolver. The up count resolver detects positive transitions of the input UP COUNT, while the down count resolver detects positive transitions of the input DOWN COUNT. (Refer to Figure 012-5.)

The up/down count resolver controls the direction of the counter chain by means of its output U/D-. In all modes except totalizing, U/D- is forced high so that the counter chain only counts up. In those modes the down count resolver is disabled. Note that if both the up count resolver and the down count resolver try to count simultaneously, then CET- stays high.

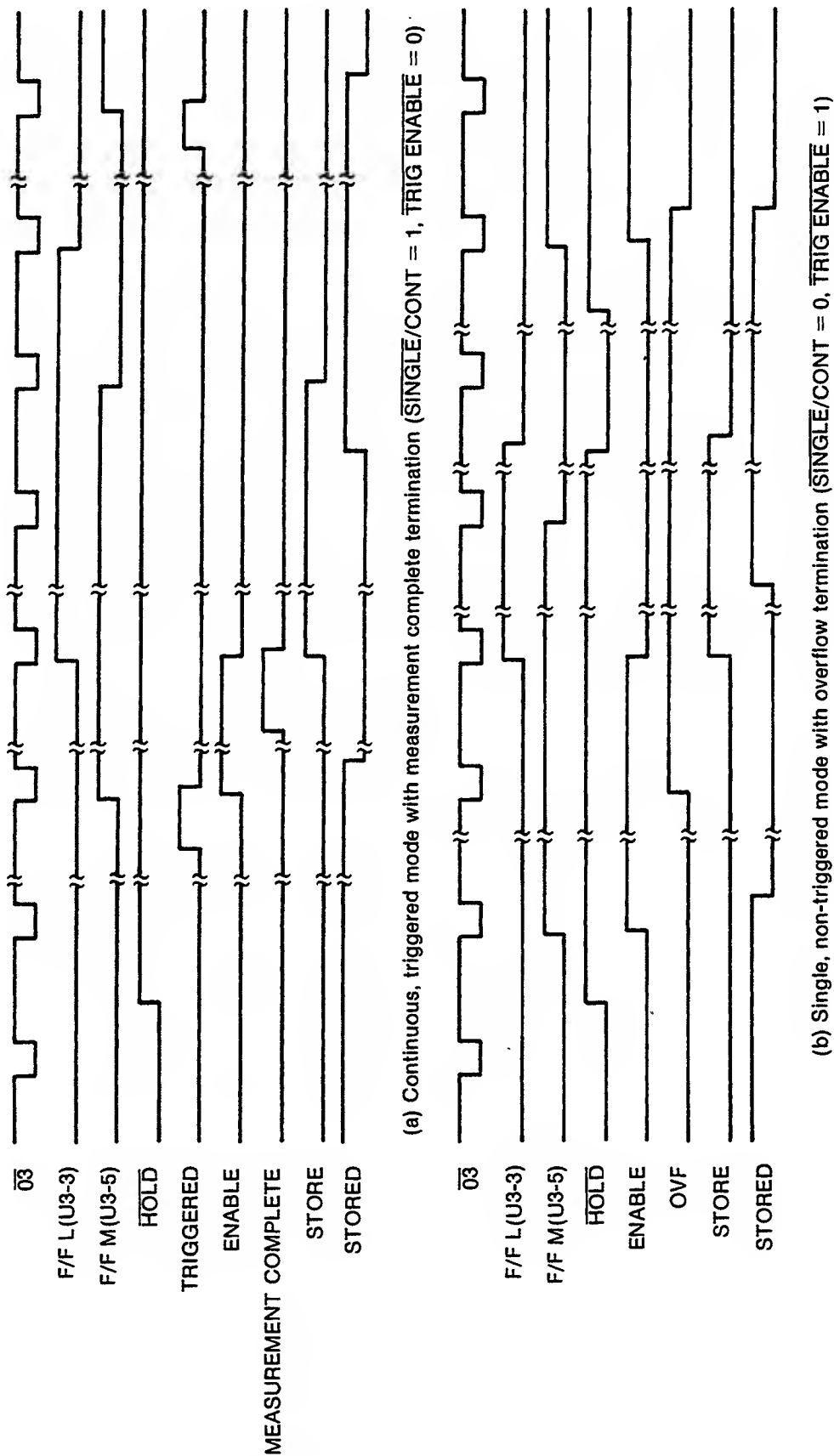


Figure 012-3. Measurement Cycling Logic (TOTALIZE = 0)

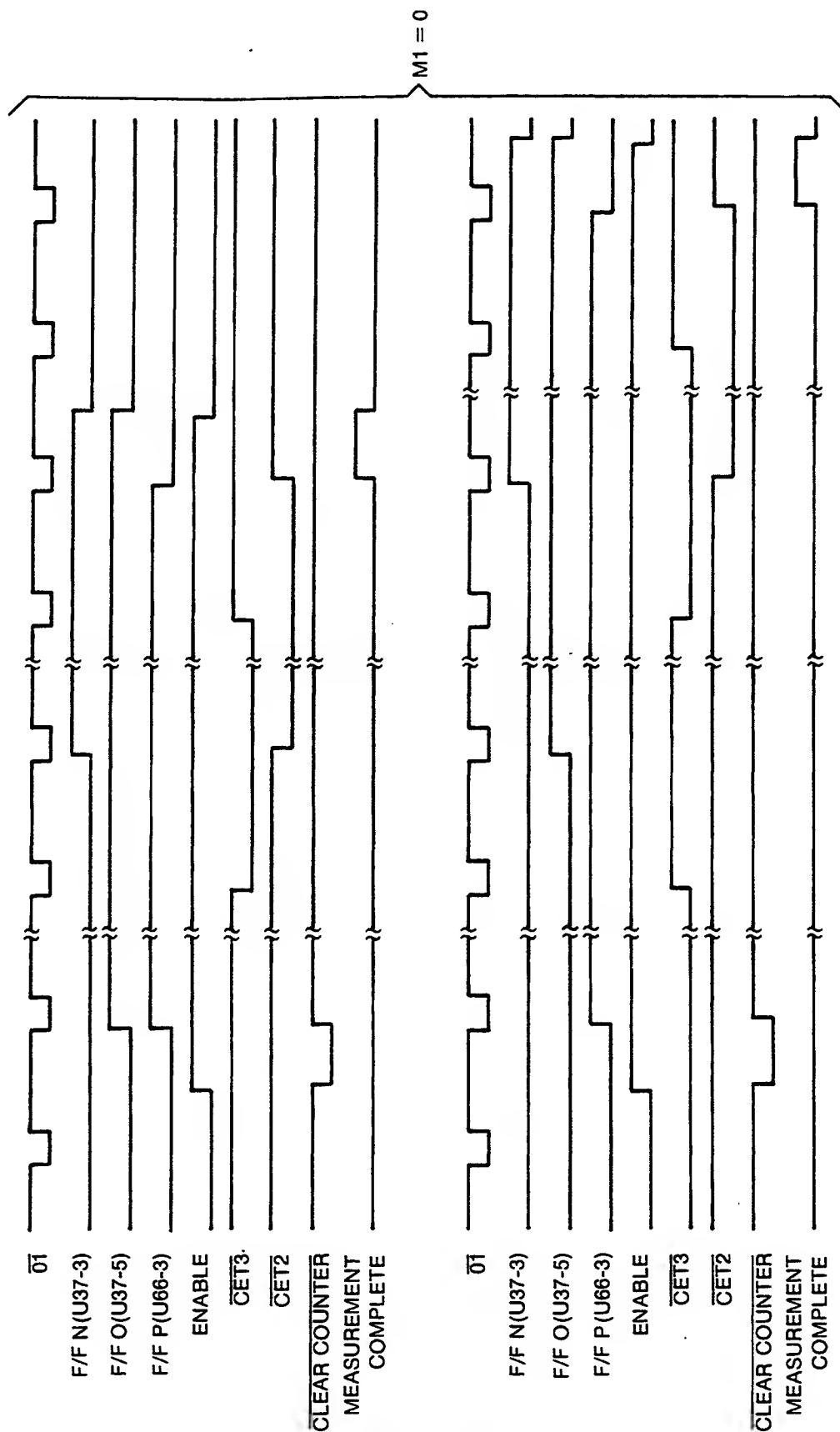


Figure 012-4. Mode-Control Logic

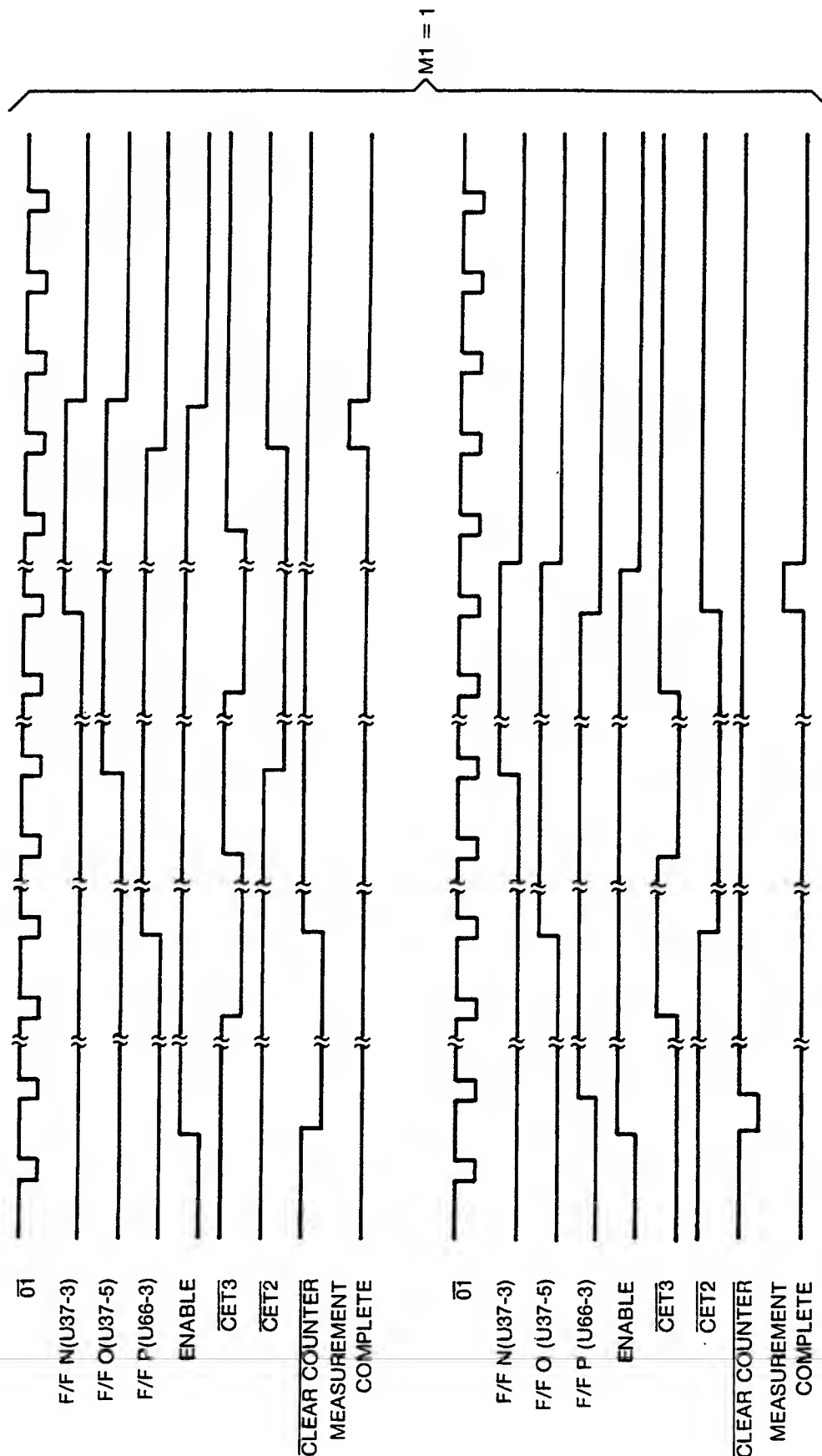


Figure 012-4. Mode Control Logic (cont)

Table 012-3. Operating Modes Per Control Bits

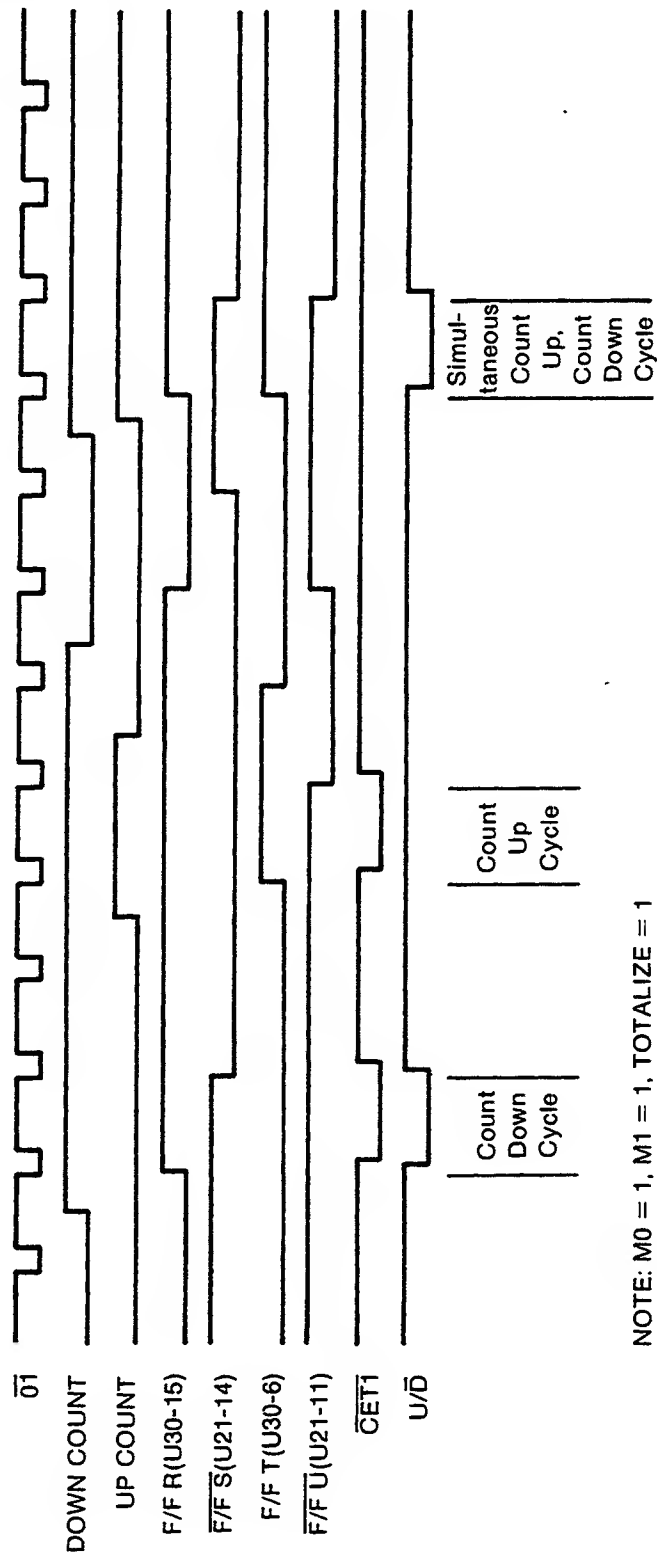
CONTROL BITS			OPERATING MODE
M2	M1	M0	
0	0	0	Time Interval — falling edge to rising edge
0	1	0	Time Interval — rising edge to rising edge
1	0	0	Time Interval - Slow Rate
1	0	1	Frequency
1	1	1	Totalizer

Table 012-4. Counter-Enable Multiplexer Modes

CONTROL BITS			OPERATING MODE	CET - FUNCTION
M2	M1	M0		
0	0	0	Time Interval — falling edge to rising edge	CET - = CET-2
0	1	0	Time Interval — rising edge to rising edge	CET - = CET-2
1	0	0	Time Interval - Slow Rate	CET - = (CET1*CET2)-
1	0	1	Frequency	CET - = (CET1*CET2)-
1	1	1	Totalizer	CET - = (CET1*CET 3)-

Table 012-5. Sources of CET3- Output (Gating- is low)

CONTROL INPUTS			-CET3 SOURCE	MODES USED IN (See note below)
G2	G1	G0		
0	0	0	U12-6 -(Gate1*Gate2) -	1, 2, 4, and 5
0	0	1	U7-4 Started/Stopped -	1, 2, 4, and 5
0	1	0	U13-4 Input-	2 and 4
0	1	1	U30-6 Input	2 and 4
1	0	0	U2-10 Gate Time 0	3
1	0	1	U4-3 Gate Time 1	3
1	1	0	U4-6 Gate Time 2	3
1	1	1	U4-8 Gate Time 3	3
OPERATING MODES:				
<ol style="list-style-type: none"> 1. Time Interval - Slow Rate 2. Time Interval - falling edge to rising edge 3. Frequency 4. Time Interval - rising edge to rising edge 5. Totalize 				



NOTE: M0 = 1, M1 = 1, TOTALIZE = 1

Figure 012-5. Up/Down Count Resolver

012-26. UP COUNT INPUT MULTIPLEXER

The up count input multiplexer (U44) routes one of four input signals onto the Up Count output. Selection is controlled by control inputs M0 through M2 and ANALOG-. (Refer to Table 012-6.)

012-27. START-STOP STATE MACHINE

The start-stop state machine (U7 and U14) interprets positive transitions of the GATE 1 Delayed (GATE 1 DLY'D) input as start signals and positive transitions of the GATE 2 Delayed (GATE 2 DLY'D) input as stop signals. The STARTED/STOPPED- output goes low after receiving a start signal and goes high after receiving a stop signal. Refer to Figure 012-6.

Positive transitions of GATE 1 DLY'D and GATE 2 DLY'D during the same 01 clock phase toggle the STARTED/STOPPED- output. If the output was stopped, the positive transition starts output; if the output was started, the transition stops output.

012-28. TRIGGER STATE MACHINE

The trigger state machine (U7) monitors the TRIGGER input for either a positive or negative edge, depending on which is selected by the control input SLOPE. Refer to Figure 012-7. If either HOLD or ENABLE is high, the trigger state machine is held in the reset state. After both become low, Flip-Flop Y (U7, pin 9) is set as soon as the TRIGGER input is high for a negative edge trigger or as soon as it is low for a positive edge trigger. Flip-Flop X (U7, pin 13) is set when the selected edge occurs, causing the TRIGGERED output to go high.

012-29. FREQUENCY DIVIDER

The frequency divider (U2, U4, and U5) consists of three dual 4-bit binary counters, forming a 24-bit free-running

divider chain clocked at 2.5 MHz. The divider chain taps are used as the gate times for frequency measurement, as control inputs for the isolated power supply, as a slow clock for the time interval-slow rate mode, and to set the debounce time for debounceable inputs.

012-30. ANALOG INPUT FRONT END

The analog input front end is isolated from the 1752A, deriving power from the isolated power supply and achieving signal output isolation through a high speed opto-isolator (U52). The trigger level of the front end is automatically set midway between the signal peaks. The output of a two-stage input buffer amplifier (U68) (each stage having a gain of approximately 10) is rectified to find the positive and negative peaks. These two signals are summed (U68), integrated (U68), and fed back as an offset into the second amplifier stage in order to balance the peaks around common. The input buffer amplifier's output is fed to a Schmitt trigger (U51) with fixed trigger levels centered around common. The output of the comparator drives the opto-isolator.

012-31. MAINTENANCE

WARNING

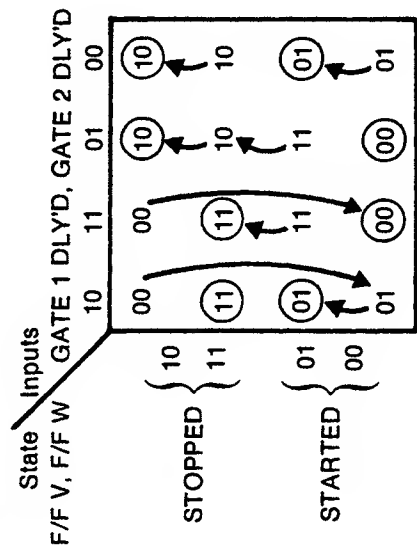
THE 1752A CONTAINS HIGH VOLTAGES. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE 1752A. TURN OFF THE INSTRUMENT AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

The following paragraphs describe maintenance procedures for the Counter/Totalizer. These procedures include hardware setup, performance testing, and troubleshooting.

Table 012-6. Sources of Up Count Output

CONTROL INPUTS				UP COUNT SOURCE
M2	M1	M0	-ANALOG	
0	x	0	0	U45-4 (-Analog Input)
0	x	0	1	U32-4 (TTL Input)
1	0	1	0	U45-4 (-Analog Input)
1	0	1	1	U32-4 (TTL Input)
1	0	0	x	U2-5 (Slow Clock)
1	1	1	x	U44-11, U38-10 (Totalize Inputs)
NOTE: X = Don't Care				

(a) Transition Table



$S_v = (GATE\ 2\ DLY'D) \wedge (F/F\ W)$
 $R_v = (GATE\ 1\ DLY'D) \wedge (F/F\ W)$
 $S_w = (GATE\ 2\ DLY'D) \wedge (F/F\ V)$
 $R_w = (GATE\ 1\ DLY'D) \wedge (F/F\ V)$

STARTED/STOPPED = F/F V

Example Timing Diagram

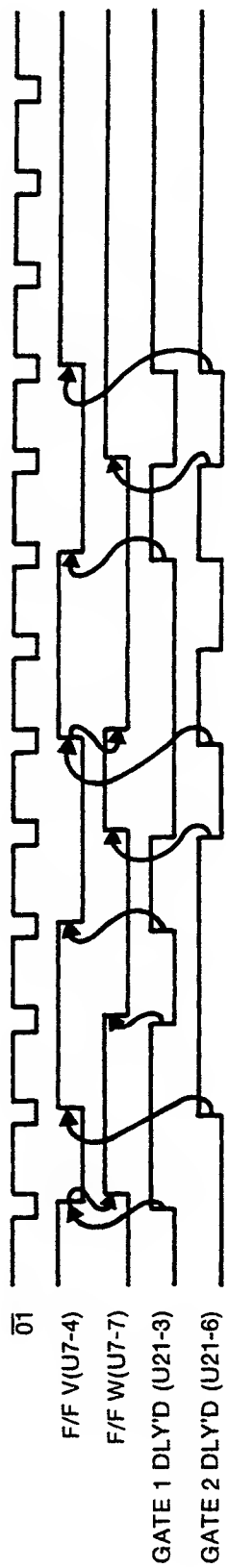
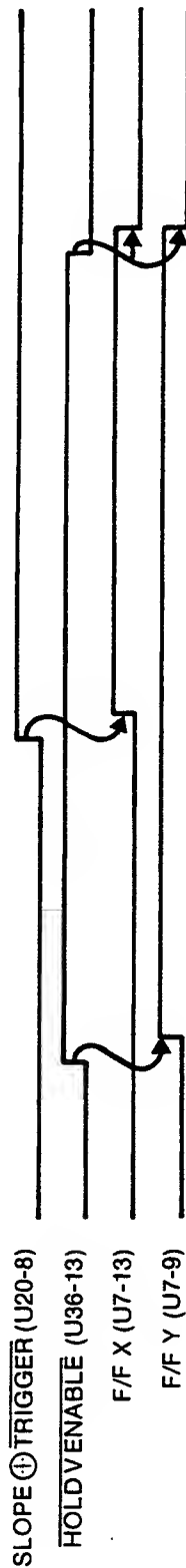
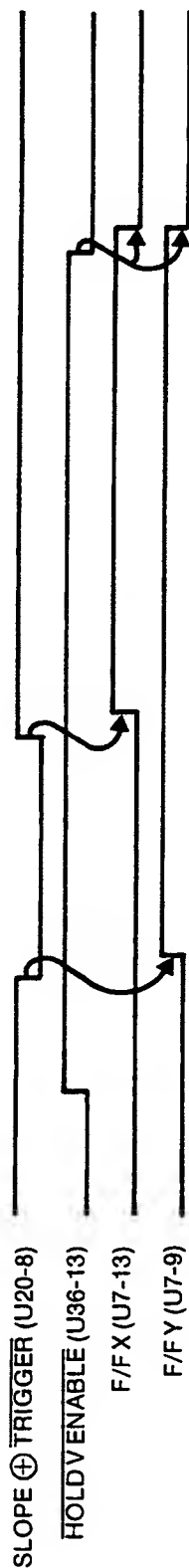


Figure 012-6. Start/Stop State Machine



TRIGGERED = F/F X

Figure 012-7. Trigger State Machine

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012-32. Hardware Setup

012-33. SETTING THE BOARD ADDRESS

You must assign a unique board address to each Counter/Totalizer in your 1752A system. The address is assigned by setting Address Switch (S2) as shown in Table 012-7. The location of address switch (S2) is shown in Figure 012-8.

assigned channel 0, board 1 would be assigned channel 1, etc.)

Note

*Switch S1 is used to select input debouncing.
 Its use is described later in this section.*

The board address can range from 0 to 31, inclusive. Setting the board address also assigns the corresponding number to the board's single channel. (Board 0 would be

The Counter/Totalizer has a 12-terminal connector for connecting to remote input source(s). See Table 012-8 for Connector Pin Assignments.

Table 012-7. Address Switch Settings

LEFT = ONE, RIGHT = ZERO S2 SWITCH SETTING = X X X X X						
Board Address	Address Switch Segments					Counter/Totalizer Channel Assigned
	B5	B4	B3	B2	B1	
0	0	0	0	0	0	0
1	0	0	0	0	1	1
2	0	0	0	1	0	2
3	0	0	0	1	1	3
4	0	0	1	0	0	4
5	0	0	1	0	1	5
6	0	0	1	1	0	6
7	0	0	1	1	1	7
8	0	1	0	0	0	8
9	0	1	0	0	1	9
10	0	1	0	1	0	10
11	0	1	0	1	1	11
12	0	1	1	0	0	12
13	0	1	1	0	1	13
14	0	1	1	1	0	14
15	0	1	1	1	1	15
16	1	0	0	0	0	16
17	1	0	0	0	1	17
18	1	0	0	1	0	18
19	1	0	0	1	1	19
20	1	0	1	0	0	20
21	1	0	1	0	1	21
22	1	0	1	1	0	22
23	1	0	1	1	1	23
24	1	1	0	0	0	24
25	1	1	0	0	1	25
26	1	1	0	1	0	26
27	1	1	0	1	1	27
28	1	1	1	0	0	28
29	1	1	1	0	1	29
30	1	1	1	1	0	30
31	1	1	1	1	1	31

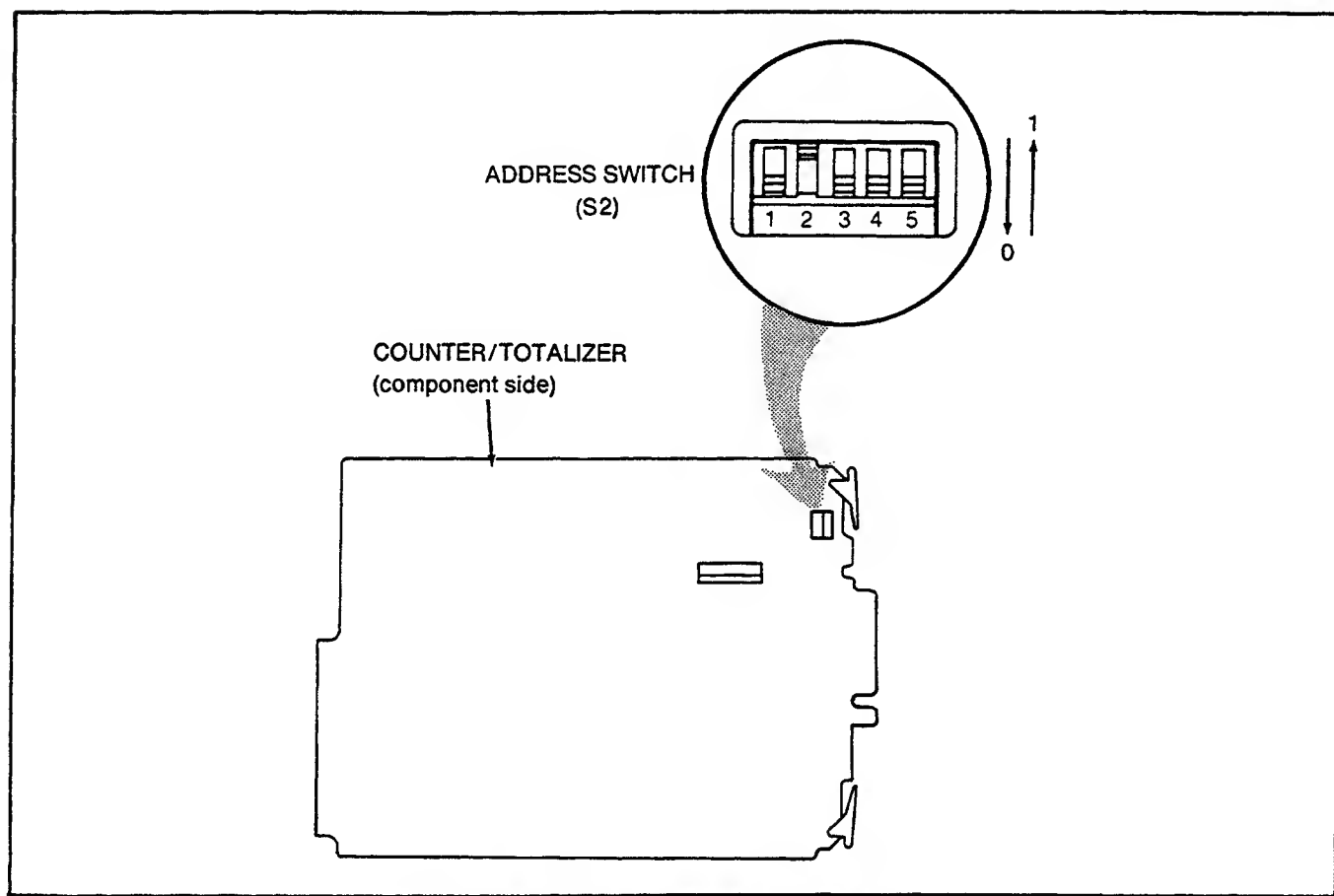


Figure 012-8. Address Switch Location

Table 012-8. Connector Pin Assignments

TERMINAL	SIGNAL	COMMON TERMINAL
1	Common (Isolated)	N.A.
2	Analog Input	1
3	Overflow	12
4	Gate 1	12
5	Gate 2	12
6	Trigger	12
7	Count Up	12
8	Count Down	12
9	Up / Down	12
10	Count	12
11	TTL Input	12
12	Common (Non-isolated)	N.A.

012-34. INPUT DEBOUNCING

Debouncing eliminates the risk of counting mechanical contact bounces when the module is totalizing contact closures. A reading is debounced by waiting after each input transition for a minimum pulse width to reject the contact bounce pulses. At the end of the timing pulse the input is accepted as having changed states. The following inputs can be individually selected for debouncing: Count, Count Up, Count Down, Gate 1, and Gate 2.

Debouncing selection is made by locating the debounce enable switches and setting them according to Table 012-9. To locate the debounce enable switches, refer to Figure 012-8.

012-35. Performance Test

The System Diagnostic Software verifies the proper operation of a majority of the Counter/Totalizer circuitry without the need for external inputs. While this software

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approach identifies many of the errors seen by factory technicians, additional tests are required to thoroughly test all of the option's circuitry. This section presents a performance test procedure that should be run in addition to the Software Diagnostic tests to completely verify the operation of the Counter/Totalizer.

The following equipment is required to complete the performance test procedure: a signal generator with a TTL and sine wave output, six pushbutton switches, one toggle switch (SPDT), a 12-pin screw terminal, and the 1752A System Diagnostic Software Disk.

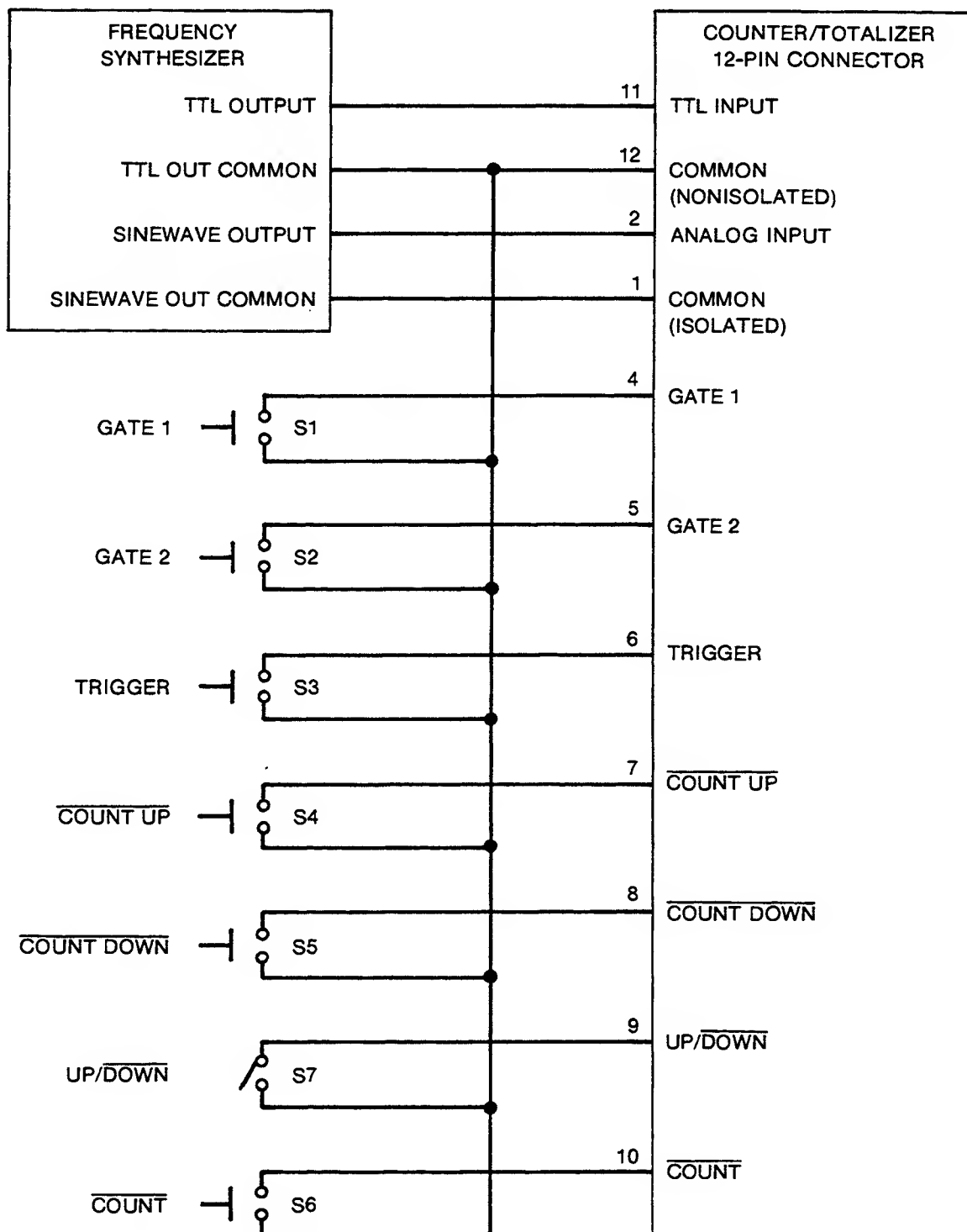
1. Turn the 1752A power off.
2. Remove the Counter/Totalizer option.
3. Set the module input debouncer switches S1, pins 1 through 5 to the ON position and place the module back into the 1752A. Refer to the paragraphs on input debouncing for debouncer switch positions.
4. Using the 12-pin screw terminal connector supplied with the Counter/Totalizer, a signal generator, six pushbutton switches, and one toggle switch, prepare the test setup shown in Figure 012-9. Push the 12-pin connector onto the Counter/Totalizer option.
5. Insert the System Diagnostic Disk and switch the 1752A power on.
6. After the System Diagnostic has loaded, run CTTST under the Counter/Totalizer subtest menu.
7. While CTTST is running, increment or decrement the channel accessed by the program to match the address switch settings of the module under test.
8. Press the following buttons on the 1752A screen in the order given:

FREQUENCY MEASUREMENT (selects mode of operation)
 ANALOG (selects source)
 209.7 ms (selects gate time)

9. Switch the signal generator power on. Output a 1 kHz 0.5V to 5 V rms sine wave voltage.
10. Verify that the reading shown on the 1752A screen is 1000 Hz \pm (4.77Hz + accuracy of the signal generator).
11. Press the HARD + and SINGLE buttons.
12. Verify that the UPDATE button on the 1752A screen is not flashing.
13. Press the trigger pushbutton shown in Figure 012-9.
14. Verify that the UPDATE button on the 1752A screen is flashing.
15. Change the signal generator frequency to 2 kHz.
16. Press the trigger pushbutton several times.
17. Press the UPDATE button on the 1752A screen. Verify that the reading shown on the 1752A screen is 1000 Hz \pm (4.77Hz + accuracy of the signal generator).
18. Set the signal generator to output a 1 kHz TTL square wave signal.
19. Press the following buttons on the 1752A screen in the order given:
 MENU (Returns you to the main menu)
 TIME MEASUREMENT
 SINGLE
20. Verify that the UPDATE button is flashing.

Table 012-9. Input Debouncing Switch Settings

UP = ON, DOWN = OFF S1 Switch Settings		
NUMBER	CARD LABEL	INPUT DEBOUNCED
S1-1	CD	Count Down
S1-2	CU	Count Up
S1-3	G1	Gate 1
S1-4	G2	Gate 2
S1-5	C	Count



NOTE: S1-S6 are S.P.S.T., N.O., pushbutton type switches. S7 is S.P.S.T., toggle type switch.

Figure 012-9. Counter/Totalizer Test Set Up

21. Press the UPDATE button several times. Verify that the readings shown on the 1752A screen are $1 \text{ ms} \pm (450 \text{ nsec} + \text{accuracy of signal generator})$.

22. Press the "- TO -" button on the 1752A screen.

23. Verify that the UPDATE button is flashing.

24. Press the UPDATE button several times. Verify that the readings shown on the 1752A screen are $1 \text{ ms} \pm (450 \text{ nsec} + \text{accuracy of signal generator})$.

25. Press the following buttons on the 1752A screen in the order given:

CONTIN
GATED
+1 TO +2 S

26. Press the GATE2 pushbutton several times. Verify that no reading is shown on the 1752A screen.

27. Press the GATE1 pushbutton, wait approximately 5 seconds, and then press the GATE2 pushbutton.

28. Verify that the reading shown on the 1752A screen is approximately 5 seconds. Do not worry about absolute accuracy.

29. Press the "+& TO -& S" button on the 1752A screen.

30. Press the GATE1 pushbutton twice. Verify that a reading is returned to the 1752A screen.

31. Press the following buttons on the 1752A screen in the order given:

MENU
TOTALIZE

32. Press the COUNT UP pushbutton once. Verify that the reading shown on the 1752A screen is 1.

33. Press the COUNT DOWN pushbutton once. Verify that the reading shown on the 1752A screen is 0.

34. Press the COUNT pushbutton once. Verify that the reading shown on the 1752A screen is 1.

35. Close the UP/DOWN switch.

36. Press the COUNT pushbutton once. Verify that the reading shown on the 1752A screen is 0.

012-36. Troubleshooting

System Diagnostic software is provided with the 1752A to aid in identifying faulty modules. The software contains subtests for specific functions of the -012 option. The System Diagnostic consists of a Counter Chain R/W Test, Timebase Selfcheck Test and CTTST. For more information on the System Diagnostic tests, see Section 3.

If an error is encountered by the System Diagnostic during the execution of a test, an entry is made in an error log. IF STOP ON FAIL was selected from the Main Menu, an error message will be displayed on the screen. If the error condition exists, first verify that the module is faulty and then replace it. (If the System Diagnostic will not load and run, see Section 3, Troubleshooting.)

The System Diagnostic Software does not verify the functionality of the entire Counter/Totalizer module. The Counter/Totalizer Performance Test provides additional tests for identifying faults.

If a module is failed by the System Diagnostic Software, or if it fails the Performance Test, the following troubleshooting procedures may be used to isolate the failure. Due to the great number of possible problems, only the most common problems encountered by factory technicians are discussed. If the problem encountered is not discussed in this section or if the procedure fails to repair a fault, contact the nearest Fluke Service Center. (See Section 4.)

Due to the complexity of the Counter/Totalizer module, isolating faults to a component level can be a very demanding and time consuming task, requiring a good understanding of the theory of operation. It is therefore recommended that you contact the nearest Fluke Service Center to replace a faulty module. If you wish to attempt to repair a module, you will need, at a minimum, the following equipment: a multi-trace oscilloscope, a $5\frac{1}{2}$ digit multimeter, a function generator with TTL output, a logic probe and a quantity of replacement components. Most chips are soldered into the circuit board, so it will be necessary to unsolder components in order to swap them.

CAUTION

Extreme care should be used when removing and replacing components to avoid irreparable damage to the printed circuit boards.

CAUTION

Modules are subject to damage by static electricity. For proper handling, see the static awareness information in Section 3.

The component-level troubleshooting information that follows is divided into three major sections. Each section describes a common symptom that may be exhibited by your 1752A. Each section is further divided into lists of possible cause(s) and suggested action(s). Suggested actions are presented in the order that they should be performed, and each action is dependent on the previous step. To use the troubleshooting information, you should first locate the applicable symptom, read the list of possible causes, and perform each action in the order presented, without skipping any steps.

SYMPTOM 1:

System Diagnostic returns the following error: Option is faulty, missing, or improperly configured.

POSSIBLE CAUSES:

- The address switches are set incorrectly (S2 segment 1 through S2 segment 5).
- The bus interface logic is faulty.

ACTIONS:

- Verify that the address switches are set correctly for the board address being tested. (Refer to paragraph 012-33 for board address switch settings.)
- Run the Counter Chain R/W test in Loop Mode and check the following:

Verify that TP60 toggles high. Failure is caused by the malfunction of the address decode circuitry (U20, U36, U53, U54, U58, U59, U63, or U64).

Verify that U53, pin 12 toggles low. Failure is caused by the malfunction of the bus synchronization circuitry (U55, U56, or U60) or the bus acknowledge circuitry (U48 or U53).

SYMPTOM 2A:

Option fails the System Diagnostic Counter Chain R/W test. Only a couple of bits of the counter chain cannot be written to or read from.

SYMPTOM 2B:

Option fails the System Diagnostic Counter Chain R/W test. All bits of the counter chain cannot be written to or read from.

POSSIBLE CAUSES:

- Address decode circuitry is faulty.
- Counter chain is faulty.
- Measurement storage register is faulty.
- Interface buffers are faulty.

ACTION 2A:

Run the Counter Chain R/W test in Loop Mode. Probe along the circuit path of the bad bits, looking for "stuck" levels. Find the source of the fault and replace the faulty components.

ACTION 2B:

Run the Counter Chain R/W test in Loop Mode. Look for logic activity on pins 5, 7, 9 and 11 of U24. Failure is most likely due to a fault in the address decode circuitry (U24, U26, U30, U41, U48, U49, U54, or U63).

012-37. Synchronous Logic Troubleshooting

The Counter/Totalizer consists of a large number of state machines that must be functional in order to complete a totalizing, time or frequency measurement. Consequently, if a fault is not approached systematically, it is very easy to "get lost" in the complex synchronous logic.

If an option cannot take measurements, check to see whether the option can totalize with external triggering disabled. This type of measurement requires the least amount of functional logic. If the module cannot totalize, proceed to Symptom 3.

If the option can totalize, check to see if it can make continuous time or frequency measurements with external gating disabled. These measurements require slightly more logic than totalizing measurements do. If the option cannot make time measurements, proceed to Symptom 4. If the option cannot make frequency measurements, proceed to Symptom 5.

If the option can take time and frequency measurements with external gating disabled, the option is almost totally functional. Check the following logic:

- Trigger state machine
- Start-stop state machine
- Analog input front end
- Overflow detection circuitry

OPTION 1752A-012
COUNTER/TOTALIZER

Use the theory of operation to troubleshoot these areas of the circuitry.

SYMPTOM 3:

Option cannot totalize with external gating disabled.

POSSIBLE CAUSES:

- Clock generator is faulty.
- Up/down count resolver is faulty.
- Counter enable multiplexer is faulty.
- Counter chain is faulty.
- Measurement storage logic is faulty.

ACTIONS:

- Look for logic activity on pins 8 and 10 of U62 and pins 3, 6 and 8 of U50. Lack of activity is due to the malfunctioning of U50, U57, U62, or U67. Troubleshoot and replace any faulty components.
- Using CTTST from the System Diagnostic Software, program the option to totalize with external gating disabled. Set all debouncer switches to the off position. (Refer to paragraph 012-34.) Input a 1kHz TTL signal into the UP COUNT- input and verify the following:

Check for logic activity at U20, pin 11. Lack of activity is most likely due to the malfunctioning of U20, U21, U25, U30, U38, U44, or U45. Troubleshoot and replace any faulty components.

Check for logic activity at TP67. Lack of activity is due to the malfunctioning of the counter enable multiplexer circuitry (U17 or U18), the input multiplexer (U11 and U30), or the control register (U40). Troubleshoot and replace any faulty components.

Check for logic activity on pins 13, 14, 15, and 16 of U1 and U8. Lack of activity indicates that the counter chain cannot increment. Troubleshoot and replace any faulty components.

Look for logic activity on the input and output pins of U22. Lack of activity indicates that the measurement storage register cannot store a reading. Troubleshoot and replace any faulty components.

Look for logic activity at U35, pin 7 (MEAS VALID signal). Failure is due to the malfunctioning of U35, U43, U54, or U61.

SYMPTOM 4:

Option cannot make continuous time measurements with external triggering disabled. The option can totalize with external gating disabled.

POSSIBLE CAUSES:

- Input multiplexer circuitry is faulty.
- The mode control logic is faulty.
- The measurement cycling logic is faulty.

ACTIONS:

- Using CTTST from the System Diagnostic Software, program the option to make continuous falling edge to rising edge time measurements on the TTL input. Disable external triggering. Input a 1 kHz TTL signal into the TTL INPUT and verify the following:

Check for logic activity at U11 pin 1. Lack of activity is due to the malfunctioning of U13, U26, U30, U31, U32, or U38. Troubleshoot and replace any faulty components.

Check for logic activity at U30, pin 12. Lack of activity is most likely due to the malfunction of U11 or U30.

Check for logic activity at U31, pin 8. Lack of activity is due to a fault in the measurement cycling logic (U3, U10, U12, U25, or U26) or the mode control logic (U12, U17, U25, U26, U31, U36, U37, U43, U48, 49, or U66). Using the theory of operation for these state machines (refer to paragraphs 012-21 and 012-22), troubleshoot and replace any faulty components.

Check for logic activity at TP67. Lack of activity is most likely due to the malfunctioning of U18.

SYMPTOM 5:

Option cannot make continuous frequency measurements with external triggering disabled. The option can totalize with external gating disabled.

POSSIBLE CAUSES:

- The frequency divider is faulty.
- The mode control logic is faulty.
- The measurement cycling logic is faulty.

ACTIONS:

- Look for logic activity on pins 12, 13, 14, and 15 of U11. Lack of activity on any of these pins is due to a failure in the frequency divider circuitry (U2, U4, U5). Troubleshoot and replace any faulty components.
- Look for logic activity at U30, pin 12. Lack of activity is most likely due to the malfunction of U11 or U30.

- Using CTTST from the System Diagnostic Software, program the option to make continuous frequency measurements on the TTL input using GATE TIME 1 (3.28 ms). Disable external triggering. Input a 1kHz TTL signal into the TTL INPUT and verify the following:

Check for logic activity at U31, pin 8. Lack of activity is due to a fault in the measurement cycling logic (U3, U10, U12, U25, or U26) or the mode control logic (U12, U17, U25, U26, U31, U36, U37, U43, U48, U49, or U66). Using the theory of operation for these state machines (refer to paragraphs 012-21 and 012-22), troubleshoot and replace any faulty components.

Check for logic activity at TP67. Lack of activity is most likely due to the malfunctioning of U18.

Option 1752A-013 Mainframe Interface Assembly

013-1. INTRODUCTION

The 1752A-013 Mainframe Interface Assembly forms a digital communication link between the 1752A Instrument Controller and the I/O options installed on the 1702A Extender Chassis. The Mainframe Interface Assembly is installed in the 1752A chassis and is connected by a shielded ribbon cable to the Extender Interface Assembly located in the 1702A.

The Mainframe Interface is a plug-in printed circuit board (pcb) assembly that connects to the motherboard in the 1752A. Two 1752A-013 modules may be installed per 1752A system. The modules are connected to the extenders by a standard 2-meter cable or the Option 2402A-502 9-meter cable.

013-2. SWITCH CONFIGURATION

The 1752A-013 option may be installed in slot 1,3,4 or 5 in the 1752A. If two Mainframe Interface Assemblies are installed, one assembly must be designated as board 0 and the other as board 1. Boards are set by moving the small slide-switch forward or backward on the pcb. The forward position designates the card as board 0 and the backward position designates the card as board 1.

013-3. SERVICING THE 1752A-013 OPTION

For 1752A-013 service information, refer to the manual supplied with the option.

013-4. ADDITIONAL SYSTEM COMPONENTS

To aid in understanding the role of the 1752A-013 interface in the 1752A extended system, brief descriptions

of the 1702A-502 I/O Extender Cable and the 1702A Extender Chassis follow.

013-5. 2402A-502 I/O Extender Cable

The extender cable is an extended length, optional 9-meter cable that provides a connection between the 1752A and 1702A. It carries data, addresses, status and commands between the 1752A Single Board Computer and the I/O options installed in the 1702A chassis. A maximum of 15 meters of cable is allowed from the 1752A to the last extender in a leg. (See Figure 013-1.)

013-6. 1702A Extender Chassis

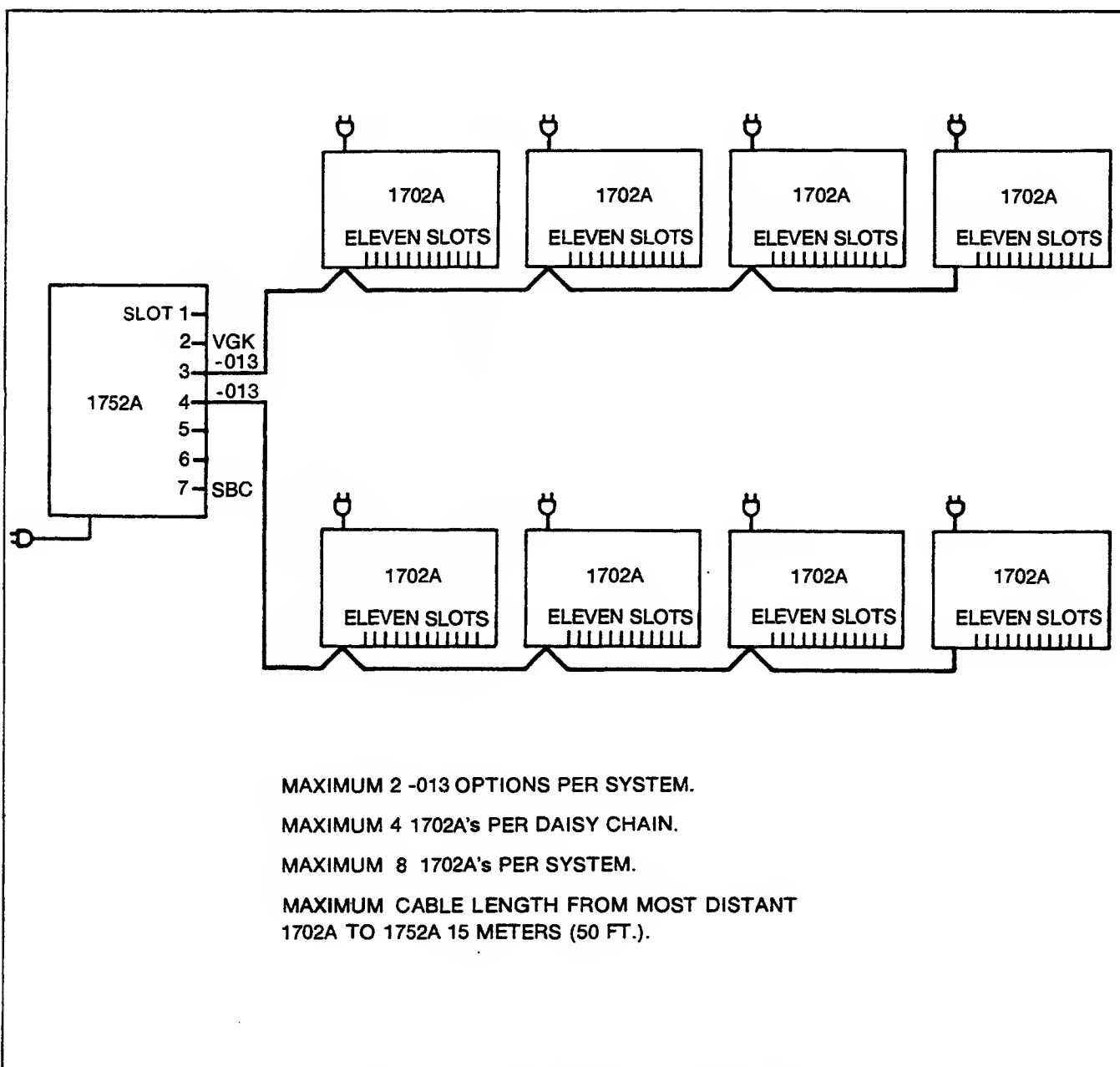
The Fluke Model 1702A I/O Extender Chassis provides further installation space for control and measurement options. Up to eight Extender Chassis may be used in a system. Each 1702A contains a power supply and 11 slots for I/O option installation. The Parallel Interface (-002 option), Analog Measurement Processor (-010 option), Analog Output (-011 option), and Counter/Totalizer (-012 option) may reside in the 1702A chassis. However, the total current required for all installed option assemblies must not exceed 11 Amps. Refer to Table 013-1 for the current draw for each option and the maximum number of boards allowed per system. For more information on the Extender Chassis, see the manual supplied with the 1702A.

013-7. System Configuration Alternatives

The daisy-chain in Figure 013-1 shows the maximum extension possibilities for the 1752A, utilizing the 1752A-013 and 1702A options.

OPTION 1752A-013**MAINFRAME INTERFACE ASSEMBLY****Table 013-1. Current Requirements and System Channel Capacity**

Option	Current Requirements	Maximum No. of Boards	Maximum No. of Channels
-002 Parallel Interface	.73A	8	16
-010 Analog Measurement Processor	.6A	4	128
-011 Analog Output Volts Current	1.3A 1.6A	32	128
-012 Counter/Totalizer	1A	32	32

**Figure 013-1. I/O Extender Chassis Configuration**

Options 17XXA-018/019/020 Nonvolatile Memory Modules

018-1. INTRODUCTION

The 17XXA-018/019/020 Nonvolatile Memory Modules provide Nonvolatile Random Access Memory (NVRAM) configured as file-structured, mass storage devices. The NVRAM modules cannot be used as Expansion Memory. Unlike the standard E-Disk, files stored in the NVRAM devices are not lost when power is removed from the mainframe. Data remains intact for a minimum of five years from the installation date of the battery. However, as with any mass storage device, making a backup copy of the contents is strongly recommended. Each NVRAM module may be write protected by the user. If the module is set to the protected mode, files cannot be written, changed, or deleted, and formatting or zeroing of the device is prevented. Reading or copying the files is still allowed. However, the System Diagnostic test does ignore the Write Protection.

The 17XXA-018/019/020 modules contain 256K, 512K, and 1024K bytes of storage, respectively. The maximum number of NV RAM modules (in any combination of sizes) that may be addressed in a system is eight, designated NV0: through NV7:. The number of available, addressable option module slots varies by instrument: the 1722A and 1752A allow for a maximum of five option slots, and the 1711A/AA allows for a maximum of eight option slots.

Unlike multiple Expanded Memory or EDISK modules which combine to make one larger logical device, each NVRAM module is always a separate device. Each board

uses its own device address designation and does not combine with others. The NVRAM modules need not be addressed sequentially. The module address may be freely changed while powered off. Modules may be transported between mainframes to transfer or distribute files.

The NVRAM modules are compatible with FDOS Version 1.6 and above and BOOT Version 1.3 and above. If the FDOS does not have the NVRAM driver included, the user will be required to recreate a new FDOS containing the NVRAM driver by running SYSGEN.

This manual applies to all members of the NVRAM family and to all revisions. If an individual member or revision differs in some significant way, it will be noted. For a description of the memory types and amounts of each of the members of the NVRAM family, refer to Table 018-1.

018-2. Overall Memory Considerations

The maximum amount of installable Extended Memory or E-Disk is reduced when any NVRAM modules are installed; the normal 3M-bytes maximum is reduced to 2.75M-bytes. The one quarter M-byte address space from 100000 through 13FFFE is used exclusively by the NVRAM options (excluding any Extended Memory or E-Disk options). Also, Extended Memory or E-Disk cannot be installed in an area where its address space would extend into this exclusive NVRAM area.

The V7800 Multifunction Board (MFB) option addresses this same space in the same manner as the NVRAM

Table 018-1. NVRAM Memory

OPTION	SIZE	MEMORY CHIP	
		NUMBER	SIZE
17XXA-018	256K-Bytes	8 (+2 for parity)	32K x 8 (28 pins)
17XXA-019	512K-Bytes	16 (+2 for parity)	32K x 8 (28 pins)
17XXA-020	1M-Bytes	8 (+2 for parity)	128K x 8 (32 pins)

modules and is specifically intended to co-exist with the NVRAM modules. When a V7800 MFB option is installed (with or without NVRAM modules), Extended Memory or E-Disk is still limited to 2.75M-bytes.

WARNING

FIRE, EXPLOSION, AND SEVERE BURN HAZARD EXISTS IF THE LITHIUM BATTERY IS RECHARGED, DISASSEMBLED, HEATED ABOVE 212 DEGREES F (100 C), INCINERATED, OR IF THE BATTERY CONTENTS ARE EXPOSED TO WATER.

CAUTION

Do not contact the circuit side of the module or the test points with any conductive material (including black foam, shielding bags, other circuit boards, conductive storage boxes, metal shelves, etc). Degradation of battery life and loss of memory contents may occur.

018-3. Low Battery Condition

The battery on the NVRAM module is normally checked each time the system is booted up (warm or cold boot). If the battery level is low, a warning message is printed; touch the TSO to continue the boot sequence. For unattended operation, the BOOTCK jumper (JM6) may be installed (Rev A and above only). The battery check will not be performed and the 1722A or 1752A will attempt boot-up regardless of battery conditions.

The low battery check is intended to detect a degraded battery well before actual loss of data. If the warning message occurs, battery replacement is recommended as soon as possible to prevent loss of data. Refer to the section below on battery replacement. The battery may also be tested with the System Diagnostic (SD) program. Finally, an FDOS call is provided for the user to allow testing of the battery status from within a program, which is especially useful if the unit is seldom turned off or rebooted. For an example of an assembly language routine and usage of the FDOS call, see CHKBAT on the System Diagnostic diskette (1722A/52A Rev 10 or 1711A/AA Rev 5, or later.)

018-4. THEORY OF OPERATION

Figure 018-1 is a block diagram of the card. Each block is discussed below.

018-5. Bus Interface

The AGGIE/ARGUS bus interface is a very straightforward set of bus receivers and transceivers. All transfers are word (16 bit) wide, so all the available data lines D0-D15 are buffered onto the board. A1-A21, AGVAL-, and ADVAL- are used for addressing, SYNC- and BUSWR-

are for control, and DCOK is for initialization reset. A higher speed receiver is needed for AGVAL- and SYNC- to meet worst-case timing specs.

018-6. Address Decoder

The card occupies space both on the ARGUS bus for control and on the AGGIE bus for memory access.

018-7. ARGUS Bus

Each card uses one word-wide address on the ARGUS bus. The address is 3F47x, where x is the board number times 2. The three card-address positions of the DIP switch set the active card ARGUS address. This enables the software driver to access up to eight NV cards individually. When a valid card address is active on the bus, ARGSEL- on that board goes true, and ADAK- is generated. Reading this address accesses the status register of U4 and U14; writing this address sets the command register U34. All communication is handled by the software driver.

018-8. AGGIE Bus

AGGIE space is used for memory array access. One 256K-byte page of NV memory is paged into AGGIE space at a time by the driver. 256K cards have only one page, while the 1M cards have four pages. The addresses used for the active page are 100000 to 13FFFE. This conflicts with the last 1/4 M-byte E-Disk/expanded memory location, so the use of the E-Disk and NV options are mutually exclusive in this address space. Effectively, this means that E-Disk/expanded memory is limited to 2.75M-byte maximum if any NV cards are used.

The V7800 Multifunction Board (MFB) communicates in a manner similar to the NV cards and has the same mutually exclusive restriction on the last 1/4M-byte of E-Disk/expanded memory. NVRAM modules and Multifunction Boards co-exist without conflict just as multiple NVRAM modules co-exist, even though they all use the same AGGIE addresses.

018-9. Status and Control Registers

Status register bits (read only) are portrayed in Table 018-2. Command register bits (write only) are defined in Table 018-3.

018-10. Data and Parity Memory Array

The memory array consists of 32Kx8 or 128Kx8 memory chips arranged word-wide (16 bits). Their chip selects are provided by the address decoder, R/W (directly from the bus), and OE- via a delay (U8 and U1) to prevent data bus glitching. They are powered by a battery backed-up supply, Vm, detailed below. Chip access time from CS- should be 120 ns or faster to provide valid data in time for the parity circuit. Since memory standby current drain is critical for rated battery life (5 years minimum), low-power parts are specified. In addition, CS- must be within 200 mV of Vm during powered down conditions in order to maintain memory.

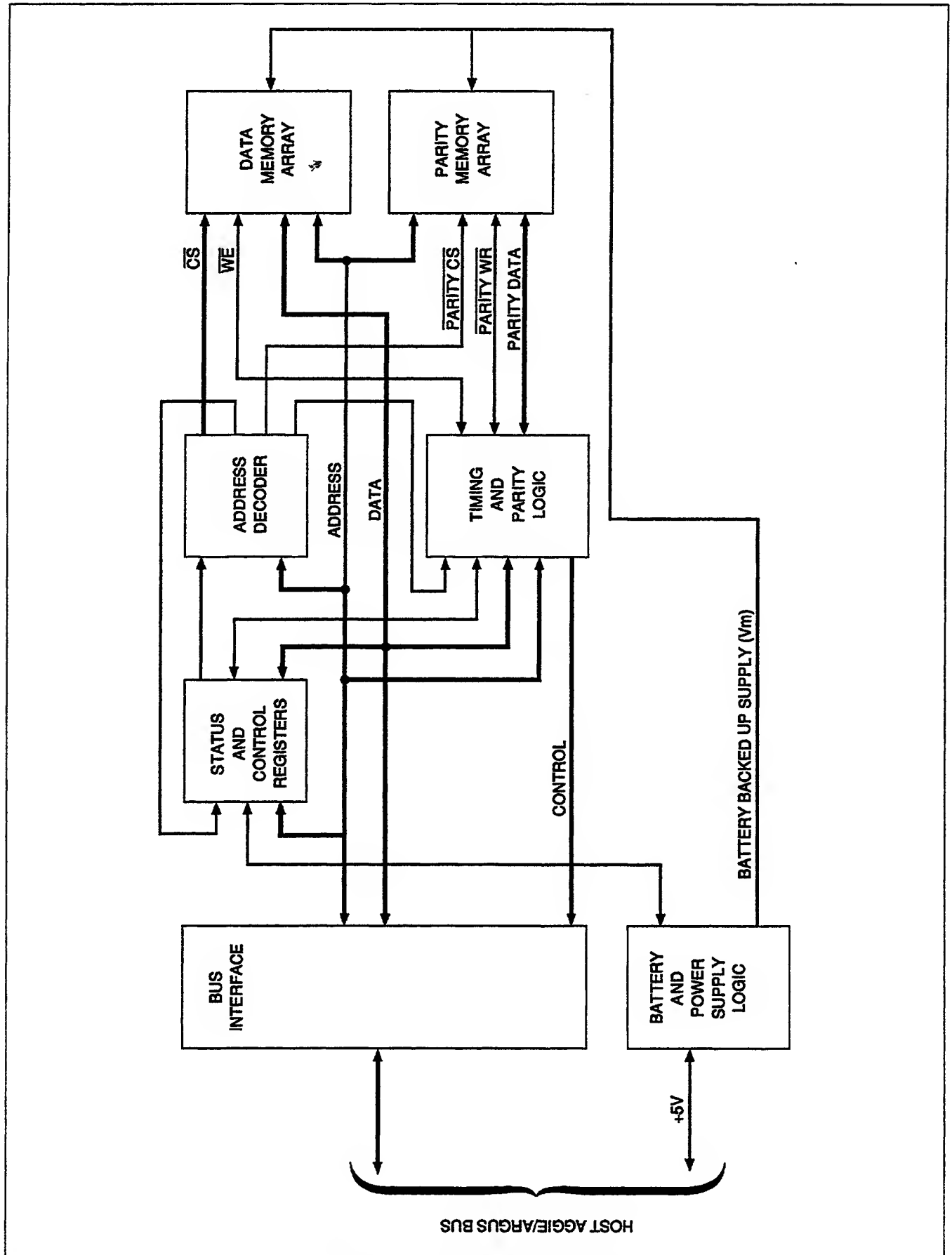


Figure 018-1. NV RAM Block Diagram

Table 018-2. Status Register

BIT	DESCRIPTION	USAGE	
0	Parity error	Active HIGH	
1	Board ready/formatted	Active LOW	
2	Battery OK	Active LOW	
3,4	Board size	BIT 3	BIT 4
	256K-Bytes	LOW	LOW
	512K-Bytes	HIGH	LOW
	1M-Bytes	LOW	HIGH
	2M-Bytes	HIGH	HIGH
5	Write protect	Active HIGH	
6	No battery boot check	Active LOW	
7	32 pin memories	Active LOW	
8-15	Reserved		

Table 018-3. Command Register

BIT	DESCRIPTION			
0,1,6	Active Memory Page Select			
	PAGE	Bit 0	Bit 1	Bit 6
	0	LOW	LOW	LOW
	1	HIGH	LOW	LOW
	2	LOW	HIGH	LOW
	3	HIGH	HIGH	LOW
	4	LOW	LOW	HIGH
	5	HIGH	LOW	HIGH
	6	LOW	HIGH	HIGH
	7	HIGH	HIGH	HIGH
2	Board enable	Active HIGH		
3	Parity error reset	Active HIGH		
4	Clear RDY/format flag	Active HIGH		
5	Set RDY/format flag	Active HIGH		
7	2M key	Active HIGH		
8-15	Reserved			

018-11. Timing and Parity Logic

To make complete use of static RAM chip space, individual output bits must be selected and used. During a memory read cycle, the upper two address bits (MA17 & 18) and the first page/bank select (BAD0) are decoded for chip select of data memory, and are used for bit select of parity memory via U21 and U28. Thus bits 0 through 7 of parity memory correspond to chips 0 through 7 of data memory. The parity bit is checked with data in U22 and U29. If it correct (odd), the rising edge of clock1 on U24 will latch in a 0, thus making PERR false, with no further action required. If either upper or lower byte parity is in

error (even), PERR will be latched true. PERR is read by the software driver via the status register.

During write cycles to parity memory, data is written to data memory in a conventional fashion. This same data is also presented to the parity checkers U22 and U29, along with the existing parity bit for that data memory location. If the parity bit is correct (a 50-50 chance), no write cycle to parity memory is required, and none is performed. However, if the parity bit is incorrect, it must be rewritten, along with all the other bits in the parity word. Wrong parity on a write cycle is signaled by a high on U23-4

(lower byte) and/or U13-13 (upper byte). This is latched into U30 by the rising edge of clock 2. An active low 'change parity bit' signal is thus present at U30-8 and/or U30-6. Simultaneously, the entire parity word is presented to the inputs of 16 exclusive OR gates (U18, 19, 25, 26). U17 generates a logic low in the other input of the active bits' exclusive OR, thus inverting the active parity bit from each byte. This 'corrected' parity word is latched into U20 and U27 by clock 2. If the bit(s) in question were incorrect, the 'change parity bit' signal(s) mentioned above will be present, and in conjunction with clock 4, will enable the outputs of U20 and/or U27 onto the parity data bus, and write that new parity data into parity memory with the PWEL- and PWEU- signals. When the host write cycle is completed, MEMSEL goes false, thus clearing the 'change parity bit' flags by resetting both halves of U30, and completing the parity cycle for writes.

The clocks used by the parity logic are generated by U12 and U7. U12 is a counter that is enabled by MEMSEL, which counts rising edges of SYNC-. Timing is arranged so that valid data is present for worst case timing conditions for all stages of the parity logic. Additionally, U12 and U32 provide ADAK- back to the host for valid card AGGIE addresses. ARGUS bus activity result in zero bus wait states, whereas AGGIE bus activity is delayed so that one bus wait state is inserted.

018-12. Battery and Power Supply Logic

Power to the data and parity memory arrays (Vm) must be maintained at all times to prevent loss of memory. U16 (on Assy Rev 0 boards) or U11 (on Assy Rev A or above boards) is an automatic power supply crossover switch. It compares the host 5-volt supply to the voltage of the battery(s), and provides the higher of the two to Vm. Bulk tantalum and ceramic bypass on Vm make for a smooth transfer. Since the automatic switch is incapable of supplying sufficient current for worst case active memory chips, Q1 is a current boost from the 5-volt supply. No boost for the battery is required since the memory chips are then in their low power deselected standby retention mode.

The READY/FORMATTED flip-flop, U35, is directly powered by the battery(s). This is set to the READY position by the software driver formatting routine, indicated by a low-true level on RDY-. When battery power is reapplied, U35 is automatically reset by C38 and R6. Any access to the memory will be blocked by the driver until the card is reformatted.

If the RDY- flag is false, an attempt to access the board will cause a "?Device error" message. If you suspect that the flag has accidentally been set false, it can manually be set true without formatting the device with either of the following two methods:

- With HDT:
FDOS>hdt
UA:caF47x (address the board, x = 2 times the board number, in hex)

UA:cw10,20 (sets the RDY flag)

UA:ex

- In hardware:

Momentarily connect U35 pin 14 (+BAT) to U35 pin 4.

However, if the contents are corrupted, the access will return a "?Illegal Directory" message. If the contents appear valid, a SCAN should still be performed. For example, send: fup nv0:/s.

U36 is the battery voltage comparator. At system boot, the battery condition is checked by the boot code. If a voltage less than 2.25V is detected, BATOK is set high (false), and the condition is shown on the system console. The operator must manually elect to continue the boot process. Although powered operation is not dependent on battery integrity, the memory may have already been corrupted while powered down. On Rev A (or above) boards, a jumper may be placed in JU6 (BOOTCK), which will bypass the battery check routine. This allows unattended operation to attempt power-up regardless of battery condition.

When there is a low battery detected from normal battery life discharge there should be sufficient charge to maintain memory until the battery can be replaced. Test points are provided on the board for battery voltage measurement. These points may also have a 3.5V source connected to them while a battery is being replaced to prevent memory loss. Application of a higher voltage may itself trigger a reset of U35.

On Assy Rev A (or above) boards, two batteries independently feed U11. The battery voltage comparator, U36, detects the first battery to fall below normal. However, since both batteries will track within a few millivolts during their normal life span, both batteries should be replaced at the same time. Premature failure of one battery would suggest replacement of only that battery.

The circuit will detect when either battery falls below the reference of approximately 2.25V. When tripped, the R5 feedback loop raises the reference slightly as a form of hysteresis. The battery connections themselves are high impedance nodes and, if not connected, will float to unknown levels potentially tripping the low battery indicator. When performing battery check in the System Diagnostics, a 1K resistor or just a wire suffices to bring the node low to cause a trip.

On the two-battery version, the fourth section of U36 lights CR4 when BATOK trips. A brief flash of CR4 is typical when power is applied or removed. The two-battery boards can be run with one battery if necessary but with the stipulation that TP2 and TP3 be tied together. This keeps both nodes high to avoid a trip.

018-13. Unused Component Positions

Although the following component positions are labeled on the NVRAM PCA, the actual components are not included:

- R22 and Q4.

These components constitute the "32PIN" flag, which is intended to signal the System Diagnostic program that 32-pin memory devices were used in place of 28-pin devices in 256K and 512K boards for use in "U" number fault isolation. The SD program does not currently recognize this flag nor have any boards been so configured.

- R15 and Q3

These components constitute the KEY, but have not been included on any units produced. The intended use of KEY was to keep the contents of a future 2M-byte option from being destroyed by early versions of the NVRAM driver. With R15 and Q3 installed, the board remains disabled unless used with BOOT version 1.7 or above or with FDOS version 2.0 or above. These newer BOOT and FDOS versions would properly support a 2M NVRAM option should one ever be produced and would be able to send an activating bit to turn on the KEY to enable the option. Prior versions of the NVRAM driver, which would destroy the contents of a 2M board, do not turn on the KEY to activate the board. The System Diagnostic program does not support a 2M NVRAM option.

018-14. TEST PROCEDURE

018-15. Equipment Required

- Fluke 1722A, 1752A, or 1711A/AA Controller
- System Diagnostic diskette appropriate for Controller - Rev 1.6 (or greater)
- Fluke DMM 8020A or equivalent with at least 1mV resolution
- 1k-ohm or less resistor, any convenient wattage, or a piece of 22AWG wire.
- 1722A/1752A Service Manual, Rev 1991
- 1720A Extender Card, Fluke PN 496752 (Do NOT use 2400A extender, PN 486910)

018-16. Test Guidelines

Throughout the testing procedure the operator is expected to fully understand the use of the System Diagnostic (SD) disk. Upon failure of any portion of these tests, make repairs before continuing.

The troubleshooting hints are intended to give the experienced technician a common starting place for attacking hardware problems. They cannot begin to cover all situations.

WARNING

FIRE, EXPLOSION, AND SEVERE BURN HAZARD EXISTS IF THE LITHIUM BATTERY IS RECHARGED, DISASSEMBLED, HEATED ABOVE 212 DEGREES F (100 C), INCINERATED, OR IF THE BATTERY CONTENTS ARE EXPOSED TO WATER.

CAUTION

Do not contact circuit side of module or the test points with any conductive material (including black foam, shielding bags, other circuit boards, conductive storage boxes, metal shelves, etc). Degradation of battery life and loss of memory contents may occur.

Fluke specifies that a pca stored with batteries installed should first be placed into a pink non-conductive bag (less prone to puncture) and then into a conductive shielding bag.

018-17. Visual Check

Before testing, carefully inspect the option for any obvious problems (solder bridges, opens, or wrong components.)

018-18. Power Supply Resistance Check

Using a DMM, check the resistance between +5V and GROUND (TP4 & TP1 respectively). Verify a resistance of 300 ohms or greater. (For Assy Rev 0 boards, measure between pins 20 and 10 of any of the ICs U1 through U6, or other convenient connection.) Problems may result from a solder bridge or trace short due to contamination or abuse. If the problem is not visible, use a very accurate ohmmeter to determine the point of least resistance.

018-19. Battery Voltage Check

Using a DMM, measure the voltages on each BT1 (TP2) and BT2 (TP3) and +Vm (TP5) to GROUND (TP1). Each should read between 2.25 and 3.7 Volts (new batteries 3.5 to 3.7V). For Assy Rev 0 boards, just measure across pads B+ to B- for the battery connection, and from any memory IC pin 28 to gnd for +Vm.

018-20. Battery Current Drain Check

For Assy Rev A (or above) boards, use a DMM with at least 1-mV resolution to measure the voltages across 1-kilohm resistors R11 and R12. Since U11 automatically draws current from the battery with the highest voltage, one measurement reads a few millivolts, and the other measurement reads near zero. (Each millivolt represents 1 μ A of battery draw through the 1-kilohm resistor.)

For Assy Rev 0 boards, remove the battery. Connect a jumper from the minus battery terminal to board ground. Connect another clip lead from the positive battery terminal to the board B+ pad (or to the end of R7 which

connects to the B+ pad. Using a DMM with at least 1-mV resolution, measure the voltage across R7, a 1K resistor.

Typical draw is 4 to 20 μ A, assuming that the memory chips are near room temperature. Current draw is higher at elevated temperatures. Maximum allowable draw is 30 μ A at room or storage temperature.

If a low battery voltage is detected, the battery may be defective, or there may be an excessive drain on the battery. If the battery voltage is good, but +V_m is low, there may be a problem in the +5 to Battery switch-over circuit or excessive drain from the memory chips. Immediately remove the battery(s) and check the battery(s) under no load; look for a cause of high current drain. On the Assy Rev 0 boards there is no series protection resistor in line with the battery. On Assy Rev A or above boards there is a 1K resistor in series with each battery. Under normal load, this resistor only drops a few millivolts. Under abnormal load, it may drop most of the voltage. The switch-over IC also drops considerable voltage under abnormal load.

Another potential source of increased current draw is excessive leakage from the memory ICs, the battery switch IC, the chip select ICs (U7 and U11 on Rev 0 or U11 and U37 on Rev A), and the format flip-flop (U35). The format flip-flop is the most likely problem source, and the memory chips are the least likely problem sources.

018-21. Battery Replacement

The battery(s) on the board can be changed without loss of data. However, a backup copy of every storage device should always be maintained to recover from the unexpected. Assuming that no trauma has occurred to the battery(s) or board, the battery(s) should last 5 to 10 years. As the battery voltage finally drops, the low battery detection circuit warns the operator of a degraded battery condition either during boot-up or if the battery is checked by the application program. This warning should occur with sufficient life in the battery to prevent loss of board contents.

1. Turn OFF power to the mainframe.
2. Remove the NVRAM board and the battery clamp.
3. For the single battery version, attach a 3.5-Volt source to the B+ and B- pads to maintain power to the memory and U35 during the change. Remove the old battery and install the new battery. Remove the external Voltage source. (Using an external source greater than 3.5 Volts will likely reset the RDY- flag.)

For the dual battery version, check the voltage of both batteries on TP2 and TP3. Starting with the lowest voltage battery, remove and replace the batteries one at a time. If both batteries are removed and then replaced, the RDY- flag will be turned false.

4. Perform "Battery Voltage Check" and "Battery Current Drain Check."

5. Replace the battery clamp.

NOTE

Fluke specifies that a pca with batteries installed first be placed in a pink non-conductive bag (less prone to puncture) and then in a conductive shielding bag.

018-22. System Diagnostics (SD)

018-23. ADDRESS SWITCH TEST

CAUTION

The System Diagnostics (SD) test below will test and destroy the contents of every NVRAM module installed. The test ignores the write protect switch on the board.

Test the address switch with the following procedure:

1. Record the settings of switch SW1 for later use.
2. Set the board as Unit 2, Write Protected, SW1 to 0101 ON-OFF-ON-OFF (position 1234 order).
3. Attach the option to the extender card, and install the set into the test mainframe.
4. Apply power to the test mainframe, and run the System Diagnostics (SD) program.
5. Select TEST ALL INSTALLED NV RAM. Watch the operation to verify that only UNIT 2 is tested and that the SD recognizes the unit as the proper size option.
6. Set the board as unit 5, not Write Protected, SW1 to 1010. Do TEST ALL INSTALLED NV RAM again and verify that only UNIT 5 is tested.
7. Set the board as unit 0, SW1 to 0000 all ON.

018-24. WRITE PROTECT SWITCH TEST

Perform the SD Write Protect Switch test as Unit 0.

The Address and Write Protect Switch tests are somewhat interrelated. The addressing and write protect use S1 and are tested for stuck bits and proper functioning. Address errors might be on the address bus, U31, or S1. The size test looks at the two jumpers JU1 and JU2. The detected size should match the memory configuration. The test does not explicitly check how much memory is installed. It only looks at these two jumpers. It is up to the technician to verify physical memory versus indicated size. Opens or shorts or misconfigured jumpers may cause an indicated difference of size. If the indicated size is less than the actual installed memory, no functional error will occur, but the full available amount of memory will not be accessible. The size jumpers are simply fed to the bus along with write protect as bits on the status register.

Note that the standard NV driver looks for the write protect bit before performing a format or write. But SD ignores this bit and destroys memory contents. The switch does not perform any hardware function on the board to inhibit write access.

Test All Installed NVRAM is the actual memory test for bad bits. Its intention is to diagnose memory IC and data bus problems to the chip or data line level. In reality, it can sometimes do this, but it can become confused by the errors, leading to misdiagnosis. Follow its advise with intelligent caution. In particular, check to make sure that a specified memory IC is located within the Bank containing the error. If they don't match, note the Bank Number specified in the test results and refer to Table 018-4.

A perplexing problem can occur with or without NVRAM modules installed. If anything latches ADACK true (low) during the boot process, the Controller acknowledges the existence of all eight possible NVRAM modules and thinks that any that are not really installed have low batteries.

018-25. LOW BATTERY TEST

1. Remove the battery clamp.
2. Perform the SD Low Battery test as Unit 0. Where SD specifies a 1000-ohm resistor, use a 1-kilohm or smaller resistor (or just a jumper wire.) This small resistance keeps the high impedance +BAT nodes from floating upwards which, after removal of the battery, would falsely indicate a good battery.

On Assy Rev A (or above) boards, perform this test twice, once replacing BT1, and once replacing BT2. While the board is powered and either (or both) battery is low, the Battery Warning LED (CR4) should be lit.

3. Reinstall the battery(s) and battery clamp.

018-26. Memory Retention Test

Format the NV with SD or FUP. Remove external power from the NV board for at least 5 minutes. Restore power to the NV card and do a Scan of NV0: with FUP to verify that data and parity remained intact (ie. FUP, NV0:/S)

018-27. Post-Test Configuration

Return the settings of SW1 to their original positions. If unknown, set SW1 to 0000 (all ON or CLOSED), not write protected, board 0.

Make sure the battery warning decal is legible. If not, apply a new battery warning decal (JF P/N 843193) to the battery clamp. For shelf storage, place the board in a non-conductive pink bag, then place this bag into the conductive shielding bag.

018-28. LIST OF REPLACEABLE PARTS

There are currently three members of the NVRAM module family. Each member is based on the same pca (printed circuit assembly), differing primarily in the size and amount of CMOS static memory installed. Early production of the family utilized a pca which did not accommodate the -020 option, and had one battery. A revised pca (PCA Rev D or Assy Rev A, or greater) added circuitry for the Option -020 (1M-byte) and dual batteries.

Refer to Section 4 of this manual for Option 018/019/020 parts information.

018-29. SCHEMATIC DIAGRAMS

Refer to Section 5 of this manual for Option 018/019/020 schematic diagrams.

Table 018-4. Memory Bank Numbers

BANK NUMBER:	0	1	2	3
256K (17XXA-018)	U100-U107			
512K (17XXA-019)	U100-U107	U110-U117		
1M (17XXA-020)	U100, U101	U102, U103	U104, U105	U106, U107
(U108, U109 are used for Parity on all versions.)				

1722A/1752A-440 Hard Disk

440-1. OVERVIEW

The 1722A/1752A-440 hard disk option provides 40M bytes of file storage. This option consists of two main components: an interface assembly and a hard disk. The component locations of the -440 option are indicated in Figure 440-1. The interface assembly, which is custom made by Virtech Inc., converts the Fluke AGGIE bus to the SCSI (Small Computer Systems Interface) bus, which is required to operate the hard drive. The SCSI hard drive is manufactured by Conner Peripherals and may be one of three models: CP-340, CP-3040, or CP-30060. The interface assembly and the hard drive are not documented as user or Service Center repairable. No schematics or component parts lists are available. Both assemblies are replaceable through the Fluke MEC (Module Exchange Center) program for repair by their respective manufacturers.

The type of hard drive used determines the minimum version of FDOS software and BOOT firmware needed for proper operation. A -440 option with a CP-340 requires FDOS and BOOT 2.0 or higher, a CP-3040 (version SA2.24 or lower) requires FDOS and BOOT 2.1 or higher, a CP-3040 (version SA2.47 or higher), and a CP-30060 requires FDOS and BOOT 2.2 or higher. (The CP-3040 version number can be found printed on the component side of the hard drive pca)

The -440 option can be directly installed into any 1722A or 1752A with serial number 4725013 or greater. Instruments below serial number 4725013 have motherboards that cannot accommodate the SCSI bus; these instruments require installation of a retrofit kit (JF PN 863522).

The interface and hard disk communicate via the SCSI bus connections provided on the motherboard of the mainframe. The interface assembly can be installed in slot 1, 3, 4, 5, or 6, provided that the right-hand 44-pin motherboard connector is installed (card cage viewed from the rear.) (The earliest SCSI compatible motherboards had the con-

nectors installed in slots 1 and 4 only, although the other positions were wired for connectors to be installed.) See the System Guide for additional operating and installation instructions. A separate option (1711A/AA-440) is provided for the 1711A/AA,

The hard disk is located above the power supply, which is shielded by anodized steel. The +5V and +12V power supplies are provided from the motherboard. Termination resistors on the hard drive are powered both by the drive itself and by the SCSI bus. The drive operates as SCSI unit 0, with parity enabled. For use in the -440 option, all four jumpers (E1, E2, E3, and E4) located on the hard drive are normally absent. (Jumper positions for other drive configurations, which are shown for reference only in Table 440-1, are not normally used for the -440 option.)

There are four John Fluke part numbers printed on the interface assembly pca's. PCA's with part number 848890 checked are supported by the MEC program. If any of the other three part numbers are checked, the pca is a special version sold and supported directly by the manufacturer (Virtech Inc.). Such special assemblies cannot be handled by Fluke or the Fluke MEC program; the customer must contact Virtech directly at 603-888-8110 for service information. The extra sockets and connectors on the interface assembly are for such Virtech-supported options and configurations as external SCSI hard drive, CD-ROM, streaming tape drive, and math coprocessor. Contact Virtech for information about these items.

There is an unsupported maintenance feature in FDOS 2.1 and greater which provides for two SCSI drives. The 2nd drive operates as SCSI unit 1. This feature can be used to transfer the entire contents from one drive to the other without using an intermediate storage device. Running CONFIG.FD2 shows extra device names available to your system. When there is more than one device on the SCSI bus, only the most distant device can have terminators. Terminators for all devices in between must be removed.

440-2. LIST OF REPLACEABLE PARTS

Refer to Section 4 of this manual for 1722A-440 option parts list information.

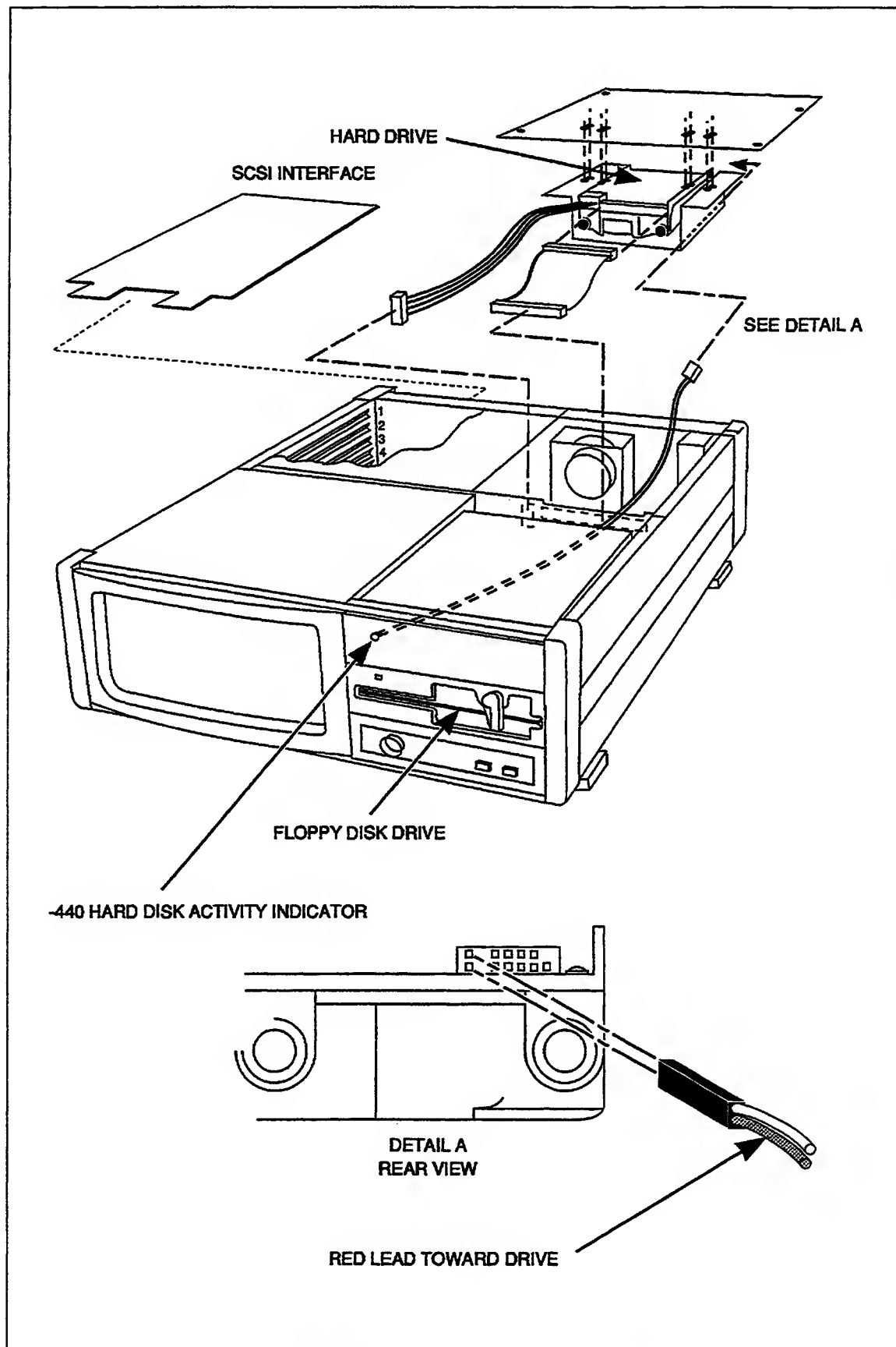


Figure 440-1. 1722A/1752A-440 Hard Disk

Table 440-1. Jumper Positions

Jumper	CP-340	CP-3040/CP-30060
E1	parity-	addr 1
E2	addr 1	addr 2
E3	addr 2	addr 4
E4	addr 4	parity- (Note 1)
Note 1: Jumper E4 does not exist on the CP-30060. Parity is always enabled.		

Section 7
Appendices

APPENDICES	TITLE	PAGE
A.	Glossary	A-1
B.	IEEE-488 Reference	B-1
C.	RS-232-C Reference	C-1

Appendix A

Glossary

16/24-

Abbreviation for 16-line/24-line raster selection signal. 24-line is not included in standard support on the 1722A.

ABORT

ABORT PROGRAM INPUT signal. Aborts applications programs.

ADACK-

ADDRESS ACKNOWLEDGE signal. An ARGUS bus signal that is sent to the Microprocessor. Driven low by the selected device.

ADVAL-

ADDRESS VALID signal. An ARGUS bus signal which is driven low by the Microprocessor when an ARGUS memory or parallel I/O bus cycle occurs.

AGGIE

A major system bus with 22 address lines, 16 data lines, and four control lines. Eighteen of the address lines are shared with the ARGUS bus.

AGGIE-

One of three signals (AGGIE, ARGUS-, and CRU-) used to select the AGGIE and ARGUS busses for I/O. The AGGIE- signal selects AGGIE memory devices with the AGVAL- signal.

AGVAL-

ADDRESS ON AGGIE BUS VALID signal. An AGGIE bus signal which is driven low by the Microprocessor when AGGIE memory or parallel I/O bus cycle occurs.

ALATCH

ADDRESS LATCH signal. Pulses high when address information is valid on the address/data bus.

APP-

ATTACHED PROCESSOR PRESENT signal. Used to coordinate execution with a co-processor.

ARGUS

A major system bus with 18 address lines, 16 data lines, and two control lines. The 18 address lines are shared with the AGGIE bus.

ARGUS-

One of three signals (AGGIE, ARGUS-, and CRU-) used to select the AGGIE and ARGUS busses for I/O. The ARGUS- signal selects ARGUS memory devices with the ADVAL- signal.

ATTREN

ATTRIBUTE ENABLE signal.

Attribute

A modification of one or more of the basic characters seen on the CRT.

ATTRRD

ATTRIBUTE READ signal.

ATTRWT-

ATTRIBUTE WRITE signal.

GLOSSARY

AUMS

Internal arithmetic, a logical unit operation or macrostore access. MPLICK is inactive.

AUMSL

Internal arithmetic, a logical unit operation or macrostore access. MPLICK is asserted.

BEEP

The control signal for the beeper on the VGK board.

BLCLK

BLINK CLOCK signal.

BMODE

BYTE MODE signal. Used with AD00 for byte addressing.

BST1

BUS STATUS LINE 1.

BST2

BUS STATUS LINE 2.

BST3

BUS STATUS LINE 3.

BUSWR-

BUS WRITE signal. When low, indicates the CPU is writing data.

C/R-

Graphics pixel address select signal.

CAPS

The control signal for the capital letter mode from the keyboard.

CAS-

COLUMN ADDRESS STROBE signal.

CCLK-

CHARACTER CLOCK signal.

CCW

Counterclockwise.

CD

CARRIER DETECT signal.

CDCLK

CHARACTER DOT CLOCK signal.

CE

Chip enable.

CHEN

CHARACTER DISPLAY ENABLE signal.

CHREN-

CHARACTER I/O SELECT signal.

CHR I/O

CHARACTER I/O memory address select.

CHRRD-

CHARACTER MEMORY READ ENABLE signal.

CHRWR-

CHARACTER MEMORY WRITE ENABLE signal.

CKLOUT

CLOCK OUT timing signal.

CLRA-

CLEAR SLOPE ACCUMULATOR signal.

CLWR-

VECTOR GENERATOR COUNT ENABLE signal.

CPU

Central processing unit.

CRACK-

COMMUNICATIONS REGISTER ACKNOWLEDGE signal. When a communications register bit is addressed, the device selected must respond with this signal.

CRCLK-

COMMUNICATIONS REGISTER UNIT CLOCK. A signal used to latch data into a device register.

CRIN

CRU INPUT signal.

CROMRD-

CHARACTER ROM LATCH READ ENABLE signal.

CROUT

CRU OUTPUT signal.

CRTC

Cathode ray tube controller.

CRTCEN-

CRT CONTROLLER ENABLE signal.

CRTCRDY

CRT CONTROLLER READY signal.

CRTCST-

CRT CONTROLLER RESET signal.

CRU

Communications Register Unit. An area of memory reserved as a register for control of devices or for other uses. See TI 9900 literature for complete discussion.

CRU-

One of three signals (AGGIE-, ARGUS-, and CRU-) used to select the AGGIE and ARGUS busses for I/O. The CRU- signal selects CRU I/O or memory-mapped I/O on the ARGUS bus.

CRU space

Memory space defined as a Communications Register Unit. Devices addressed in the Communications Register Unit in memory are said to exist in that processor's CRU space.

CRUACK

COMMUNICATIONS REGISTER UNIT ACKNOWLEDGE, the acknowledge signal sent back to the Microprocessor by memory addressed as a COMMUNICATIONS REGISTER UNIT.

CRUCLK

COMMUNICATIONS REGISTER UNIT CLOCK signal.

CRUIN

CRU INPUT DATA signal.

ST8/D15/CRUOUT

Memory mapper enable bit, the least significant data bit and output signal for serial CRU I/O operations.

CSYNC

COMPOSITE SYNCHRONIZATION signal.

CTRL

CONTROL signal from the control key on the keyboard.

CTRL1-

CONTROL REGISTER 1 ENABLE signal.

CTRL2-

CONTROL REGISTER 2 ENABLE signal.

CTS

CLEAR TO SEND signal.

CUR2

DELAYED CURSOR signal.

CURLAT

CURSOR LATCH signal.

CVID

CHARACTER VIDEO signal.

DBIN-

DATA BUS IN (READ) signal.

DBLSZ

DOUBLE SIZE signal.

DCLK

DOT CLOCK signal.

DCOK

DC POWER OK signal. Also used as system RESET.

DE1

DISPLAY ENABLE 1 signal.

DE2

DISPLAY ENABLE 2 signal.

GLOSSARY

DEN-

DATA ENABLE, a control signal that is pulsed low when data may be placed on the address/data bus.

DIN

DATA INPUT signal.

DOUT

DATA OUTPUT signal.

DSI

Dual Serial Interface.

DSR

DATA SET READY signal.

DTR

DATA TERMINAL READY signal.

EPROM

Erasable programmable memory.

EVEN-

Selects even data byte for transfer.

FDOS

Fluke Disk Operating System.

FROMKB

FROM KEYBOARD signal.

GDOTRD-

GRAPHICS DOT READ ENABLE signal.

GDOTWR-

GRAPHICS DOT WRITE ENABLE signal.

GLOAD-

GRAPHICS DATA LOAD ENABLE signal.

GND

Chassis ground.

GREN

GRAPHICS DISPLAY ENABLE signal.

GRIN

BUS GRANT INPUT signal. Input for granting bus control.

GROUT

BUS GRANT OUTPUT signal. Output for granting bus control.

GVID

GRAPHICS VIDEO signal.

HALT

HALT signal. Used for debugging.

HCTS-

HOST CLEAR TO SEND signal from the VGK to the Single-Board Computer.

HIGHT

HIGHLIGHT signal. Greater than normal intensity.

HOLDA-

When low, this signal grants control of memory to a DMA (direct memory access) device.

HRIN

HOST RECEIVE DATA IN signal to the Single-Board Computer to the VGK.

HSYNC

Horizontal synchronization pulse.

HXOUT

HOST XMT DATA OUT signal from the Single-Board Computer to the VGK.

IC0-IC3

IC0 (MSB), IC1, IC2, and IC3 (LSB) are interrupt priority codes, four bits that can define 16 interrupt priority levels. When INTREQ- is low, IC0-IC3 indicate what level interrupt request is active. IC0-IC3 are all low for the highest interrupt level, and are all high for the lowest interrupt level.

INHIBIT

INHIBIT for refresh signal.

INTREQ

INTERRUPT REQUEST signal. When low, indicates that there is an interrupt in process.

KBRD

KEYBOARD READ signal.

LCOM

LOGIC COMMON.

LED

Light emitting diode.

LEDWR-

LED LATCH WRITE ENABLE signal.

M1

Selects type of access to graphics memory.

M2

Selects type of access to graphics memory.

MEM-

MEMORY CYCLE signal. When low, indicates that a memory cycle is taking place.

MEMEN

MEMORY ENABLE signal.

MEMSTB

MEMORY STROBE signal.

MERR

MEMORY REGISTER RESERVED signal. Driven active if illegal address is written. Causes a level 2 interrupt.

MHWR-

Slope accumulator high-byte enable.

MID

MACROINSTRUCTION DETECTED, a bus status code sent by the Microprocessor.

MLWR-

Slope accumulator low-byte enable.

MODE

Describes the combined effect of M1/M2 signals. The modes are NEW, OR, AND, and XOR.

MUX

Multiplex.

NMI

Non-maskable interrupt. When pulsed low, always causes the CPU to perform the NMI interrupt service routine.

ODD-

Selects Odd data byte.

OSK

OSK 0-9 OVERLAY SCAN

OTHER

CRU I/O decode signal. Occurs when non-memory or non-I/O cycle is detected.

PAL

Programmable Array Logic, a fuse-programmed device that replaces discrete logic devices such as AND gates, OR gates, flip flops, and counters. A single 20-pin PAL can replace from four to 12 TTL logic packages.

PANYWR-

PAN Y REGISTER ENABLE signal.

PANXWR-

PAN X REGISTER ENABLE signal.

PCLK

PIXEL CLOCK signal.

PEIN

PARITY EVEN-BYTE INPUT signal.

PEOUT

PARITY EVEN-BYTE OUTPUT signal.

PEVEN-

PARITY EVEN error signal.

PG MODE

PAGE MODE.

PIN

PIXEL IN signal.

PODD-

PARITY ODD error signal.

POIN

PARITY ODD-BYTE INPUT signal.

GLOSSARY

POUT

PARITY ODD-BYTE OUTPUT signal.

PROM

Programmable read-only memory.

PSK

PSK 0-3, programmer's keyboard select.

R/W

READ/WRITE signal. High during read, low during write.

RAM

Random access read-write memory.

RAMAD-

RAM ADDRESSED signal.

RAMSEL

RAM SELECT signal.

RAS-

ROW ADDRESS SELECT signal.

RAMTRIG

RAM TRIGGER signal. Used to initiate DRAM access cycle.

RBW

READ BEFORE WRITE.

RDY

READY signal. Used to add wait states during memory and I/O operations.

REC

RECEIVED DATA signal.

RESET

BUS STATUS CODE signal. When active low, this signal resets the Microprocessor.

RET

Signal (logic) ground.

REV

REVERSE VIDEO.

RFRRAS

REFRESH ROW ADDRESS STROBE.

RFRRAS-

REFRESH RAS signal.

RINT

REQUEST INTERRUPT signal.

ROM

Read-only memory.

ROW

ROW ADDRESS OUTPUT signal.

RQIN

REQUEST IN signal.

RQOUT

REQUEST OUT signal.

RAS-

ROW ADDRESS STROBE signal.

RTS

READY TO SEND signal.

SBC

Single-Board Computer.

SELCOL

SELECT COLUMN signal.

SHIFT

Signal from shift key on keyboard.

SRLSD

SECONDARY RECEIVE LINE SIGNAL DETECT.

SRTS

SECONDARY REQUEST TO SEND signal.

ST

STATUS REGISTER UPDATE, a bus status code.

STATAD-

STATUS ADDRESS signal, for error status decoding.

SYNC-

CLOCK signal.

SYS-

Output of CRU I/O Decoder. Selects Error Interrupt PAL on SBC.

STATRD-

STATUS READ ENABLE signal.

TOKB

TO KEYBOARD signal.

TSO

Touch-Sensitive Overlay, a touch-sensitive keypad which is laid over the screen, and in addition to the keyboard, serves as an alternate means of controlling the 1722A.

TTL Logic

Transistor to transistor logic.

UART

Universal Asynchronous Receiver Transmitter.

UNDER1

DELAYED UNDERLINE ATTRIBUTE signal.

UNDER2

DELAYED UNDERLINE ATTRIBUTE signal.

VBUSY

VECTOR GENERATING HARDWARE BUSY signal.

VCC

DC power source.

VCLK

GRAPHICS REFRESH CLOCK signal.

VSS

Ground reference.

VSNC

VERTICAL SYNCHRONIZATION pulse.

WBOOT

WARM BOOT signal.

WE-

WRITE ENABLE signal.

WE/CRCLK

WRITE ENABLE CRU CLOCK signal.

WERR

WRITE ERROR. Write protects reserved register in memory. Causes a Level-2 interrupt if the Microprocessor is writing to memory.

WP

WORKSPACE POINTER UPDATE, a bus status code sent by the Microprocessor.

X-PAN

Locates X-axis of display window in graphics memory.

XHWR-

X-AXIS (HIGH BYTE) COORDINATE ENABLE signal.

XLWE-

X-AXIS (LOW BYTE) COORDINATE ENABLE signal.

XMT

TRANSMITTED DATA signal.

XUP

INCREMENT X-AXIS VECTOR GENERATOR.

XY TRAN

X-Y AXIS TRANSPOSE.

Y-PAN

Locates Y-axis of display window in graphics memory.

YLWR-

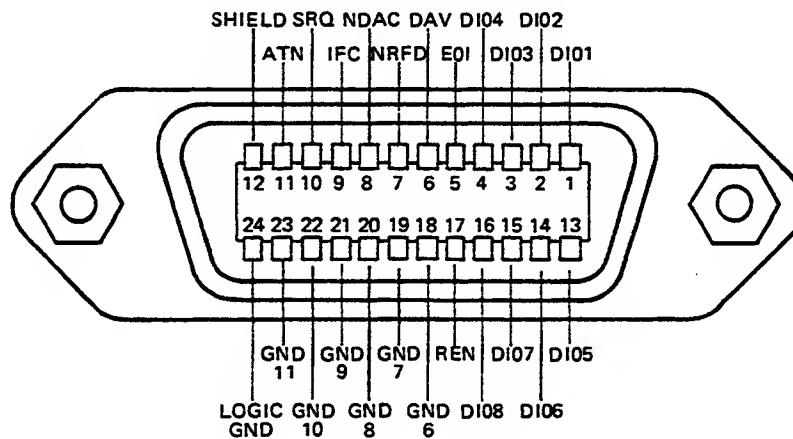
Y-AXIS (LOW BYTE) COORDINATE WRITE ENABLE signal.

YUP

INCREMENT Y-AXIS VECTOR GENERATOR.

Appendix B IEEE-488 Reference

IEEE-488-1978 Instrument Ports (Port 0 and Port 1)



BUS	PIN	SIGNAL	DEFINITION
DATA BUS	1	DI01	Data input and output lines, bidirectional and active-low, DI08 is most significant. Data transfers are 8-bit parallel and byte serial.
	2	DI02	
	3	DI03	
	4	DI04	
	13	DI05	
	14	DI06	
	15	DI07	
	16	DI08	
MANAGEMENT BUS	11 23	ATN ATN Return	Attention. Activated by the 1722A when peripheral devices are being assigned as listeners and talkers. The 1722A assumes it is the only source of this signal.
	10 22	SRQ SRQ Return	Service request. Any peripheral device on the Instrument Bus can request the attention of the 1722A Controller by setting SRQ active low.

IEEE-488 REFERENCE

IEEE-488-1978 Instrument Ports (Port 0 and Port 1) (cont)

BUS	PIN	SIGNAL	DEFINITION
MANAGEMENT BUS (cont)	9 21	IFC IFC Return	Interface clear. Set by the 1722A to place all instruments on the bus in a predetermined reset state. The 1722A assumes that it is the only source of this signal.
	17	REN	Remote enable. Causes all responding instruments on the Bus to ignore their front panel controls and operate under remote control via signals and control messages received over the Bus.
	5	EOI	End or identify. Can be used by a talker to identify the end of a data transfer sequence, or with ATN by a Controller, to execute a polling sequence.
TRANSFER BUS	7 19	NRFD NRFD Return	Not ready for data. An active low signal line to indicate that one or more assigned listeners are not ready to receive the next data byte. When all of the assigned listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. The talker can then place the next data byte on the Data Bus.
	6 18	DAV DAV Return	Data valid. Activated by the talker shortly after placing a valid data byte on the Data Bus. An active low DAV signal tells each listener to capture the data byte presently on the Data Bus. The talker should be inhibited from activating DAV when NRFD is active low.
	8 20	NDAC NDAC Return	Not data accepted. Held active low by each listener until the listener captures the data byte currently being transmitted over the Data Bus. When all listeners have captured the data byte, NDAC goes inactive high. This tells the talker the transfer is complete.

ASCII and IEEE-488 Mnemonic Abbreviations

ACK	Acknowledge	MSA	My Secondary Address
ASCII	American Standard Code for Information Interchange	MTA	My Talk Address
ATN	Attention	NAK	Negative Acknowledge
BEL	Bell	NDAC	Not Data Accepted
BS	Backspace	NRFD	Not Ready For Data
CAN	Cancel	NUL	Null
CR	Carriage Return	OSA	Other Secondary Address
DCL	Device Clear	OTA	Other Talk Address
DCn	Device Control 1, 2, 3, or 4	PCG	Primary Command Group
DEL	Delete	PPC	Parallel Poll Configure
DION	Data Input/Output 1 through 8	PPD	Parallel Poll Disable
DLE	Data Link Escape	PPE	Parallel Poll Enable
ENQ	Enquiry	PPRn	Parallel Poll Response 1 through 8
EOF	End of File	PPU	Parallel Poll Unconfigure
EOI	End or Identify	REN	Remote Enable
EOT	End of Transmission	RS	Record Separator
ESC	Escape	SDC	Selected Device Clear
ETB	End of Transmission Block	SI	Shift In
ETX	End of Text	SO	Shift Out
FF	Form Feed	SOH	Start of Heading
GET	Group Execute Trigger	SP	Space
GND	Ground	SPD	Serial Poll Disable
GTL	Go To Local	SPE	Serial Poll Enable
HT	Horizontal Tab	SRQ	Service Request
IEEE	Institute of Electrical and Electronic Engineers	STB	Status Byte
IFC	Interface Clear	STX	Start of Text
LF	Line Feed	TCT	Take Control
LLO	Local Lockout	UNL	Unlisten
MLA	My Listen Address	UNT	Untalk
		US	Unit Separator



ASCII & IEEE-488 BUS CODES

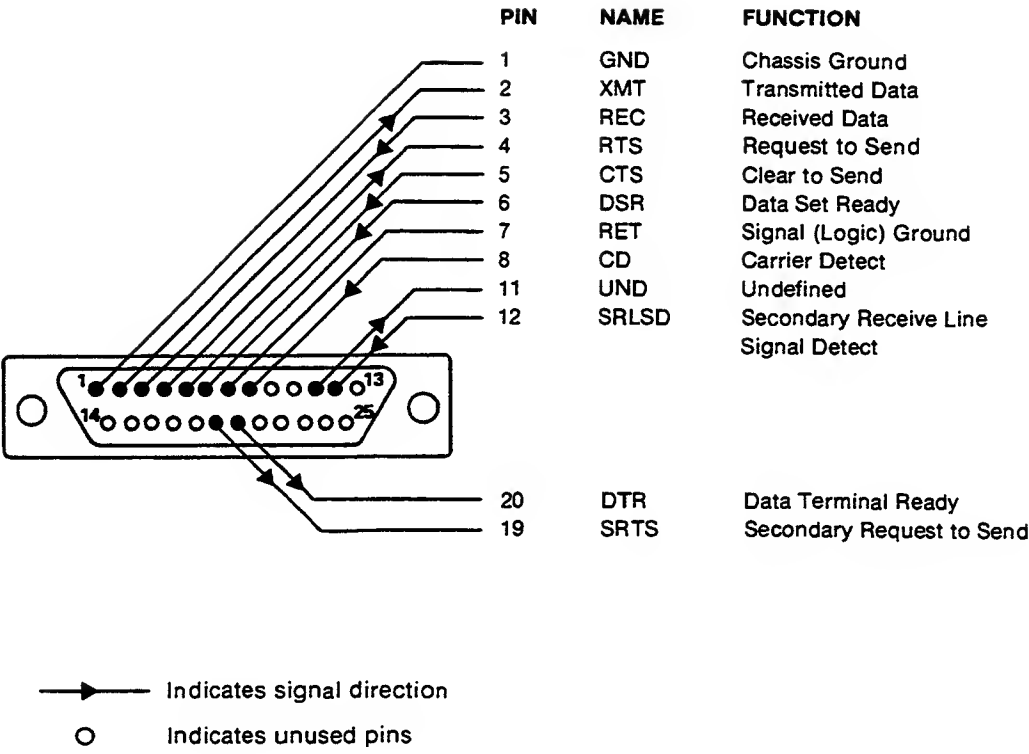
B ⁷ B ⁶ B ⁵ BITS B ³ B ² B ¹ B ⁰	0 0 0 0		0 0 0 1		0 0 1 0		0 0 1 1		0 1 0 0		0 1 0 1		0 1 1 0		0 1 1 1		2 ⁷ 2 ⁶ 2 ⁵ 2 ⁴
	CONTROL				NUMBERS SYMBOLS				UPPER CASE				LOWER CASE				
0 0 0 0	0 NUL NUL	16 ρ DLE	32 SP SPACE MLA0	48 0 MLA16	64 @ MTA0	80 P MTA16	96 ' MSA0	112 p MSA16									
0 0 0 1	1 β SOH GTL	17 σ DC1	33 ! MLA 1	49 1 MLA17	65 A MTA1	81 Q MTA17	97 a MSA1	113 q MSA17									
0 0 1 0	2 γ STX	18 τ DC2	34 " MLA2	50 2 MLA18	66 B MTA2	82 R MTA18	98 b MSA2	114 r MSA18									
0 0 1 1	3 δ ETX	19 υ DC3	35 # MLA3	51 3 MLA19	67 C MTA3	83 S MTA19	99 c MSA3	115 s MSA19									
0 1 0 0	4 ε EOT SDC	20 φ DC4 DCL	36 \$ MLA4	52 4 MLA20	68 D MTA4	84 T MTA20	100 d MSA4	116 t MSA20									
0 1 0 1	5 ζ ENQ PPC	21 χ NAK PPU	37 % MLA5	53 5 MLA21	69 E MTA5	85 U MTA21	101 e MSA5	117 u MSA21									
0 1 1 0	6 η ACK	22 ψ SYN	38 & MLA6	54 6 MLA22	70 F MTA6	86 V MTA22	102 f MSA6	118 v MSA22									
0 1 1 1	7 BEL BEL	23 ω ETB	39 ' MLA7	55 7 MLA23	71 G MTA7	87 W MTA23	103 g MSA7	119 w MSA23									
1 0 0 0	8 BS BS GET	24 Ω CAN SPE	40 (MLA8	56 8 MLA24	72 H MTA8	88 X MTA24	104 h MSA8	120 x MSA24									
1 0 0 1	9 HT HT TCT	25 √ EM SPD	41) MLA9	57 9 MLA25	73 I MTA9	89 Y MTA25	105 i MSA9	121 y MSA25									
1 0 1 0	10 LF LF	26 → SUB	42 * MLA10	58 : MLA26	74 J MTA10	90 Z MTA26	106 j MSA10	122 z MSA26									
1 0 1 1	11 VT VT	27 ESC ESC	43 + MLA11	59 ; MLA27	75 K MTA11	91 [MTA27	107 k MSA11	123 { MSA27									
1 1 0 0	12 FF FF	28 ↑ FS	44 , MLA12	60 < MLA28	76 L MTA12	92 \ MTA28	108 l MSA12	124 ! MSA28									
1 1 0 1	13 CR CR	29 ÷ GS	45 - MLA13	61 = MLA29	77 M MTA13	93] MTA29	109 m MSA13	125 } MSA29									
1 1 1 0	14 SO SO	30 Σ RS	46 . MLA14	62 > MLA30	78 N MTA14	94 ^ MTA30	110 n MSA14	126 ~ MSA30									
1 1 1 1	15 SI SI	31 ≈ US	47 / MLA15	63 ? UNL	79 O MTA15	95 — UNT	111 o MSA15	127 ■ RUB-OUT MSA31									
2 ³ 2 ² 2 ¹ 2 ⁰	ADDRESSED UNIVERSAL COMMANDS COMMANDS				LISTEN ADDRESSES				TALK ADDRESSES				SECONDARY ADDRESSES OR COMMANDS				

KEY

decimal 38 & 26 hex 1722A DISPLAY
ASCII & MLA6 IEEE-488

Appendix C

RS-232 Reference



RS-232 CONNECTOR REAR PANEL VIEW

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Section 9 1722A/1752A OEM Assembly

Contents

The following assemblies are used with newer versions of the 1722A/1752A and are documented in this section:

Floppy Disk Drive	(Panasonic JU455-8)
Power Supply	(Computer Products XL 200)
Video Kit	(Data Ray 1059)

Other assemblies were used in earlier versions of the 1722A/1752A and are documented in a separate manual (Fluke Part Number 919969). These assemblies include the following:

Floppy Disk Drives	(NEC) (Shugart SA450) (TEAC FD55)
Power Supplies	(NPT) (Computer Products XL160)
Video Kits	(Ball 12V Video) (Dotronix R.D.O.)

Floppy Disk Drive

Panasonic JU455-8

Application Manual

Flexible Disk Storage Drive

JU-455-8

Revision-1

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SECTION I INTRODUCTION

1.1 GENERAL DESCRIPTION

The JU-455-8 is a 5.25 inch half height double-sided, double density mini floppy diskette drive designed for applications which require the combined benefits of compact size, high performance and low power consumption.

The JU-455-8 offers the same basic performance as its predecessors in the JU-455 series. Significant improvements in the reliability and efficiency have been made by integrating the circuits and reducing the number of individual components.

The JU-455-8 contains lead screw actuator, a DC direct drive spindle motor, bicompliant read/write heads, a track zero detector, a write protect detector an index detector, read/write electronics and motor speed control electronics.

Typical application for the JU-455-8 are: word processing systems, entry level micro processor systems, intelligent calculators, storage oscilloscope analyzers, musical synthesizers requiring large memory backup, certifier applications, disk duplicator systems, computer systems and other applications where low cost random access data storage is required.

Key Features:

- Compact size
- 0.5 Mbyte storage capacity (unformatted)
- 4 ms track to track access time
- Brushless DC direct drive motor
- Low power consumption
- 10,000 hours MTBF
- 125/250 Kbits / transfer rate

1.2 SPECIFICATION SUMMARY

1.2.1 Performance Specifications

Capacity (in bytes)	Single Density (FM)	Double Density (MFM)
Unformatted		
Per Disk	250,000	500,000
Per Surface	125,000	250,000
Per Track	3,125	6,250
Formatted (16 Sectors/Track)		
Per Disk	163,840	327,680
Per Track	2,048	4,096
Per Sector	128	256
Formatted (10 Sectors/Track)		
Per Disk	204,800	409,600
Per Track	2,560	5,120
Per Sector	256	512
Transfer Rate	125 kbits/sec	250 kbits/sec
Latency (avg.)	100 msec	100 msec
Access Time		
Track to Track	4 msec	4 msec
Average	53 msec	53 msec
Settling Time	15 msec	15 msec
Motor Start Time	500 msec	500 msec

1.2.2 Functional Specifications

	Single Density 300 rpm	Double Density 300 rpm
Rotational Speed		
Recording Density (Track 39, side 1)	2,938 bpi	5,876 bpi
Flux Density (Track 39, side 1)	5,876 fci	5,876 fci
Track Density	48 tpi	48 tpi
Cylinders	40	40
Tracks	80	80
Read/Write Heads	2	2
Encoding Method	FM	MFM
Media Requirements	Double sided / Double Density / ANSI SPEC	

1.2.3. Reliability Specifications

M.T.B.F.	10,000 POH
M.T.T.R.	30 minutes
Component life	15,000 POH or 5 years
Error Rates	
Soft Error Rate	1 per 10 ⁹ bits read
Hard Error Rate	1 per 10 ¹² bits read
Seek Error	1 per 10 ⁶ seeks
Media Life	
Number of Passes per Track	3.5 × 10 ⁶
Number of Media Clamp	3.0 × 10 ⁴

1.2.4 Physical Specifications

	Shipping	Storage	Operating
Environmental Limits			
Ambient Temperature	-40 to 144°F (-40 to 62.2°C)	-8 to 131°F (-22.2 to 55°C)	41 to 115°F (5 to 46.1°C)
Relative Humidity	1 to 95% RH	1 to 95% RH	20 to 80% RH
Max. Wet Bulb Temp.	No-Condensing	No-Condensing	85°F (29.4°C)
Vibration	≤ 5G (5-55 Hz)	≤ 5G (5-55 Hz)	≤ 0.5G (5-55 Hz)
Shock	≤ 40G - 10msec	≤ 40G - 10msec	≤ 0.5G - 10msec
Mechanical Dimension: (excluding front plate)			
Width =	5.75 ± 0.02 Inches (146.0 ± 0.5mm)		
Height =	1.65 Inches (41.8mm) Max.		
Depth =	7.95 Inches (202mm) Max.		
Mechanical Dimension: (including front plate)			
Width =	5.88 ± 0.02 Inches (149.4 ± 0.5mm)		
Height =	1.63 ± 0.02 Inches (41.5 ± 0.5mm)		
Depth =	8.15 Inches (207.0mm) Max.		
Weight =	2.87 pounds (1.3kg)		

1.2.5 Power Requirements

Item			Rating		
Power requirement	12 VDC	Voltage	12 V \pm 10% Max Ripple 100 mVp-p		
		Current	During operating	Seek	0.55 A (Max) 0.32 A (Typ)
				Read	0.21 A (Max) 0.17 A (Typ)
				Write	0.23 A (Max) 0.19 A (Typ)
			At motor start	0.90 A (Max.) 0.70 A (Typ.)	
	5 VDC	Voltage	5 V \pm 5% Max Ripple 50 mVp-p		
		Current	During operating	Seek	0.34 A(Max) 0.28 A(Typ)
				Read	0.45 A(Max) 0.37 A(Typ)
				Write	0.47 A(Max) 0.38 A(Typ)
	Power consumption		Seek	9.05 W(Max) 5.24 W(Typ)	
			Read	5.13 W(Max) 3.89 W(Typ)	
			Write	5.50 W(Max) 4.18 W(Typ)	
			Stand by	2.00 W(Max) 1.47 W(Typ)	

Note : Calculation Method Power Consumption :
Our voltage specification is subject to 12VDC \pm 10% accordingly, in case of calculating maximum figure, it becomes larger than that of the competitor's by \pm 5%
"Stand by mode" states all input signals "off".

- Note :
1. At motor start : Up to 500 ms after motor start
 2. Seek : For seeking after 500 ms subsequent to motor start
 3. Power requirements represent the values in the case where a media with a media load of 100 g-cm is used.
 4. Peak currents are as specified in figures 2-3.

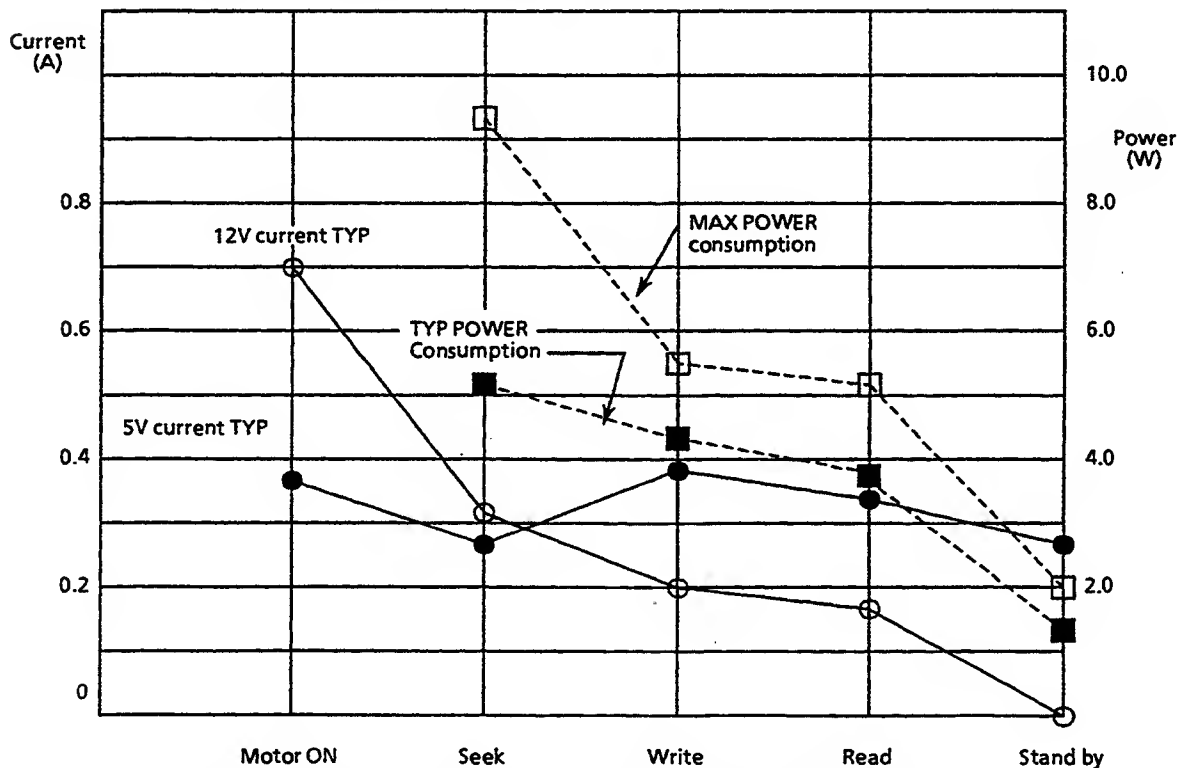


Figure 1 - 1 D.C POWER PROFILE OF POWER CONSUMPTION

1.3 FUNCTIONAL CHARACTERISTICS

The JU-455-8 Consists of read/write and control electronics, drive mechanism, read/write heads, and precision track position mechanism. These components perform the following functions:

- a. Interpret and generate control signals.
- b. Move read/write heads to the desired track.
- c. Read and write data.

The interface signals and their relationship to the internal functions are shown in figure 1-2.

1.3.1 Read/Write Control Electronics

The electronics package contains:

- a. Index detector circuits
- b. Head positioning driver circuits
- c. Read/Write amplifier and transition detector
- d. Write Protect detector
- e. Drive select circuit
- f. Drive motor control circuit
- g. Track ØØ detector

1.3.2 Drive Mechanism

The DC drive motor under servo speed control (using a frequency generator) rotates the spindle motor at 300 rpm through a direct drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange.

1.3.3 Positioning Mechanics

The read/write head assembly is accurately positioned through the use of a leading screw which is attached to the head carriage assembly. Precise track location is accomplished as the head carriage is moved by the precise discrete rotation of a stepper motor.

1.3.4 Read/Write Heads

The proprietary heads are a single element ceramic read/write head with tunnel erase elements to provide erased areas between the data tracks. Thus, normal interchange tolerances between media and drives will not degrade the signal to noise ratio, ensuring diskette interchange.

The heads are mounted on a carriage which is located on precision guide rods. The diskette is held in a plane perpendicular to the read/write heads by a platen located on the base casting. This precise registration assures perfect compliance with the read/write heads. The read/write heads are in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette with minimum head/diskette wear.

1.3.5 Recording Formats

The formats of the data written on the diskette are totally a function of the host system. The formats can be designed around the users application (FM or MFM) to take complete advantage of the total available bits that can be written on any one track.

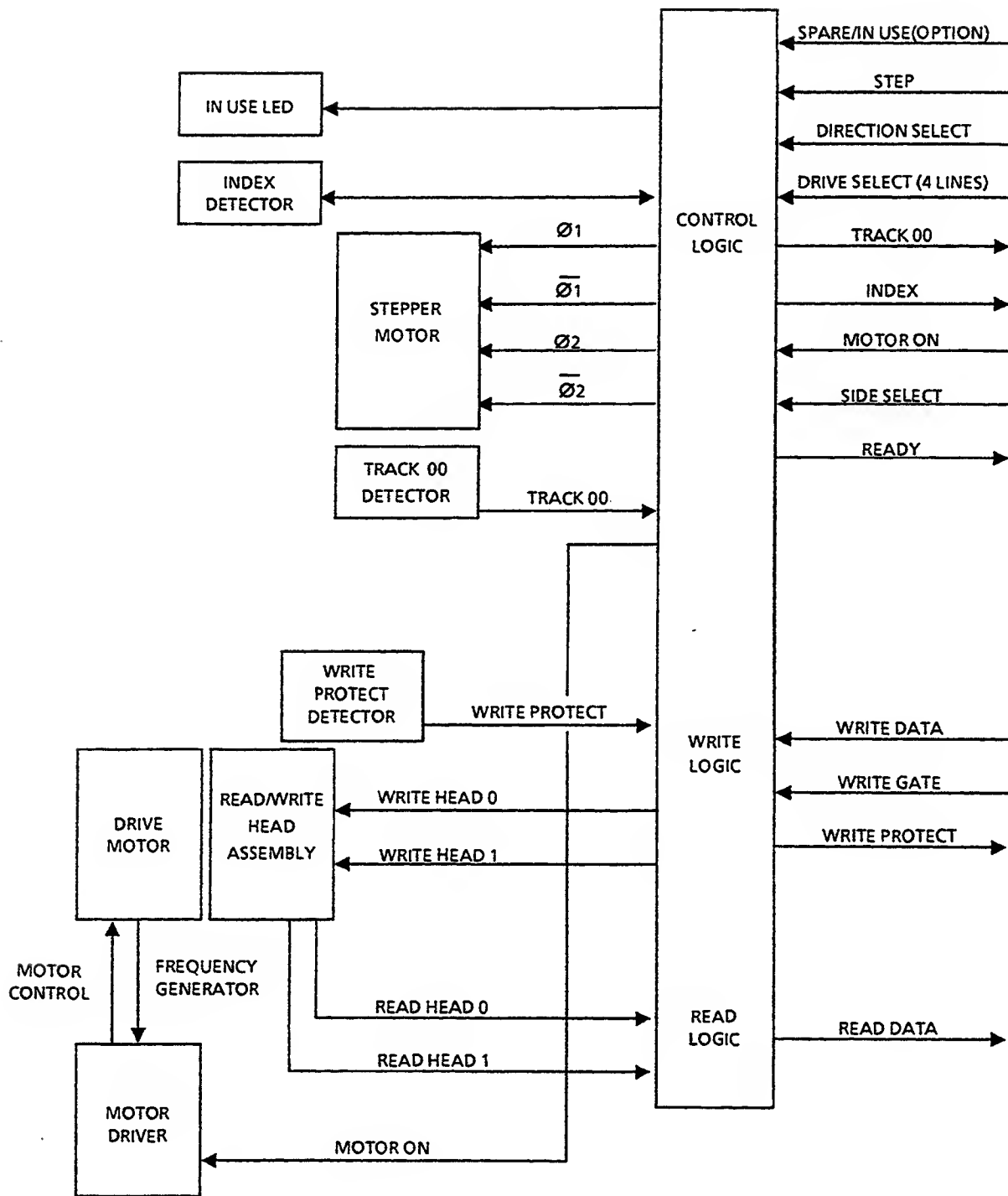


FIGURE 1-2 FUNCTIONAL DIAGRAM

SECTION II ELECTRICAL INTERFACE

The following section provides the electrical definition for each line. Figure 2-1 shows all of the interface connections with respect to the host system.

The signal interface consists of the following two categories:

- a. Control Lines
- b. Data Transfer Lines

All lines in the signal interface are digital in nature and either provides signals to the drive (input), or provide signals to the host (output), by way of the interface connector J1.

The DC power connector, J2, provides + 5V DC and + 12V DC power.

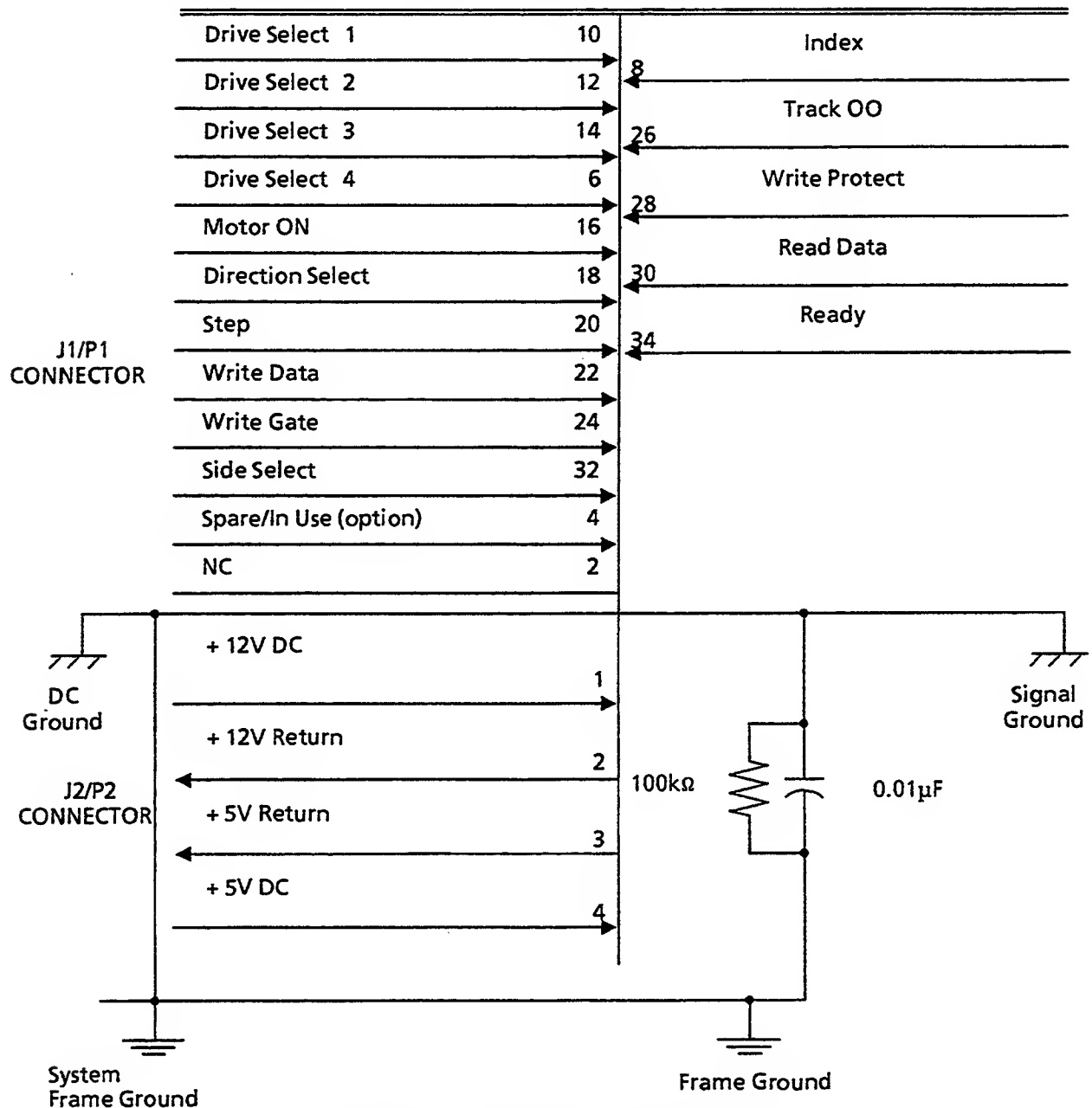


FIGURE 2 - 1 INTERFACE CONNECTION

2.1 SIGNAL INTERFACE

The JU-455-8 uses the industry standard open collector, low level - true, multiplexed interface convention. The industry standard open-collector, 40 milliamperere TTL driver 7438 or equivalent, is used to transmit the I/O signals. The transmitted signals are detected by the hysteresis input inverter, 7414 or equivalent. A 150Ω pull-up resistor between the signal line and +5 volts is necessary on the receiving circuit. The input of each receiver is terminated through a 150Ω resistor.

When using two or more drives on a daisy chain, remove all plug jumper "TM" except for last drive on daisy chain.

The input signal lines which are not multiplexed are MOTOR ON and IN USE. The input/output lines have the following electrical specifications. See Figure 2-2 for the recommended circuits.

(input signal lines)

True = Logical zero = $V_{in} = +0.0$ to $+0.5$ Volts

False = Logical one = $V_{in} = +2.0$ to 5.25 Volts

(output signal lines)

True = Logical zero = $V_{out} = +0.0$ to $+0.4$ Volts

False = Logical one = $V_{out} = +2.4$ to 5.25 Volts

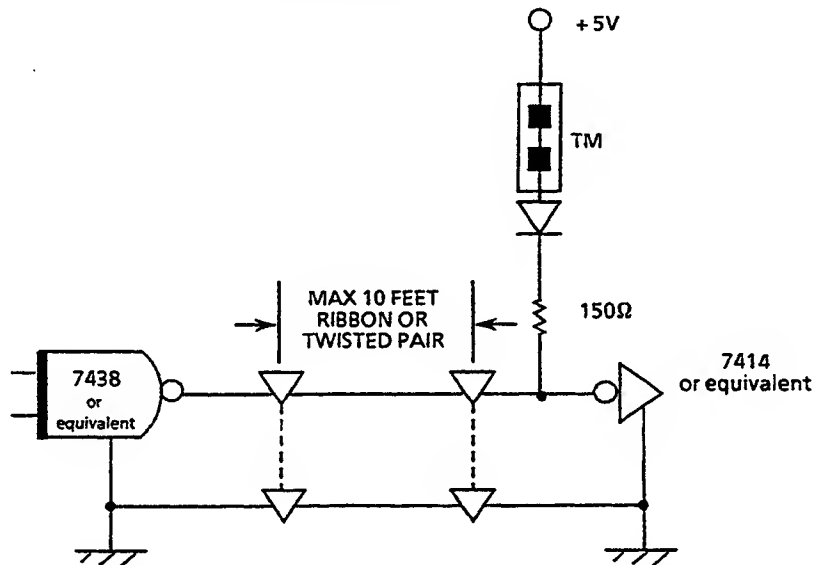


FIGURE 2-2 INTERFACE SIGNAL DRIVER/RECEIVER

2.2 INPUT LINES

There are twelve active low TTL input lines to the JU-455-8 drive. Individual signal line characteristics are described below.

2.2.1 Drive Select 1, 2, 3, or 4 (J1 Pins #10, 12, 14, and 6)

Four separate input lines, drive select 1, drive select 2, drive select 3, and drive select 4 are provided so that in standard configuration (jumper MX. open) up to four drives may be multiplexed together in a system that have separate drive select lines. Traces DS1, DS2, DS3, and DS4 have been provided to select which drive select line will activate the interface signals for a unique drive. Drive select, when activated to logical zero level, enable the multiplexed I/O lines.

2.2.2 Direction Select (J1 Pin #18)

'Direction select' determines the direction the head-carriage assembly will move when the JU-455-8 is properly selected, and when step pulses with the proper timing are sent to the JU-455-8. If 'direction select' is at logic low, the head-carriage assembly will seek toward the center of the diskette, and away from the center when high.

'Direction select' must be stable at its correct logic state for at least 1 microsecond before each occurrence of the trailing edge of the step pulse, as measured at the drive interface connector, J1.

If the drive is not selected or a write operation is in process, 'direction select' is ignored by the JU-455-8.

2.2.3 Motor On (J1 Pin #16)

The 'motor on' signal causes the JU-455-8 spindle drive motor to turn on. In standard configuration (jumper MS open), this input signal line when true (logic low), will activate the motor if + 5V DC and + 12V DC are applied to the drive, whether or not the drive is selected. A minimum delay of 500 milliseconds must be allowed by the host system after activating this line before attempting to read or write, to allow the diskette to attain proper speed.

It is recommended that the spindle drive motor should be turned off when the drive has not been selected for 10 revolutions or more. This will extend motor and diskette life and decrease power consumption. Host system workload must be analyzed to determine optimum delay between reselection of the drive and turning off the spindle drive motor.

2.2.4 Step (Pin #20)

When the JU-455-8 is properly selected and the trailing edge (a low-to-high transition) of the 'step' signal occurs, the head-carriage assembly will move one track in the direction selected by 'direction select' J1 pin 18.

'Step' and its timing are generated by the host system controller.

First the drive should be selected, then 'direction select' should be set to its correct logic level, then 'step' should be set to a logic low level. A minimum of 1 microsecond later 'step' may make its low-to-high transition (trailing edge of 'step') to initiate head-carriage movement. The minimum allowable time between trailing edges of 'step' is 4 milliseconds. The minimum allowable pulse width for 'step' is 1 microsecond.

Any change in 'direction select' must be made at least 1 microsecond before the trailing edge of 'step', and 'direction select' logic level must be maintained 1 microsecond after the trailing edge of 'step'.

If the JU-455-8 is not properly selected or a write operation is in process, the 'step' pulses from the host system will be ignored.

If 'direction select' is a logic low level and the drive is at the inside track (track 39), and a 'step' pulse is issued by the host system, the head-carriage assembly will attempt to move until stopped by the mechanical safety stop installed on the JU-455-8.

But driving the head-carriage assembly of the JU-455-8 into the safety stops is not recommended. The host system controller should know the position of the head-carriage assembly at all times by reading the sector or track ID address field. In the event that the controller should lose track of the head-carriage assembly's location, it is recommended that 'direction select' be set to a logic high level and several 'step' pulses be issued, at a time, checking after the proper delay each time for the 'track 00' signal to return to a true state (logic low). The head-carriage assembly of the JU-455-8 is automatically positioned to the track zero, after DC powering on.

2.2.5 Write Data (J1 Pin #22)

This interface line provides the data to be written on the diskette in the appropriate sector. Each transition from a high logic level to a low logic level on this line causes write current to be reversed through the head. This line is enabled by 'write gate' being activate. 'write data' must be inactive during a read operation. And if the drive is not properly selected, a write protected diskette is installed, a seek operation is not complete or the drive has no diskette installed, the write data will be ignored.

2.2.6 Write Gate (J1 Pin #24)

The active state (logic low) of this line enables 'write data' to be written on the diskette. The inactive state (logic high) enables the read data logic and seek operation completed.

2.2.7 Side Select (J1 Pin#32)

'Side select' determines which side of a double-sided diskette is to be written on or read from. A logic low (true or logic zero) selects the side 1 head ; a logic high (false or one) selects the side 0 head.

When switching from one side to another, 100 microseconds delay is required before read or write operation can be initiated, and 1100 microsecond delay is required after write operation is complete.

2.2.8 In Use (J1 Pin #4)

Using appropriate jumper options, this line can light the in use LED. See DA/UA jumper option section.

2.2.9 (J1 Pin #2) - Not Used. Reserved for optional use.

2.3 OUTPUT LINES

The JU-455-8 drive has five active signal lines as output. Each output line is driven by a 7438 or equivalent open collector output gate. Individual signal line characteristics are described below:

2.3.1 Index (J1 Pin #8)

'Index' signal is generated once each revolution of the diskette and indicates the physical beginning of a track. When the 'index' signal is true, the signal is a logic low level. When using the 'index' signal, look for a leading edge rather than a level for determining. This interface line is active low when a drive is selected without the diskette. The 'index' signal pulse width is 1.0 to 10.0 milliseconds.

2.3.2 Track 00 (J1 Pin #26)

An active low on this signal line indicates that the read/write head is positioned at track zero (the outermost track). When the read/write head is not at track zero, this line is inactive. When the read/write head is at track zero and additional step out pulse is issued to the drive, microprocessor logic will keep the read/write head positioned at track zero.

2.3.3 Write Protect (J1 Pin #28)

An active low level on this signal line indicates that a write protected diskette has been installed. The drive will inhibit writing when a write protected diskette has been installed, and will notify the host system.

2.3.4 Read Data (J1 Pin #30)

This interface line provides the raw data as detected by the drive electronics. This includes the data and the clock pulse together. Each flux reversal that is sensed on the diskette produces a transition to active low level.

2.3.5 Ready (J1 Pin #34)

This interface line is active low when a diskette is properly inserted and the drive motor is up to speed (about 600 milliseconds after activating the 'motor on'), and informs the controller that the drive is active.

2.4 POWER INTERFACE

The JU-455-8 requires only DC power for operation. DC power to the drive is provided via P2/J2. The two DC voltages, their specifications, and their P2/J2 pin designation is outlined in Table 2-1. The specifications outlined on current requirements are for one drive. The multiple drive systems, the current requirements are a multiple of the maximum current times the number of drives in the system. In addition, Figure 2-3 illustrates the DC power profile.

2.5 FRAME GROUND

Frame ground for the JU-455-8 is provided by a push-on tab terminal, mounted on the rear of the drive directly. See Figure 7-1

When the host systems input power is AC, the JU-455-8 drive frame must be grounded to the third wire safety ground. If the host system is DC powered, the frame ground may be tied to the DC power ground.

2.6 SYSTEM POWER AND GROUND DISTRIBUTION

To provide optimum performance and noise immunity, extreme care must be used to provide low noise grounds. Independent frame ground wires should run from each JU-455-8 drive and other system components to a single point system frame ground.

The 5 volt and 12 volt return lines should be connected together at the host system, but these DC power supply return lines should be isolated from the system frame (AC) ground. These return lines are isolated from frame ground on the JU-455-8 PCB by a 0.01 uF capacitor and 100 kΩ resistor in parallel. The network is provided to suppress differential noise between the DC and AC grounds while providing a DC connection.

Grounding for the TTL signal lines between the JU-455-8 PCB logic ground and host system (controller) PCB logic ground should be provided by the 17 signal ground pins of the J1 connector. All odd pins, 1 through 33, should be connected to the controller signal ground plane.

TABLE 2-1 DC POWER REQUIREMENTS

P2/J2 PIN	DC VOLTAGE	TOLERANCE	CURRENT at OPERATING	CURRENT at STANDBY	MAX RIPPLE
1	+ 12V	$\pm 10\%$ ($\pm 1.2V$)	0.17A TYP 0.55A MAX 0.9A PEAK	0.01A TYP 0.02A MAX	100 mV p-p
2	+ 12V Return	**			
3	+ 5V Return	**			
4	+ 5V	$\pm 5\%$ ($\pm 0.25V$)	0.37A TYP 0.47A MAX	0.27A TYP 0.33A MAX	50 mV P-P

** + 12V and + 5V Ground Returns are tied together at drive PCB.

MODE	MOTOR-ON	DRIVE SEL.	SIDE 1 SEL.	WRITE GATE
STANDBY	H	H	H	H
MOTORON	L	H	H	H
READ	L	L	H or L	H
WRITE	L	L	H or L	L
SEEK	L	L	—	H

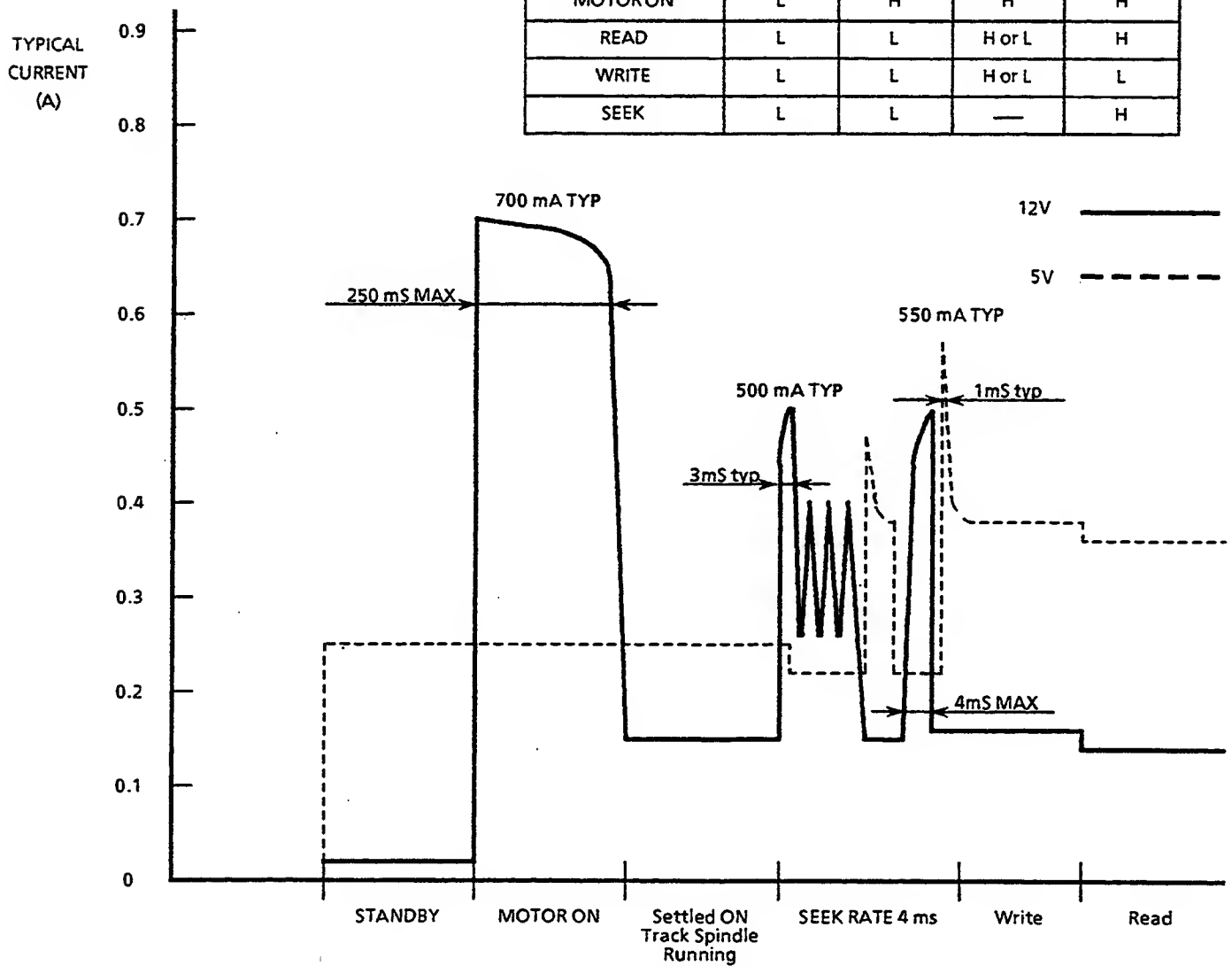


FIGURE 2-3 DC POWER PROFILE

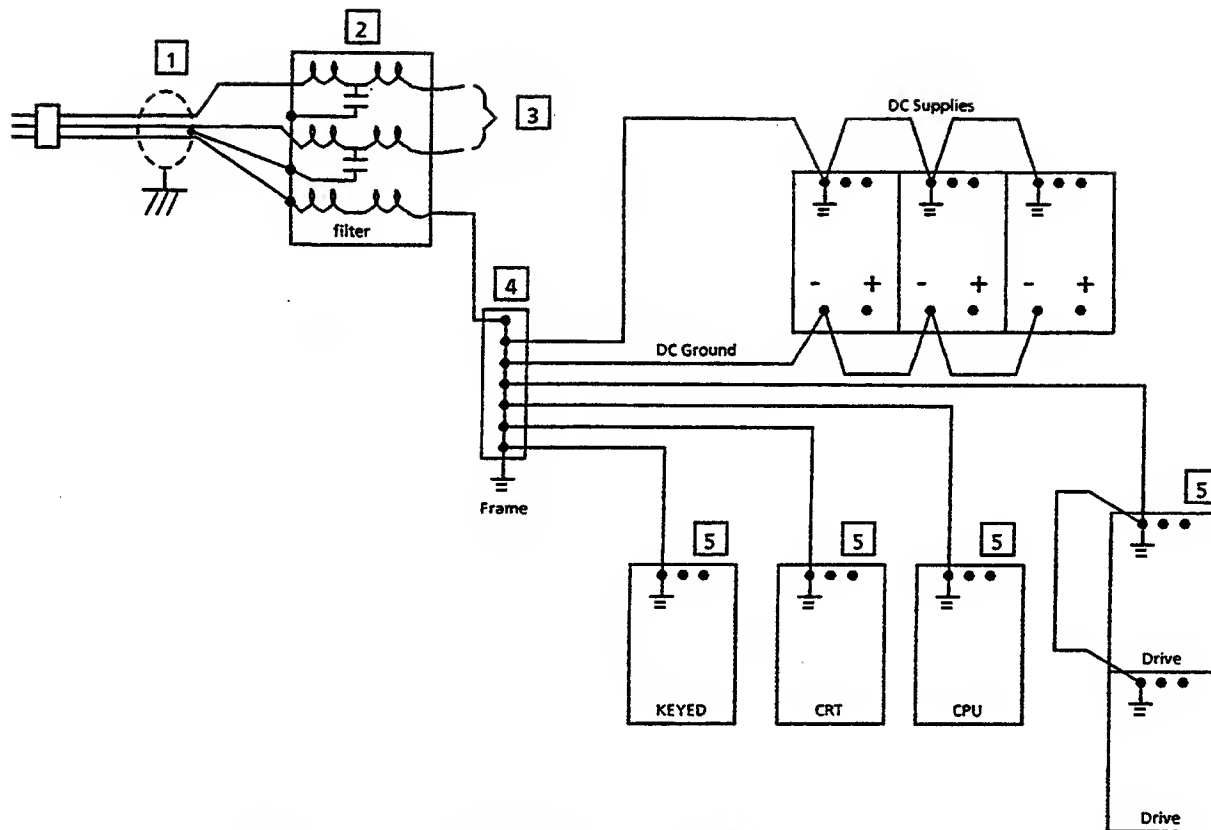


FIGURE 2-4 RECOMMENDED POWER AND GROUND DISTRIBUTION

NOTE:

1. Shield power cable- Should be only one and tied to ground at filter end only.
2. Line filter Isolated from frame with system ground filtered.
3. AC distribution- Twisted pair cable including ground wire (as shown in 3 places) . Wire size large enough to maintain less than 25 mV/ft drop.
4. AC ground TB- Only one connection to frame for all DC grounds and one AC ground.
5. DC distribution- Separate twisted pair cable from each device to the DC supplies (as shown in four places). Wire size large enough to maintain less than 10 mV/ft drop.

2.7 FUNCTIONAL OPERATIONS

2.7.1 Power Sequencing

Applying dc power to the drive can be done in any sequence. However, during power up, the WRITE GATE line must be held inactive or at a high level. This will prevent possible "glitching" of the media. After application of dc power, a 500 milliseconds delay should be introduced before any operation is performed.

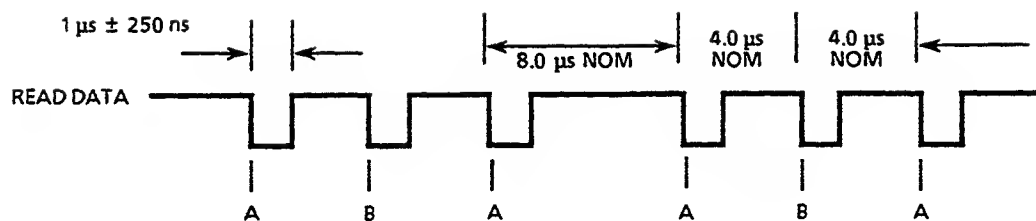
After powering on, initial position of the read/write head is at track 0. Because of it, a recalibrate operation should not be required.

2.7.2 Read Operation

Reading data from the drive is accomplished by:

- a. Activating the DRIVE SELECT line.
- b. Selecting the head.
- c. WRITE GATE being inactive.

The timing requirements for the read operation is shown in Figure 2-5.



A = LEADING EDGE OF BIT MAY BE ± 800 ns FROM ITS NOMINAL POSITION.
 B = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.

FIGURE 2 - 5 READ DATA TIMING (FM ENCODING)

2.7.3 Write Operation

Writing data to the drive is accomplished by:

- Activating the DRIVE SELECT line.
- Selecting the head.
- Activating the WRITE GATE line.
- Pulsing the WRITE DATA line with the data to be written.

The timing specifications for the write data pulse are shown in Figure 2-6. Write data encoding can be FM or MFM.

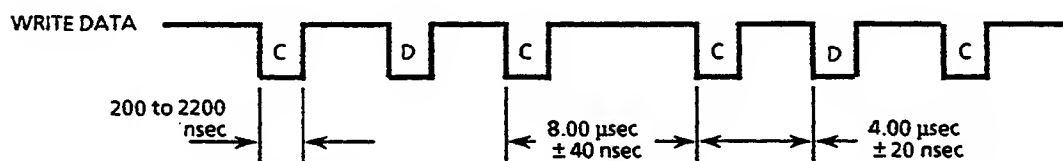


FIGURE 2 - 6 WRITE DATA TIMING (FM ENCODING)

SECTION III ERROR RECOVERY

3.1 WRITE ERROR

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation (commonly called a "write check"). To correct the error, another write and write check operation must be done. If the write operation is not successful after ten attempts have been made, a read operation should be attempted on another track. This is done to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

3.2 READ ERROR

Most errors that occur will be "soft" errors. Soft errors are usually caused by the following:

- a. Airborne contaminants passing between the read/write head and the disk. The contaminants will generally be removed by the cartridge self-cleaning wiper.
- b. Random electrical noise which usually lasts for a few microseconds.
- c. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedure is recommended to recover from errors:

- a. Reread the track ten times or until such time as the data is recovered.
- b. If data is not recovered after using step "a." access the head to the adjacent track in the same direction it was moved previously. Return to the desired track.
- c. Repeat step "a."
- d. If data is not recovered, the error is not recoverable.

3.3 SEEK ERROR

Seek errors are detected by reading the ID field after the seek is completed. The ID field contains the track address. If a seek error is detected, the host system should issue a recalibrate operation (step out until the TRACK 00 line goes active) and seek back to the original track.

SECTION IV CUSTOMER INSTALLABLE OPTIONS

4.1 PLUG / WIRE OPTIONS

The JU-455-8 can be modified by the user to suit individual needs. These modifications can be implemented by adding, changing, or deleting connections. These changes can be accomplished by the use of a plug jumper (See Table 4-1) or by a wire jumper (See Table 4-2). Figure 4-1 shows plug jumper and wire jumper location.

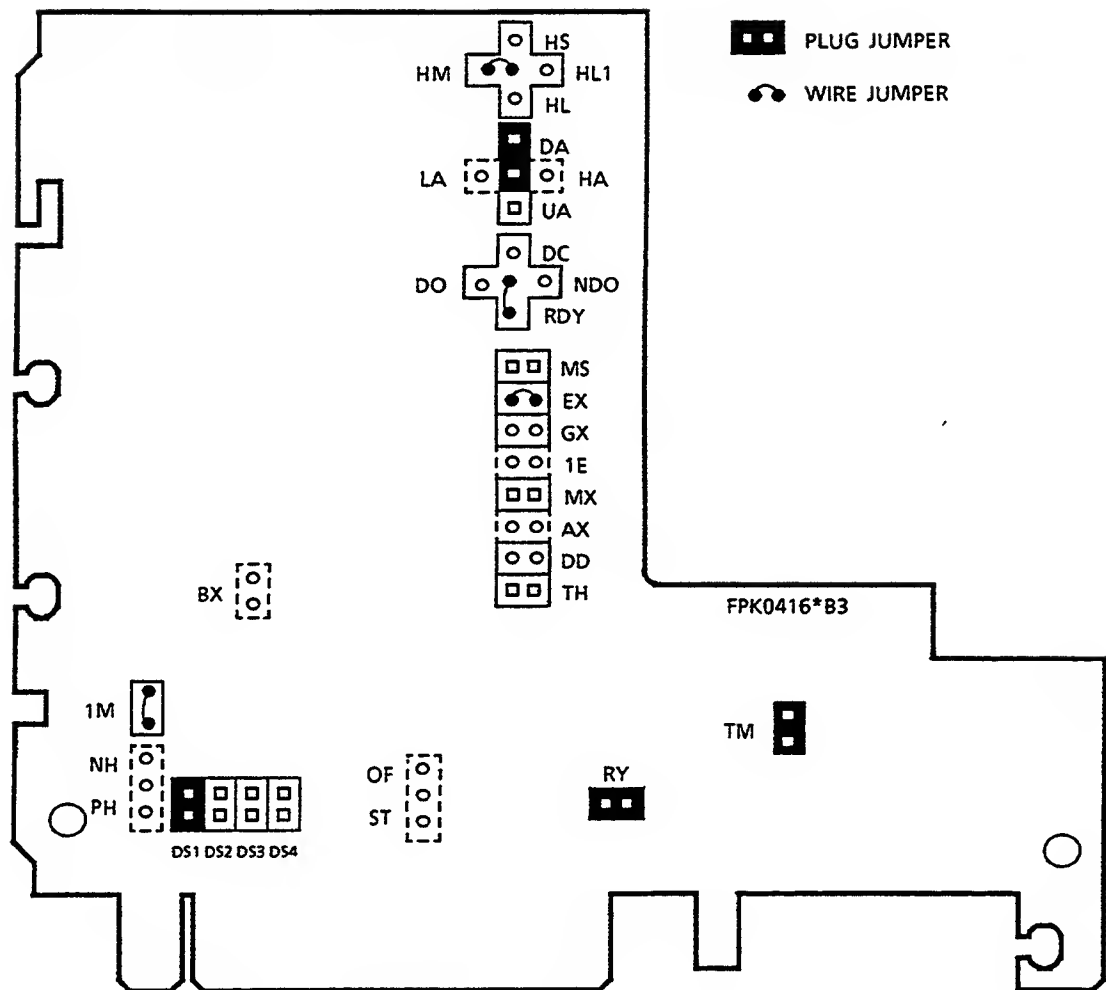
Option plug jumper : 2 mm pitch, Iriso Part Number IMSA 9215 H - T

Table 4 - 1 Plug Jumper Option

Plug Jumper	Description	Shipped form Factory (JU - 455 - 8)	
		Open	Short
DS1	Drive Select 1		○
DS2, 3, 4	Drive Select 2, 3, 4	○	
MX	Constant Drive Select Use in a single drive system (only)	○	
MS	Enables Drive Motor with Drive Select (MS short) / with Motor On (MS open)	○	
RY	Ready Signal (J1 #34)		○
UA	In Use LED lights with In Use	○	
DA	In Use LED lights with Drive Select		○
TM	Terminal Resistor		○

Table 4 - 2 Wire Jumper Option

Wire Jumper	Description	Shipped form Factory (JU - 455 - 8)	
		Open	Short
RDY	Enable True Ready		○
1M	Signal Mode		○
EX	Disenable True Ready (Index)		○



NOTE : PH, NH, 1M, ST, OF, BX, 1E, AX, HM, RDY, EX, GX, DD, TH FACTORY USE ONLY

FIGURE 4-1 PLUG JUMPER & WIRE JUMPER LOCATIONS

4.2 JUMPER OPTIONS (at PCB-NO FPK 0416★B3)

4.2.1 DA/UA JUMPER (See Figure 4-4)

DA	UA	IN USE LED
OPEN	CLOSED	In use LED is a direct function of "IN USE" line only of J1 I/O.
CLOSED	OPEN	In use LED is a direct function of "DRIVE SELECT" line only of I/O.

Note : DA/UA : Plug jumper option.

4.2.2 MS JUMPER (See Figure 4-3)

MS	SPINDLE MOTER
OPEN	Spindle motor is a function of "MOTOR ON" line of J1 I/O. Motor is turned on when there is a logical "Low" on "MOTOR ON" signal.
CLOSED	Spindle motor is not a function of "MOTOR ON" line, instead the motor is turned on when the drive is selected.

Note : MS : Plug jumper option.

4.2.3 MX JUMPER (See Figure 4-3)

MX	DRIVE SELECTION
OPEN	Drive is selected when "DRIVE SELECT" line of J1 I/O. interface is low.
CLOSED	Drive is always selected irrespective of any logic level on "DRIVE SELECT" line of J1 I/O. interface.

Note : MX : Plug jumper option.

4.2.4 HS / HL JUMPER (See Figure 4-6) ※※※ OPTION ※※※

HS	HL	HEAD LOAD
CLOSED	OPEN	Head load is a direct function of "DRIVE SELECT" line only of I/O.
OPEN	CLOSED	Head load is a direct function of "IN USE" & "DRIVE SELECT" line of I/O.

Note : HS / HL : Wire jumper option.

4.2.5 GX JUMPER (See Figure 4-3) ※※※ OPTION ※※※

GX	READ DATA (PIN #30 of I/O INTERFACE)
CLOSED	Read Data is masked when the diskette doesn't attain proper speed, or seek operation.
OPEN	Read Data isn't masked,

Note : GX Wire jumper option.

4.2.6 EX JUMPER (See Figure 4-3) ※※※ OPTION ※※※

EX	INDEX (PIN #8 of J1 I/O INTERFACE)
CLOSED	'INDEX' is generated once each revolution of the diskette, when 'DRIVE SELECT' line of J1 I/O interface is low.
OPEN	'INDEX' is generated once each revolution of the diskette, only after read/write head has 'settled' on a track. This mode is usable in seeking process to tell the host system (via latent index) that the drive is 'internally' not ready yet for the host system to perform any read or write operation on it.

Note : EX Wire jumper option.

4.2.7 RY JUMPER (See Figure 4-5)

RY	READY
CLOSED	Connect the READY signal to Pin #34 of J1.
OPEN	Special applications - IBM PC/XT,PC/AT*

* IBM is the registered trademark of International Business Machines : IBM Corp.

Note : RY : plug jumper option.

4.2.8 READY (See Figure 4-5)

Closed RDY, RY

Ready PIN #34 is active LOW when a diskette is properly inserted, the drive motor is up to speed and more than two INDEX pulses are detected.

Note: RDY : wire jumper option.

4.2.9 DISK CHANGE *** OPTION *** (See Figure 4-6)

Closed DC, RY

Disk change PIN #34 is latched LOW by "DRIVE SELECT" during power up or when the door is open.

To unlatch the logic level, the drive should step a track while it selected, powered up and door closed.

Note: DC : wire jumper option.

4.2.10 DOOR OPEN *** OPTION *** (See Figure 4-6)

Closed DO, RY

Disk change PIN #34 is direct function of door open status.

It is active Low when the door is open; otherwise it remains High.

Note : DO : wire jumper option.

4.2.11 DOOR CLOSED *** OPTION *** (See Figure 4-6)

Closed NDO, RY

Disk change PIN #34 is direct function of door open status.

It is active High when the door is open; otherwise it remains Low.

Note : NDO : wire jumper option.

*** OPTION ***

There is need to the Door SW mechanism.

4.2.12 TH JUMPER (See Figure 4-3)

TH	PIN #34 of I/O INTERFACE
CLOSED	PIN #34 is not gated by DRIVE SELECT signal.
OPEN	PIN #34 is gated by DRIVE SELECT signal.

Note : TH : plug jumper option.

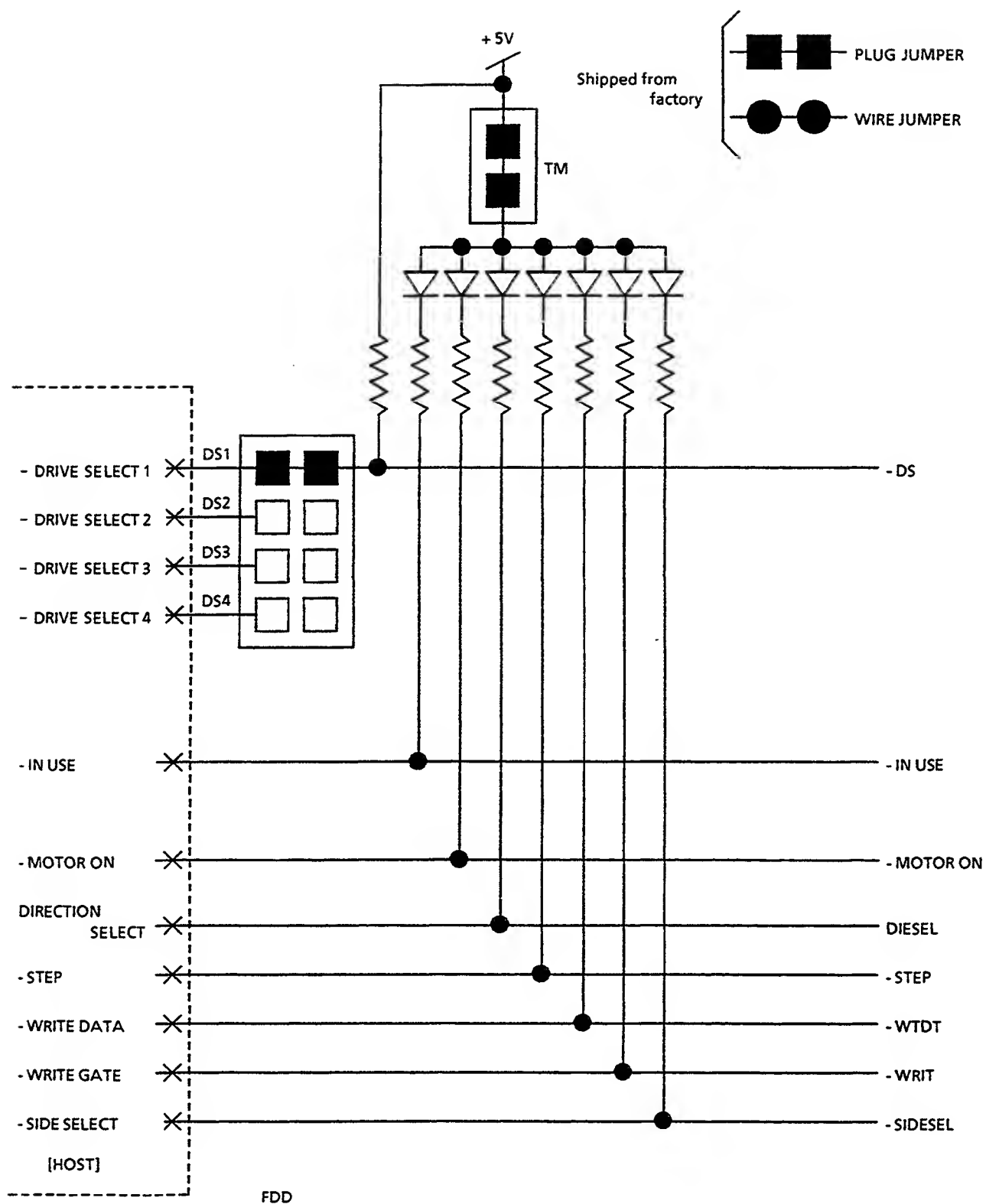


FIGURE 4-2 JUMPER CONFIGURATION FOR DRIVE SELECT, & TERMINATION

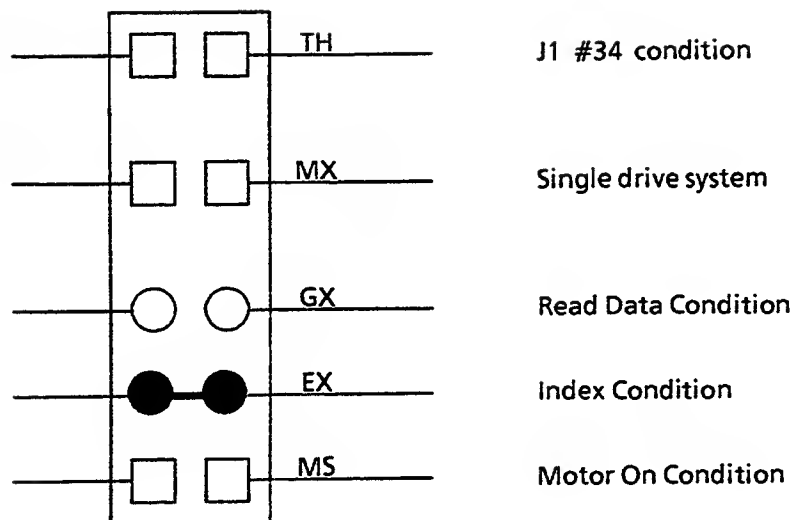


FIGURE 4 - 3 JUMPER CONFIGURATION FOR TH, MX, GX, EX, MS

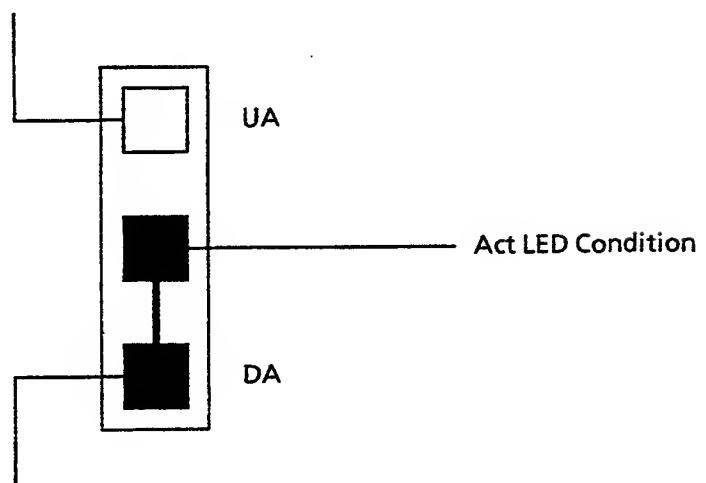


FIGURE 4 - 4 JUMPER CONFIGURATION FOR ACT. LED CONTROL

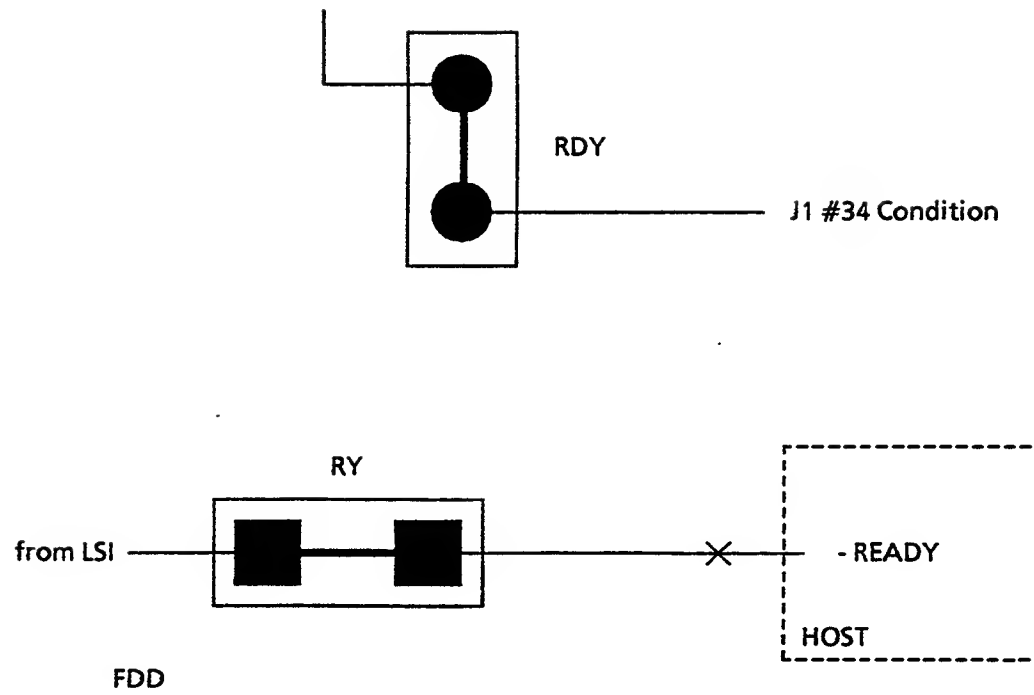
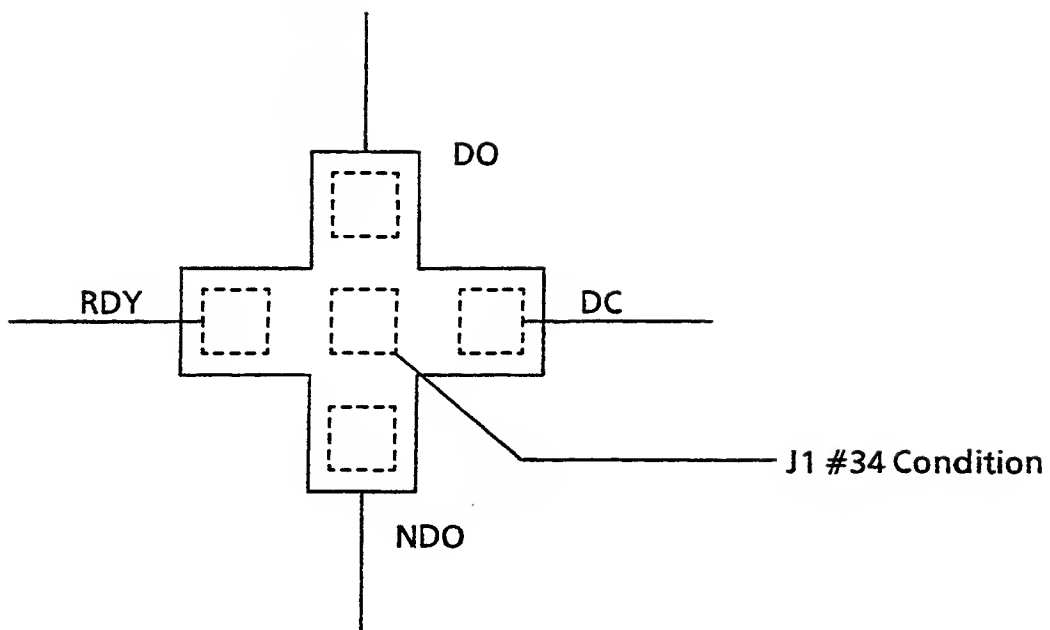


FIGURE 4-5 JUMPER CONFIGURATION FOR READY

*** OPTION ***

(1) J1 #34 CONDITION



(2) HEAD LOAD

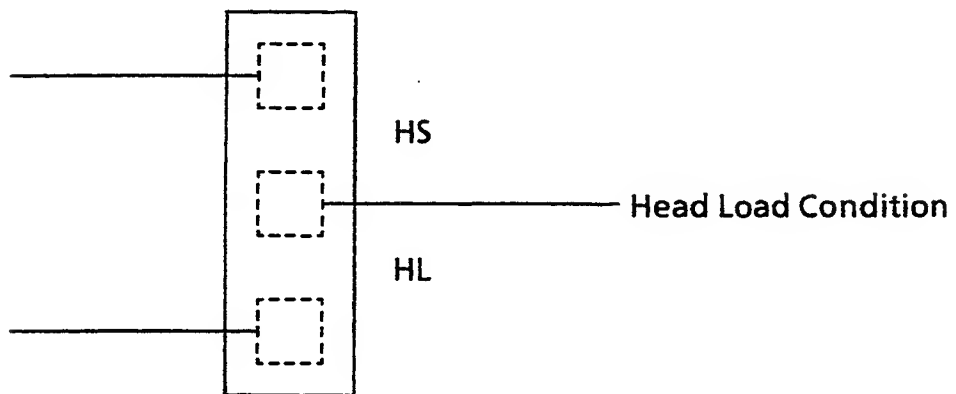


FIGURE 4-6 OPTION JUMPER CONFIGURATION

SECTION V

OPERATION PROCEDURES AND PRECAUTIONS

5.1 POWER ON PROCEDURE

The DC power supply can be turned on in any order. The write gate signal should be held at high level, however, so that the power on action does not cause illegal writing. An interval of 500 milliseconds is necessary between power-on time and operation start time. During power on, in order to reset the circuits of drive (Power on Reset), the rise-up-time of DC power is required at least 100 microseconds without the bouncing. After powering on, initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, JU-455-8 is provided a Step Out operation that the read/write heads move until the 'track 00' signal becomes active low (Recalibrate operation). Because of this, a recalibrate operation should not be required.

5.2 DRIVE SELECTION

The drive is selected when the drive select signal goes to low level.

5.3 DRIVE MOTOR TURN-ON

Throughout data reading and writing, the drive motor must rotate at a constant speed. The drive motor is activated when the motor on signal is set at low level, and requires 500 millisecond to reach constant speed. When the motor on signal changes to high level, the drive motor stops in about 4 seconds. When the write protect detector detects a change point due to insertion or removal of the diskette, the drive motor rotates for 10 seconds.

5.4 PRECAUTIONS

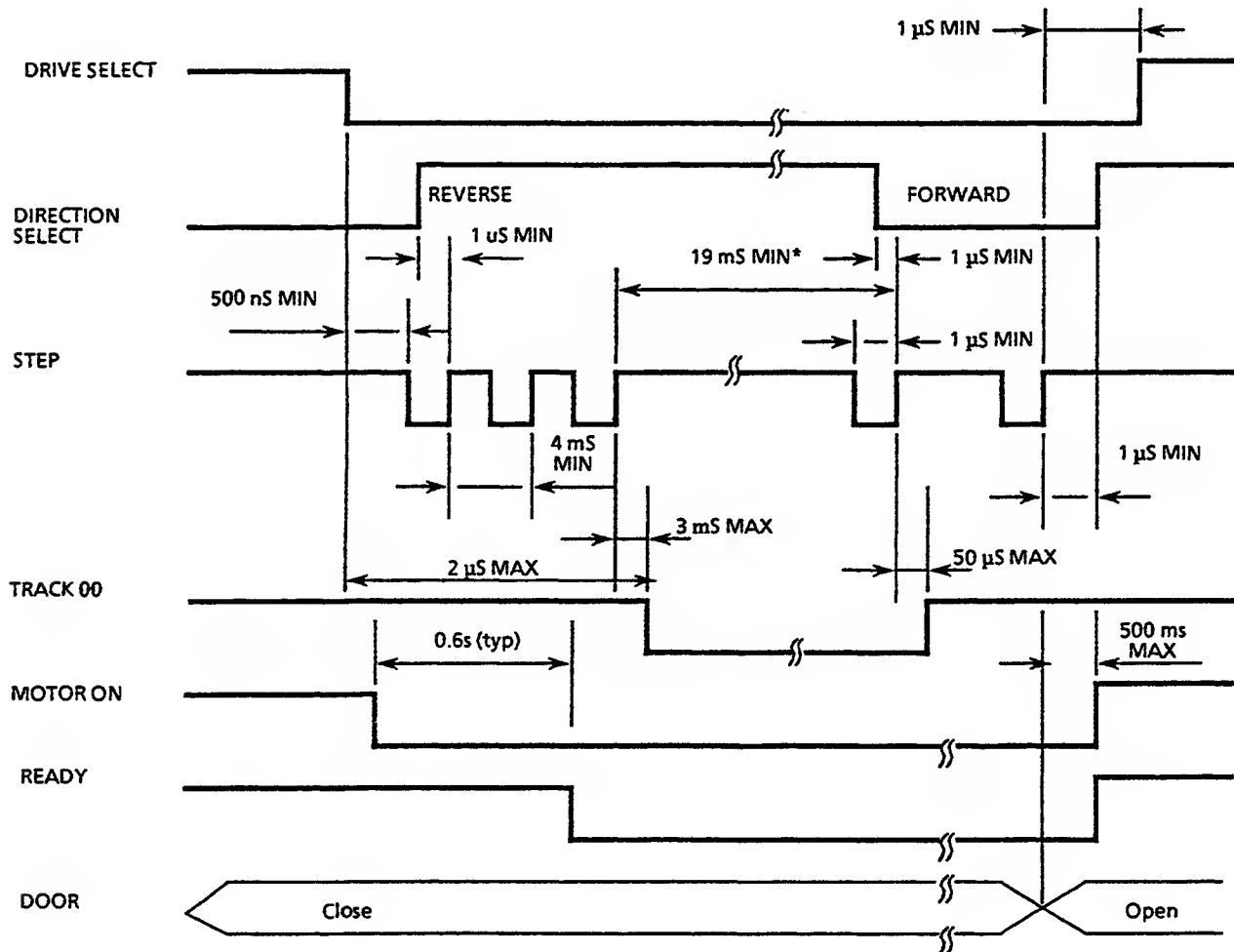
- 1) Upon installation, pay close attention to reducing the ambient electrical noise, such as the noise from the switching power supply or CRT.
- 2) JU-455-8 automatically rotates the spindle motor for about 10 seconds, when a diskette is inserted, for better clamping accuracy. This also prevents the diskette from being damaged upon clamping. For full use of this feature, turn power on before inserting a diskette, then clamp the diskette within 10 seconds after insertion.
- 3) When shipping the drive, insert the dummy sheet and turn the handle to clamp in the same manner as a diskette.

SECTION VI TIMING DIAGRAM

The step, read, write and general control timings are given on the following pages.

Note: **MIN** = The minimum amount of time (or longer) the controller must wait for the execution of the next operation.

MAX = The maximum amount of time required by the drive to complete on operation. The maximum amount of time delay allowed by the controller for next operation: i.e. The controller must execute (start to stop) on operation within the maximum limit amount of time.



*NOTE: Turn around time is $19\ \text{ms}$ (MIN) when direction is changed.

FIGURE 6 - 1 STEP TIMING

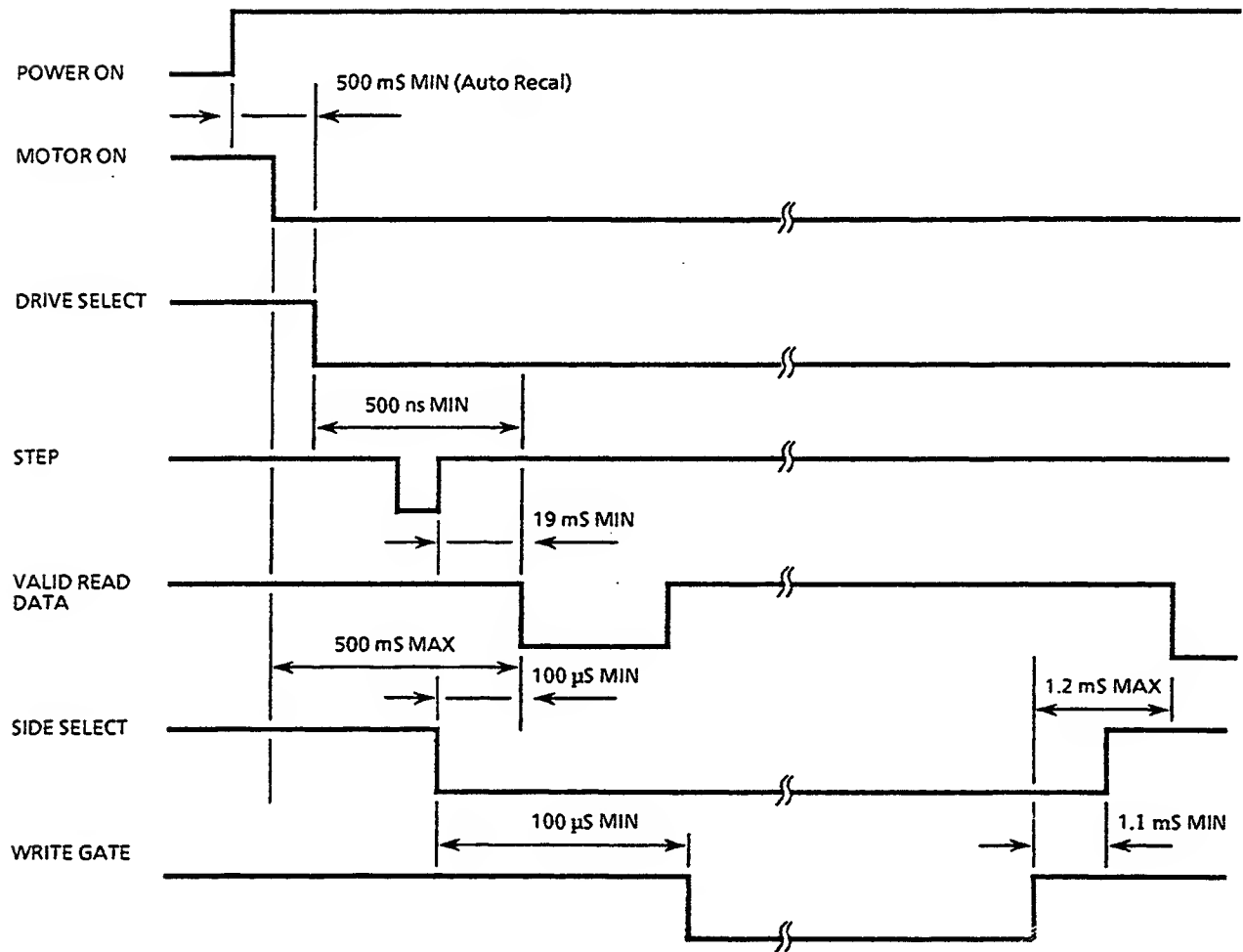


FIGURE 6 - 2 READ INITIATE TIMING

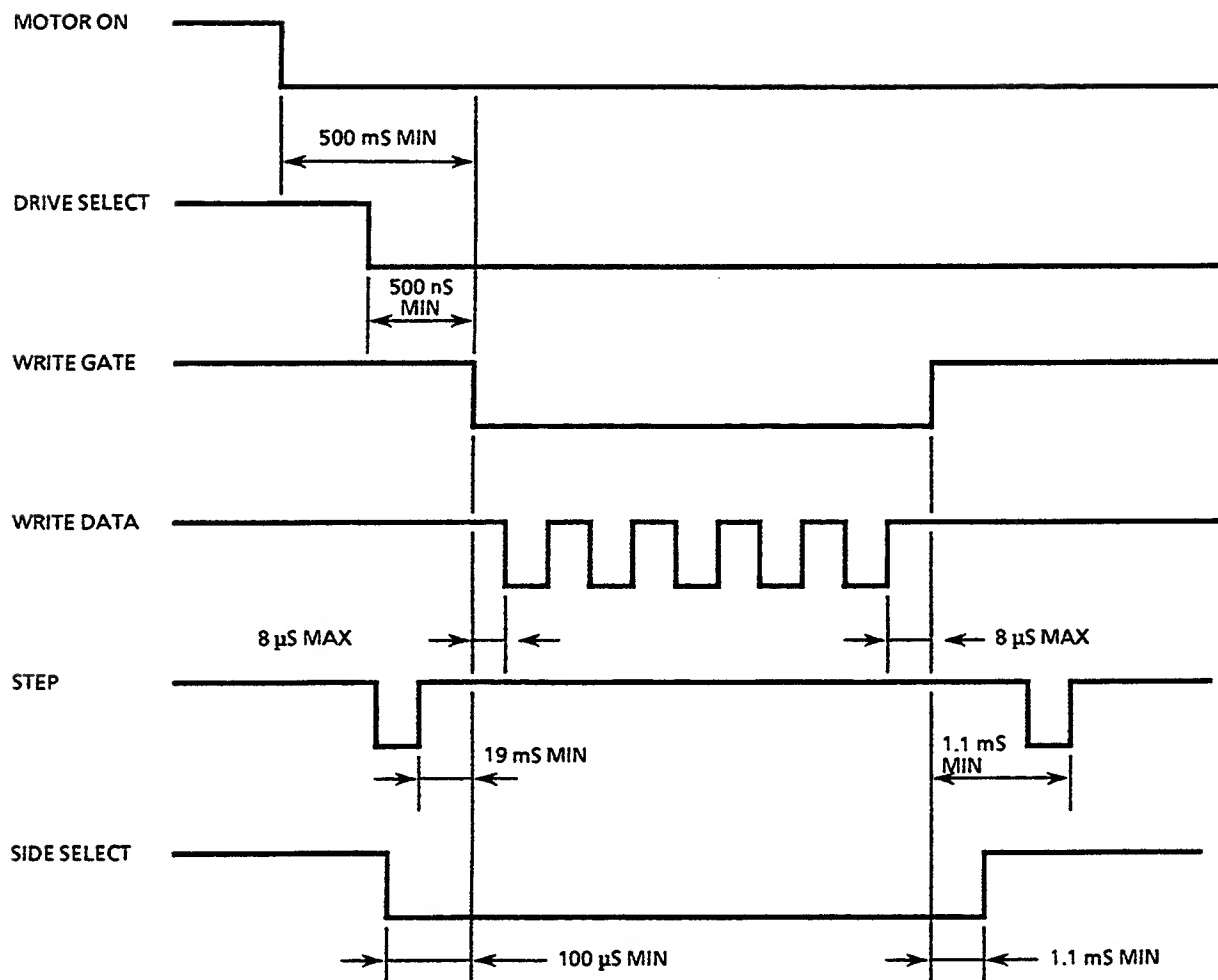


FIGURE 6-3 WRITE INITIATE TIMING

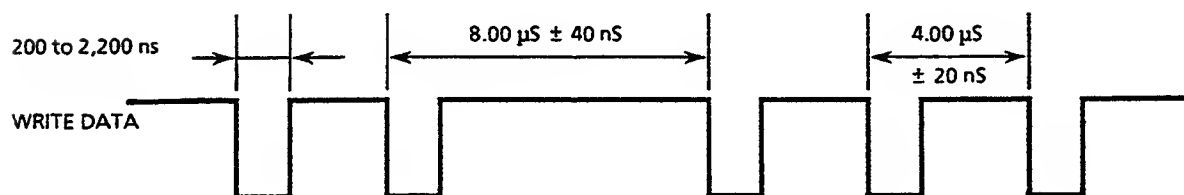
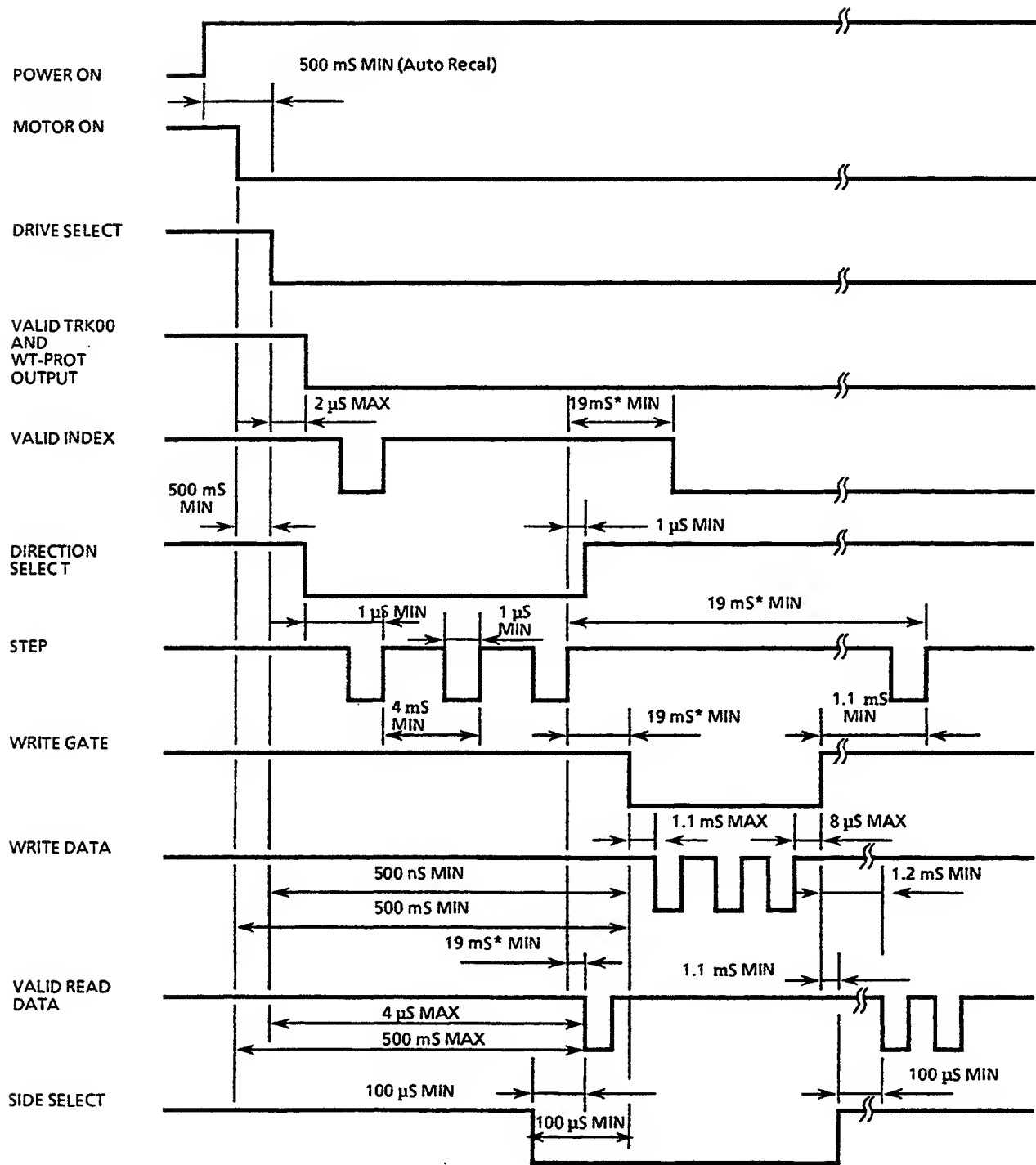


FIGURE 6-4 WRITE DATA TIMING



*Seek settle time is 19 mS MIN.

FIGURE 6-5 GENERAL CONTROL AND DATA TIMING

SECTION VII PHYSICAL SPECIFICATION

The electrical interface between the JU-455-8 and the host system is via three connectors. The first connector, J1, provides all of the TTL level I/O control signals for the host system and the drive. The second connector J2, provides DC. power for the drive from the host system. The third connector, a push on tab terminal, provides a frame ground for the drive. See Figure 7-1 for connector locations.

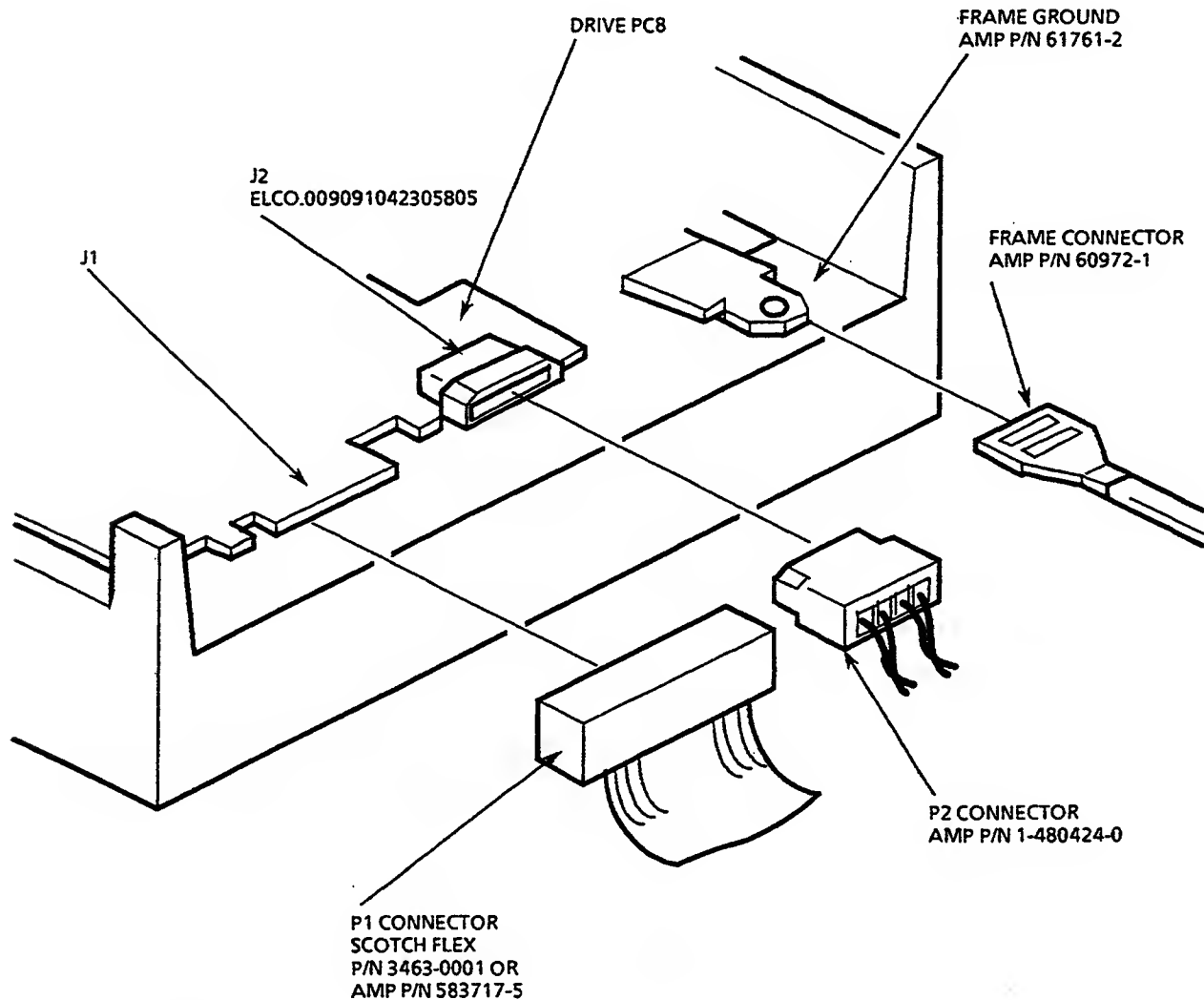


FIGURE 7-1 INTERFACE CONNECTOR LOCATIONS

7.1 J1 CONNECTOR (SIGNAL)

Connection to J1 is through a 34 pin P.C.B. edge connector. The dimensions for this connector are shown below. The pins are numbered 1 through 34 with the even numbered pins containing the control and data signals and the odd pins being ground. A key slot is provided between pins 4 and 6 for optional keying.

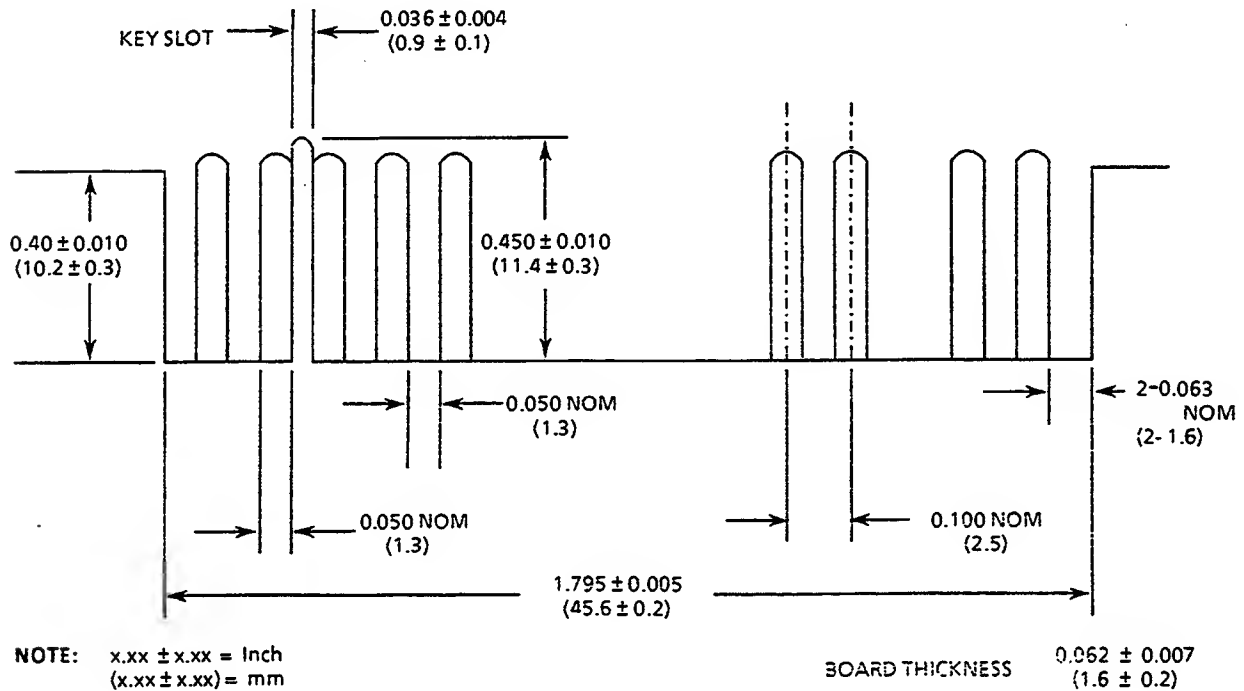


FIGURE 7-2 J1 CONNECTOR DIMENSIONS

7.2 J2 CONNECTOR (POWER)

The D.C. power connector, J2, is located in the rear of the drive. J2 is a four pin ELCO connector 009091042305805. The recommended mating connector is AMP P/N 1-480424-0 or equivalent utilizing AMP pins P/N170121-1 or equivalent.

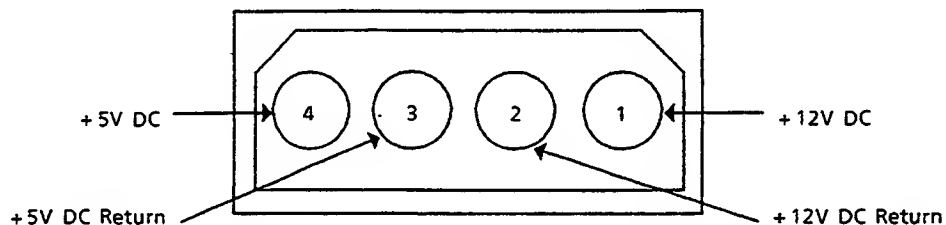


FIGURE 7-3 J2 CONNECTOR PIN ASSIGNMENT

7.3 FRAME GROUNDING

CAUTION

The drive must be frame grounded to the host system to ensure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good AC ground, a wire from the system AC ground must be connected to drive. For this purpose, a faston tab is provided on the drive in the rear. The tab is AMP P/N 61761-2 or equivalent and its mating connector is AMP P/N 60972-1 or equivalent.

7.4 DESCRIPTION OF THE TEST POINTS (TP)

TP 1 & TP 2	:	Differential Analog Read Data Signal
TP 7	:	Index
TP 8	:	Track 00
TP 12	:	Step
TP 6	:	Read Data
TP 5, TP 10	:	Ground

7.5 MOUNTING

The JU-455-8 is capable of being mounted in any of the following positions.

1. Front Loading - mounted vertical with door opening left or right.
- mounted horizontal with PCB up.

CAUTION

Do not mount the JU-455-8 horizontally with the PCB down and Top Loading (mounted upright). Such a configuration could cause damage to the drive.

The mounting hardware for the bottom and side holes is to be #3 metric.

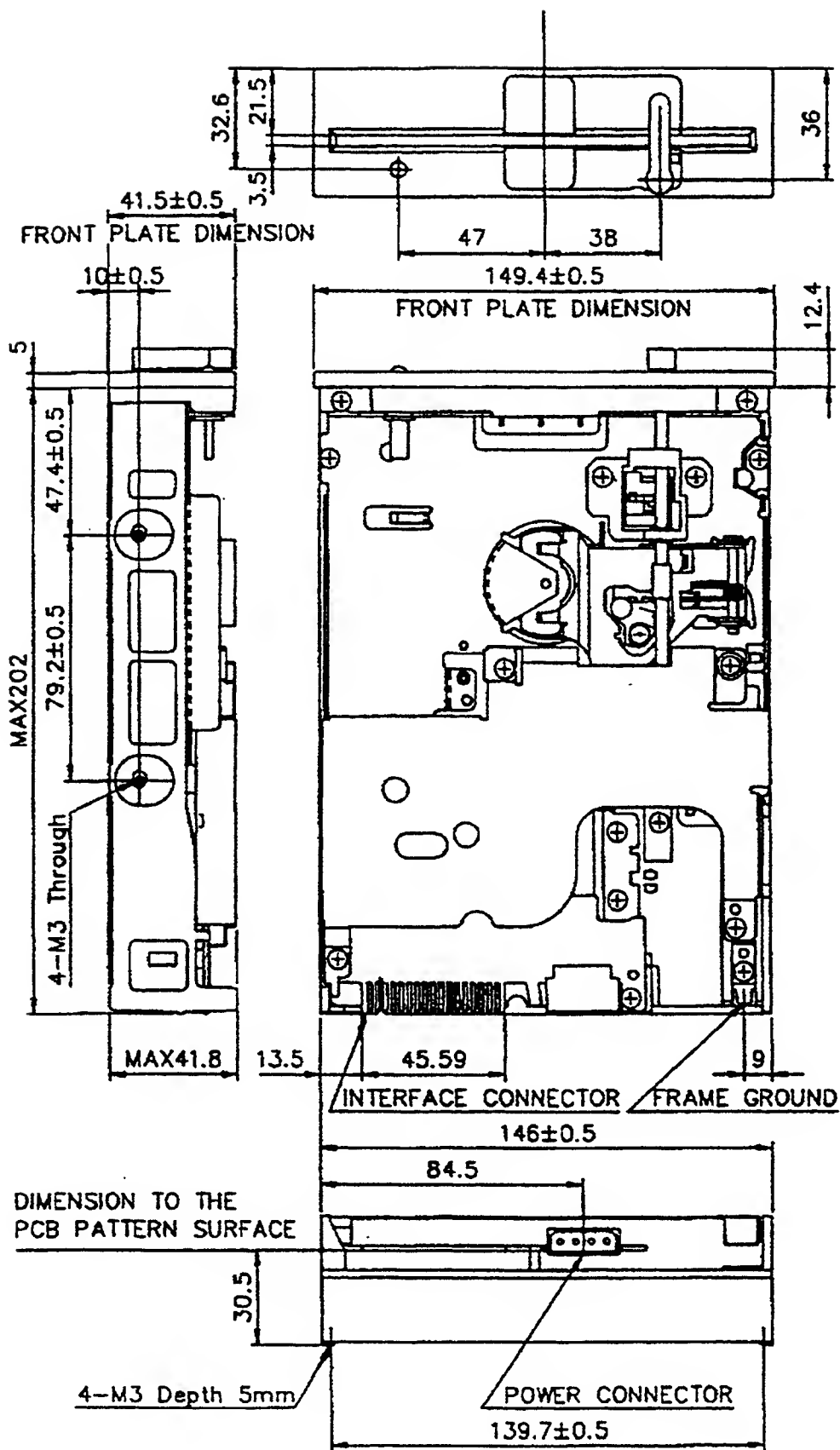


FIGURE 7-4 MECHANICAL DIMENSIONS

Power Supply Computer Products XL200

=====

AS OF 5/20/91

720126-03* REV: C NFS200-7603*, TOP ASSY

MODEL:

ECO NO: 15878

DATE OF LAST ECO: 5/03/91

PART NUMBER	DESCRIPTION	ITM	QTY PER ASSEMBLY	UM	SC	REFERENCE DESIGNATOR	EFF DATE	OBS DATE
100018-150	DIODE, FR,	1	1.000	EA	P1	CR34	12/28/89	99/99/99
100035-200	DIODE, FR,	2	1.000	EA	P1	CR31	12/28/89	99/99/99
120016	XSTR, PNP,	8	1.000	EA	P1	Q14	12/28/89	99/99/99
140003	IC, SHUNT R	18	1.000	EA	P	VR4	12/28/89	6/17/91
210056-687	CAP, ALUM,	23	2.000	EA	P1	C50,C53	6/01/90	99/99/99
220010-104	CAP, MPST,	29	2.000	EA	P1	C51,C54	12/28/89	99/99/99
220011-474	CAP, MPST,	30	1.000	EA	P1	C52	12/28/89	99/99/99
240001-105	CAP CER 1 U	32	1.000	EA	P1	C66	11/29/89	99/99/99
240015-471	CAP, CER DI	33	1.000	EA	P1	C38	12/28/89	99/99/99
300020-223	RES, CF, 1/	41	1.000	EA	P1	R45	12/28/89	99/99/99
300020-471	RES, CF, 1/	43	2.000	EA	P1	R64,R65	12/28/89	99/99/99
300030-1.0	RES/FUSE, C	50	3.000	EA	P	R63,R69,	12/28/89	99/99/99

R5

CONTINUE? *

1 File 2 3Command 4Logging 69 11 5 File 6Terminal7 Help 8 Exit
Transfer Options c Manager AdvLink

=====

AS OF 5/20/91

720126-03* REV: C NFS200-7603*, TOP ASSY

MODEL:

ECO NO: 15878

DATE OF LAST ECO: 5/03/91

PART NUMBER	DESCRIPTION	ITM	QTY PER ASSEMBLY	UM	SC	REFERENCE DESIGNATOR	EFF DATE	OBS DATE
320010-1872	RES, MF, 1/	60	1.000	EA	P1	R67	12/28/89	99/99/99
320010-4871	RES, MF, 1/	62	1.000	EA	P	R68	12/28/89	99/99/99
330010-470	RES, MO, 2W	68	1.000	EA	P	R47	12/28/89	99/99/99
330020-221	RES, MO, 1W	70	1.000	EA	P1	R78	12/28/89	99/99/99
430009-0187	TUBING, SHR	75	.050	FT	F	.6" ON R78	11/29/89	99/99/99
500407-01	CHASSIS, L-	80	1.000	EA	P		12/28/89	99/99/99
530003-163	LABEL, SFTY	85	.000	EA	X	HK USE	12/28/89	99/99/99
						ONLY		
530004-163	LABEL, SFTY	86	1.000	EA	X	SIDE OF L2	11/29/89	99/99/99
560005-170	HEATSINK, P	90	1.000	EA	X	CR31	12/28/89	99/99/99
560007-110	HEATSINK, P	91	1.000	EA	X	Q14	12/28/89	99/99/99
600004-0250	SCREW, PH P	95	2.000	EA	P	Q14,CR31	12/28/89	99/99/99
600059	NUT, HEX, K	96	2.000	EA	P	Q14,CR31	12/28/89	99/99/99

CONTINUE? *

1 File 2 3Command 4Logging 94 11 5 File 6Terminal7 Help 8 Exit
Transfer Options c Manager AdvLink

AS OF 5/20/91
 720126-03* REV: C NFS200-7603*, TOP ASSY
 MODEL:
 ECO NO: 15878
 DATE OF LAST ECO: 5/03/91

PART NUMBER	DESCRIPTION	ITM	QTY PER		REFERENCE		EFF DATE	OBS DATE
			ASSEMBLY	UM SC	DESIGNATOR			
640019	THERMAL COM	100	.001	GA F	Q14,CR31		11/29/89	99/99/99
790126-01	ASSY, SUB N	105	1.000	EA X			11/29/89	99/99/99
800131	INDUCTOR, .	110	1.000	EA P	L13		12/28/89	99/99/99
800235	CHOKE, COUP	111	1.000	EA P	L14		12/28/89	99/99/99
800263	TRANSFORMER	112	1.000	EA M	T1		12/28/89	99/99/99
800244	INDUCTOR, -	113	1.000	EA M	L11		12/28/89	99/99/99
840021	TAPE, 2 SID	116	.001	RL F	L11,L13, L14		11/29/89	99/99/99
970416	PINOUT/OUTL	120	.000	EA F	SHIP WITH SUPPLY		12/28/89	99/99/99
970418	GERMAN INST	121	.000	EA F	SHIP WITH SUPPLY		12/28/89	99/99/99
620036	FOOT, TAPER	122	1.000	EA P	UNDER L2		4/29/91	99/99/99

ASSEMBLY: PART NUMBER?

*
 1 File 2 3Command 4Logging 120 23 5 File 6Terminal7 Help 8 Exit
 Transfer Options c Manager AdvLink

REV.	ECO.	DESCRIPTION	DATE	ASPO.
REV. 1	1	1/1/78		
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REV. 7	7	1/1/78		
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REV. 9	9	1/1/78		
REV. 10	10	1/1/78		
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REV. 24	24	1/1/78		
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REV. 99	99	1/1/78		
REV. 100	100	1/1/78		

COMPONENT VALUE CHART

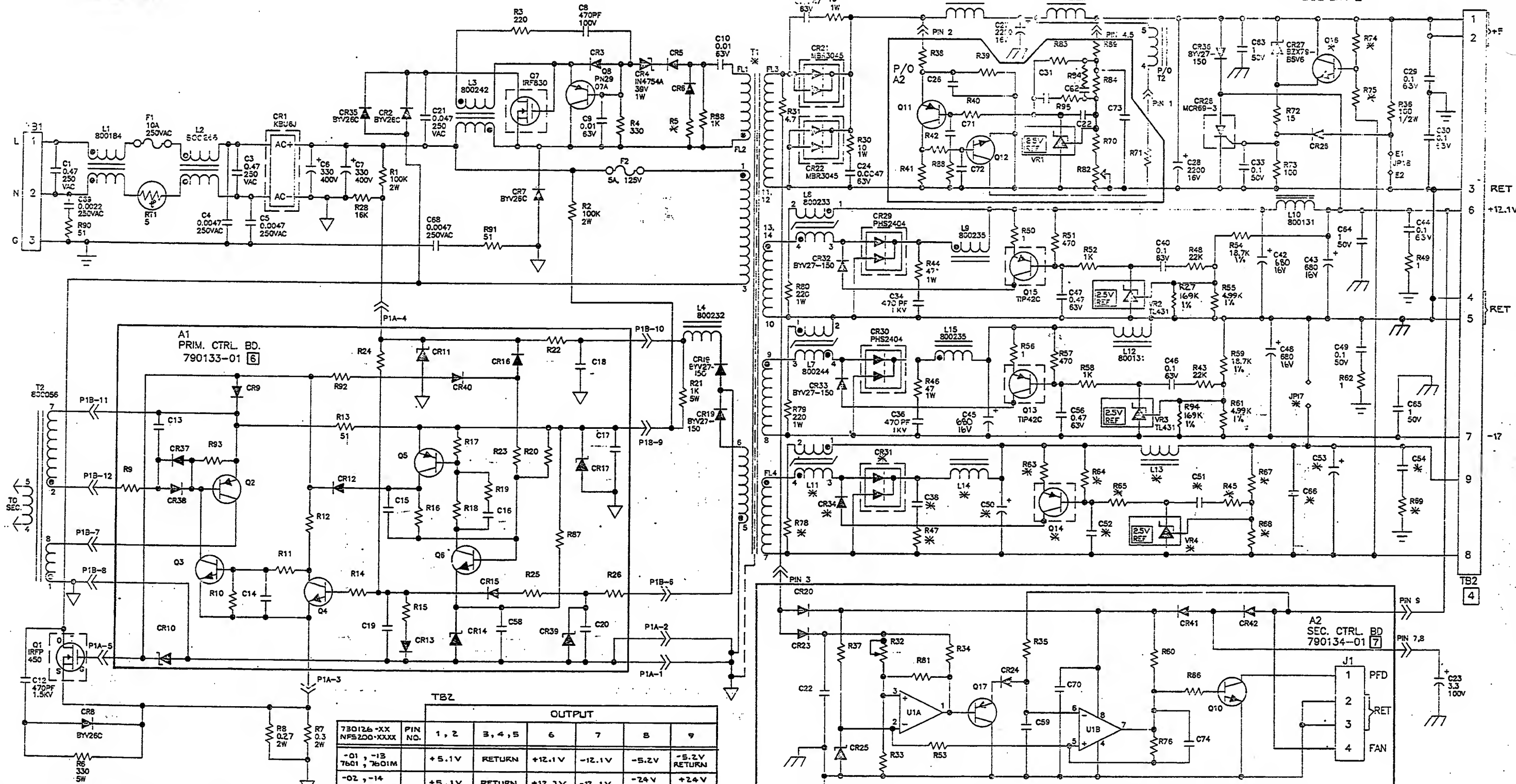
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730126-01/-13 NFS200-7601/-7601M	100035-200 16A, 200V	BYV27-150	TIP42C	2N3904	TL431.5	2200PF, 100V	1800, 10V	0.1, 63V	0.47, 63V	1800, 10V	0.1, 63V	1.0, 50V	1.0	22K	47 1/2W	1.0	470	470	5.23K, 1%	4.87K, 1%	1.0	1K	820	220, 1W	JUMPER	800244	800131	800235	800236
730126-02/-14 NFS200-7602/-7602M	100072-400 8A, 400V	BYV26C	MJE5731A	—	TL431.5	470PF, 1KV	680, 35V	0.1, 63V	0.47, 63V	680, 35V	0.1, 63V	1.0, 50V	4.7	33K	47 2W	1.0	470	470	42.2K, 1%	4.87K, 1%	1.0	—	—	1K 1W	—	800264	800131	800265	800262
730126-03/-15 NFS200-7603/-7603M	100035-200 16A, 200V	BYV27-150	TIP42C	—	TL431.5	470PF, 1KV	680, 35V	0.1, 63V	0.47, 63V	680, 35V	0.1, 63V	1.0, 50V	1.0	22K	47 2W	1.0	470	470	18.7K, 1%	4.87K, 1%	1.0	—	—	220, 1W	—	800244	800131	800235	800263
730126-04/-16 NFS200-7608/-7608M	—	—	—	—	—	—	—	—	—	—	—	—	4.7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	800236

APPROVALS DESIGNED CHECKED ENG. DATE		DATE 1/1/78	
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730126-01/-24		SHEET 2 OF 2	

CAD GENERATED

REV.	ECO.	DESCRIPTION	DATE	APPD.
9F	14733	CONNECTION OF DRAWINGS PRELIMINARY RELEASE	11-27-89	7-1
9H	14917	INC.	3-20-90	11-1

SEE SHT 2



730126-XX NFS200-XXXX	PIN NO.	OUTPUT					
		1, 2	3, 4, 5	6	7	8	9
-01, -13 7601, 7601M		+5.1V	RETURN	+12.1V	-12.1V	-5.2V	-5.2V RETURN
-02, -14 7602, 7602M		+5.1V	RETURN	+12.1V	-12.1V	-24V AUX	+24V AUX
-03, -15 7603, 7603M		+5.1V	RETURN	+12.1V	-12.1V	-12.1V AUX	-12.1V AUX
-04, -16 7604, 7604M		+5.1V	RETURN	+12.1V	-12.1V	NOT USED	NOT USED

- * SEE COMPONENTS VALUE TABLE FOR SHEET 2.
- SEE TB2 OUTPUT TABLE.
- ALL DIODES ARE IN4448.
- ALL CAPACITANCE VALUES ARE IN MICROFARDS, VOLTAGES IN D.C.
- ALL RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.

7 FOR SCHEMATIC VALUES SEE DWG. NO. 780134-01.
6 FOR SCHEMATIC VALUES SEE DWG. NO. 780133-01.

VR4	NOT USED
U1	NOT USED
TS1	NOT USED
TB2	NOT USED
TZ	NOT USED
RT1	NOT USED
R93	NOT USED
LAST USED	NOT USED

Q17	NOT USED
P1	NOT USED
L15	NOT USED
JP18	NOT USED
J1	NOT USED
F2	NOT USED
CR42	NOT USED
C74	NOT USED
C2, 11, 32, 35, 37, 39, 41, 55, 57, 60, 61, 67	NOT USED
AZ	NOT USED
LAST USED	NOT USED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:

DO NOT SCALE DRAWING

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DATE: 11/1/89
BY: KEITH K. SANTO
CHECKED: 7-2-90
APPROVED: 7-2-90

SCALE: NONE

SHEET 1 OF 2

SCHEMATIC POWER SUPPLY NFS200-76XX

DWG. NO. 730126-01/-24

REV. C

Video Kit Data Ray 1059

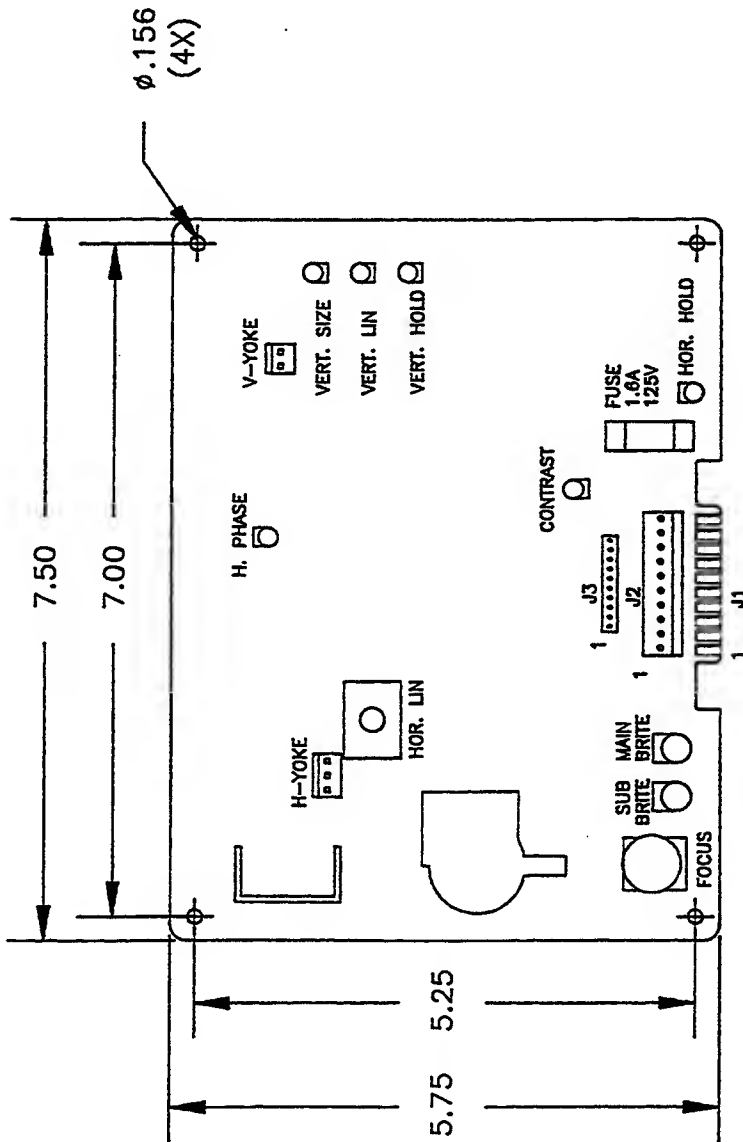
INTERFACE CONNECTOR PIN ASSIGNMENT

1. GND.
2. REMOTE BRIGHT. LOW
3. REMOTE BRIGHT. HIGH
4. REMOTE BRIGHT. WIPER
5. GND.
6. HORIZ. SYNC.
7. +12 VOLTS
8. VIDEO INPUT
9. VERT. SYNC.
10. GND.

INTERFACE CONNECTOR OPTIONS

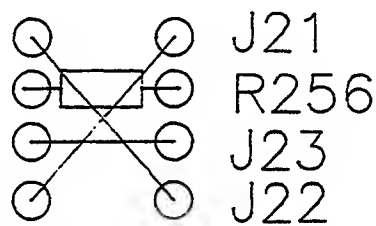
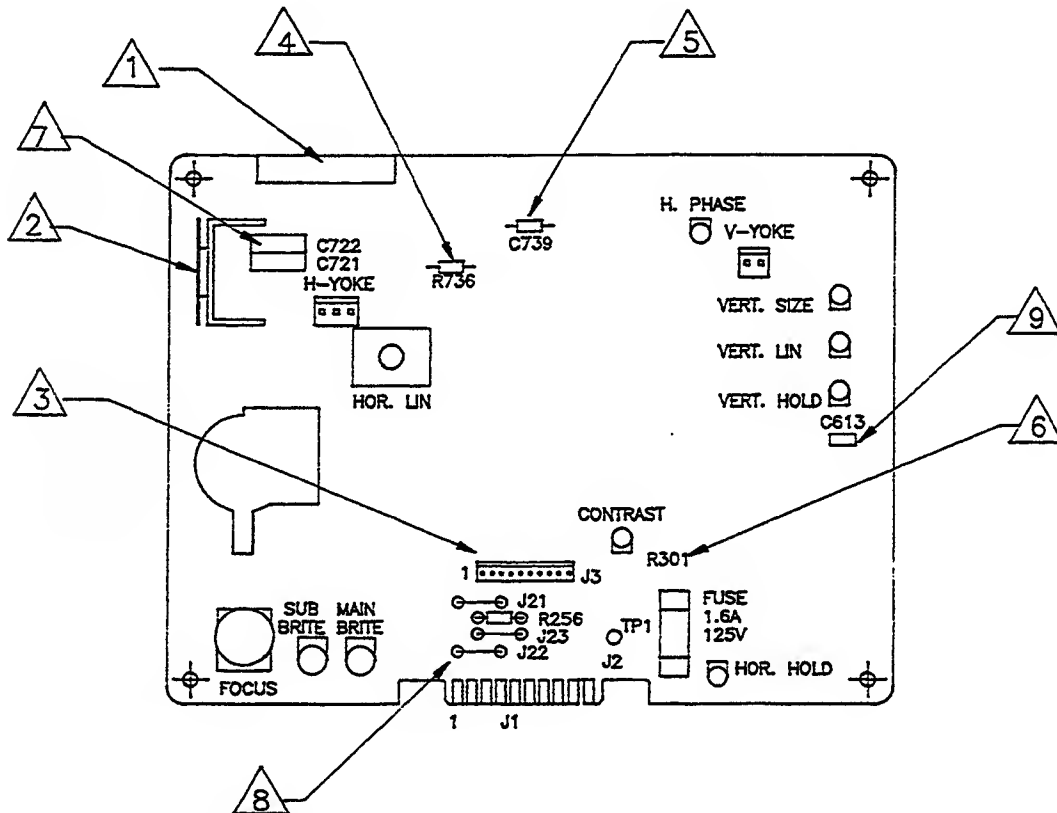
- J1 10 PIN CARD EDGE
 J2 MOLEX 26-48-1105 .156 CTR.
 (OR EQUIV.)
 J3 MOLEX 22-23-2101 .100 CTR.
 (OR EQUIV.)

MAX. COMPONENT HEIGHT: 3.20



CAD FILE NAME: 210103 2X TIME:		DATE:		UNLESS OTHERWISE STATED TAB IS -000	
MATERIAL:		TOLERANCES UNLESS OTHERWISE STATED .XXX=.005 DIMENSIONS ARE IN INCHES ANGULAR TOL $\pm 1^\circ$		TITLE OUTLINE DEFL. DR10	
FINISH:		DRAWN BY PB 6/28/89		DRAWING NO 210103	
INTERPRET DRAWING PER ANSI Y14.5M		CHECKER LS 6/28/89		REV 2X	
		PROJECT EE		USED ON: DR10	
		PROJECT ME		SCALE 1:2	
		ENG MGR		SHEET 1 OF 1	

REVISION



SINGLE LEVEL BILL OF MATERIALS BY REF ID
 PEGGY 740154 REV C 04/25/91
 ERJ 14:09:38
 PAGE: 1




REF. ID	PART NO.	DESCRIPTION	UM	MB	REV
Parent	740154	PWA DR1059 DEFL/VIDEO	EA	M	C
A001	740136	PWA DR10 DEFL/VIDEO WITH ARC-GND WIRE	EA	B	A
C722	520131	CAP .047uF 400V 5X NET POLYPROP 15mm	EA	B	A
C739	520169	CAP 120pF 1000V 10X CERAMIC SGN RAD	EA	B	A
H1	280101	INSULATOR 1.4"x1.6" FISHPAPER	EA	B	A
H2	716904001	COMPOUND RTV	GZ	B	C
J003	340101-010	CONN HDR 10 CIR .100 SP .025 SQ PC MNT STGT	EA	B	A
R301	540223	RES CF 1/4 82.00 5X	EA	B	A
R736	540285	RES CF 1/4 33.00K 5X	EA	B	A
----- END OF BILL -----					


SINGLE LEVEL BILL OF MATERIALS BY REF ID
 PEGGY 800000-027 REV B 09/12/90
 ENG 12:56:04
 PAGE: 1

REF. ID	PART NO.	DESCRIPTION	UM	MB	REV
Parent	800000-027	FINAL DR1059 FLUKE P/N 875612 KIT	EA	M	B
A01	740154	PWA DR1059 DEFL/VIDEO	EA	M	B
A02	380111	YOKE ASSY 90 DEG 20mm 140uh 11.5mh DR10	EA	B	A
A03	360118	ARC GROUND WIRE	EA	B	A
H01	701380513	LABEL CAUTION HI-V	EA	B	A
H02	110104-001	LABEL SERIAL NUMBER DRC LAB NEXT ASSY	EA	M	B
H03	130100-002	MAGNET BAR YEL	EA	B	A
H04	130100-003	MAGNET BAR RED	EA	B	A
H05	130102-004	MAGNET FLEX YEL 4G	EA	B	A
H06	130102-005	MAGNET FLEX GRN 11G	EA	B	A
H07	731950006	TAPE INSULATION GLASS .75 Inch WIDE	FT	B	A
H08	721900007	TERMINAL RING #6 UNINS 22-18 AWG	EA	B	B
H09	110134	LABEL BLANK .90"x.25"	EA	B	A
V01	400116	CRT 5X9 90 20 P31	EA	B	A
----- END OF BILL -----					

REPLACEMENT PARTS

SEMICONDUCTORS


SIMBOL	STOCK NO.	DESCRIPTION	
IC701	2915211	IC SILICON	μPG1379C
Q301	2320637	TRANSISTOR SILICON	2SA673 C/D
Q302	2321871	TRANSISTOR SILICON	2SD655 D
Q303	2322562	TRANSISTOR SILICON	2SC2688 K/M
Q701	2320596	TRANSISTOR SILICON	2SC458 C/D
Q703	2320647	TRANSISTOR SILICON	2SC1213 C/D
Q704 	2323991	TRANSISTOR SILICON	2SD1163
Q771 	2390022	THYRISTOR SILICON	M21C (Y)
Q781	2322562	TRANSISTOR SILICON	2SC2688 K/L
D251	2334581	DIODE SILICOM	ES1A
D301	2331912	DIODE SILICOM	1SS82
D302	2331912	DIODE SILICOM	1SS82
D602	2332851	DIODE SILICOM	EH1Z
D702	2333001	DIODE SILICOM	RU2M
D703	0J00801	DIODE SILICOM	RU4M
D705	2334581	DIODE SILICOM	ESA1
D741	2334592	DIODE SILICOM	EM1Z
D751	Y290365	DIODE SILICOM	ES01F
D781	2330351	DIODE SILICOM	1S2076
ZD251	0J00021	DIODE SILICOM	HZ27-1
ZD601	0J00811	DIODE SILICOM	RD2.4EB2
ZD602	2331797	DIODE SILICOM	HD5C-1
ZD603	2331797	DIODE SILICOM	HD5C-1
ZD771 	2332001	DIODE SILICOM	HZ36-1


Components marked with a  have special characteristics important to safety

ISSUE 1/7

DR6	DWN.	K. Takahashi Feb. 9 '90	TITLE CDU-12XX61 REPLACEMENT PARTS LIST (11'-12'-125)	Hitachi, Ltd. Tokyo Japan	YOKOHAMA WORKS DWG. NO 27
	CHKD.	J. Takahashi			
	APPD.	K. abur			

RESISTORS

SIMBOL	STOCK NO.	DESCRIPTION			
R251 	0119505S	FUSE RESISTOR	2.2Ω	±5%	RN1/4W
R253	0100095G	CARBON FILM	18KΩ	±5%	RD1/8W
R254	0150650	CONTROL	100KΩ-B	±20%	0.2W
R255	0150650	CONTROL	100KΩ-B	±20%	0.2W
R256	0100117G	CARBON FILM	150KΩ	±5%	RD1/8W
R257	0100107G	CARBON FILM	56KΩ	±5%	RD1/8W
R258	0113787G	CARBON FILM	33KΩ	±5%	RD1/2W
R268	0113733G	CARBON FILM	220Ω	±5%	RD1/2W
R302	0100029G	CARBON FILM	33Ω	±5%	RD1/8W
R303	0100069G	CARBON FILM	1.5KΩ	±5%	RD1/8W
R304	0100067G	CARBON FILM	1.2KΩ	±5%	RD1/8W
R305	0100069G	CARBON FILM	1.5KΩ	±5%	RD1/8W
R306	0100025G	CARBON FILM	22Ω	±5%	RD1/8W
R307	0113725G	CARBON FILM	100Ω	±5%	RD1/2W
R308	0100059G	CARBON FILM	560Ω	±5%	RD1/8W
R309	0100029G	CARBON FILM	33Ω	±5%	RD1/8W
R310	0150151	CONTROL	500Ω-B	±20%	0.1W
R311	0110245S	METAL OXIDE FILM	1KΩ	±5%	RS2W
R314	0113725G	CARBON FILM	100Ω	±5%	RD1/2W
R602	0100055G	CARBON FILM	1KΩ	±5%	RD1/8W
R603	0100055G	CARBON FILM	1KΩ	±5%	RD1/8W
R604	0100089G	CARBON FILM	10KΩ	±5%	RD1/8W
R605	0100089G	CARBON FILM	10KΩ	±5%	RD1/8W
R606	0150156	CONTROL	10KΩ-B	±20%	0.1W
R607	0100099G	CARBON FILM	27KΩ	±5%	RD1/8W
R608	0100098G	CARBON FILM	24KΩ	±5%	RD1/8W
R609	0100081G	CARBON FILM	4.7KΩ	±5%	RD1/8W
R610	0100103G	CARBON FILM	39KΩ	±5%	RD1/8W
R611	0100079G	CARBON FILM	3.9KΩ	±5%	RD1/8W
R612	0113703G	CARBON FILM	12Ω	±5%	RD1/2W
R613	0113684G	CARBON FILM	2.2Ω	±5%	RD1/2W
R615	0150151	CONTROL	500Ω-B	±20%	0.1W
R616	0150151	CONTROL	500Ω-B	±20%	0.1W

Components marked with a  have special characteristics important to safety.

ISSUE 2

DWN K. KAWAZU Feb 9 90

CHKD J. Takahashi

TITLE CDU-12XX61
REPLACEMENT
PARTS LIST



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YOKOHAMA WORKS DWG. NO

27

DR7

RESISTORS

SIMBOL	STOCK NO.	DESCRIPTION			
R618	0110233S	METAL OXIDE FILM	330Ω	±5%	RS2W
R620	0113742G	CARBON FILM	470Ω	±5%	RD1/2W
R621 	0A01331	FUSE RESISTOR	4.7Ω	±5%	RN1/6W
R702	0100065G	CARBON FILM	1KΩ	±5%	RD1/8W
R704	0100060G	CARBON FILM	620Ω	±5%	RD1/8W
R709	0100075G	CARBON FILM	2.7KΩ	±5%	RD1/8W
R710	0100025G	CARBON FILM	22Ω	±5%	RD1/8W
R711	0100065G	CARBON FILM	1KΩ	±5%	RD1/8W
R712	0100065G	CARBON FILM	1KΩ	±5%	RD1/8W
R713	0100099G	CARBON FILM	27KΩ	±5%	RD1/8W
R714	0100083G	CARBON FILM	5.6KΩ	±5%	RD1/8W
R715	0100073G	CARBON FILM	2.2KΩ	±5%	RD1/8W
R716	0100089G	CARBON FILM	10KΩ	±5%	RD1/8W
R717	0150155	CONTROL	5KΩ-B	±20%	0.1W
R718	0113739G	CARBON FILM	390Ω	±5%	RD1/2W
R719	0100041G	CARBON FILM	100Ω	±5%	RD1/8W
R721	0100041G	CARBON FILM	100Ω	±5%	RD1/8W
R722	0110219S	METAL OXIDE FILM	82Ω	±5%	RS2W
R725 	0119514S	FUSE RESISTOR	10Ω	±5%	RN1/4W
R732	0100085G	CARBON FILM	6.8KΩ	±5%	RD1/8W
R734	0100101G	CARBON FILM	33KΩ	±5%	RD1/8W
R735	0100099G	CARBON FILM	27KΩ	±5%	RD1/8W
R751	0113815G	CARBON FILM	470KΩ	±5%	RD1/2W
R753	0A00511	CONTROL	2MΩ-B	±20%	0.5W
R754	0113815G	CARBON FILM	470KΩ	±5%	RD1/2W
R755	0113815G	CARBON FILM	470KΩ	±5%	RD1/2W
R756	0113774G	CARBON FILM	10KΩ	±5%	RD1/2W
R757	0113815G	CARBON FILM	470KΩ	±5%	RD1/2W
R767	0113744G	CARBON FILM	560Ω	±5%	RD1/2W
R771	0113803G	CARBON FILM	150KΩ	±5%	RD1/2W
R772	0100099G	CARBON FILM	27KΩ	±5%	RD1/8W
R773	0100081G	CARBON FILM	4.7KΩ	±5%	RD1/8W
R774	0100025G	CARBON FILM	22Ω	±5%	RD1/8W

Components marked with a  have special characteristics important to safety

ISSUE

3

DWN. K. TAKAHASHI Feb. 9 '90

CHKD. J. Takahashi

APPD. H. A. G.


TITLE CDU-12XX61
REPLACEMENT
PARTS LIST
(110-111-112K)


Hitachi, Ltd.
Tokyo Japan

YOKOHAMA WORKS DWG. NO

27

RESISTORS

SYMBOL	STOCK NO.	DESCRIPTION			
R781	0100079G	CARBON FILM	3.9K Ω	$\pm 5\%$	RD1/8W
R782	0100083G	CARBON FILM	5.6K Ω	$\pm 5\%$	RD1/8W
R783	0100073G	CARBON FILM	2.2K Ω	$\pm 5\%$	RD1/8W
R785	0113799G	CARBON FILM	100K Ω	$\pm 5\%$	RD1/2W
R791	0100099G	CARBON FILM	27K Ω	$\pm 5\%$	RD1/8W
R792	0150155	CONTROL	5K Ω -B	$\pm 20\%$	0.1W
R793	0100041G	CARBON FILM	100 Ω	$\pm 5\%$	RD1/8W
R901	0A00941S	METALLIZED FILM	0.22 Ω	$\pm 5\%$	RN1W
R951 	0119687S	FUSE RESISTOR	4.7 Ω	$\pm 5\%$	RN1/4W

Components marked with a  have special characteristics important to safety

ISSUE

4

DWN. K. TAKAHASHI Feb 9, '90
CHKD. J. Takahashi

TITLE CDU-12XX61
REPLACEMENT
PARTS LIST

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YOKOHAMA WORKS DWG. NO.

27

DR9

CAPACITORS

SYMBOL	STOCK NO.	DESCRIPTION			
C251	0253290F	ELECTROLYTIC	100 μ F	$\pm 20\%$	DC100V
C252	0253972F	ELECTROLYTIC	10 μ F	$\pm 20\%$	DC250V
C253	0244541F	CERAMIC	0.01 μ F	$\pm 10\%$	DC500V
C254	0253912F	ELECTROLYTIC	1 μ F	$\pm 20\%$	DC100V
C301	0252945F	ELECTROLYTIC	47 μ F	$\pm 20\%$	DC16V
C302	0252960F	ELECTROLYTIC	10 μ F	$\pm 20\%$	DC25V
C303	0248688F	CERAMIC	150PF	$\pm 5\%$	DC50V
C601	0276262F	POLYESTER FILM	6800PF	$\pm 10\%$	DC50V
C602	0244139F	CERAMIC	1000PF	$\pm 10\%$	DC50V
C604	0252946F	ELECTROLYTIC	100 μ F	$\pm 20\%$	DC16V
C605	0276373F	METALLIZED POLYESTER FILM	1 μ F	$\pm 10\%$	DC63V
C606	0255946F	ELECTROLYTIC	100 μ F	$\pm 20\%$	DC16V
C607	0292716F	TANTALUM	1 μ F	$\pm 10\%$	DC20V
C608	0252950F	ELECTROLYTIC	10 μ F	$\pm 20\%$	DC25V
C609	0252950F	ELECTROLYTIC	1000 μ F	$\pm 20\%$	DC16V
C610	0276267F	POLYESTER FILM	0.047 μ F	$\pm 10\%$	DC50V
C611	0276263F	POLYESTER FILM	0.01 μ F	$\pm 10\%$	DC50V
C613	0244109F	CERAMIC	4700PF	$\pm 10\%$	DC50V
C614	0252949F	ELECTROLYTIC	470 μ F	$\pm 20\%$	DC16V
C710	0276269F	POLYESTER FILM	0.1 μ F	$\pm 10\%$	DC50V
C711	0252974F	ELECTROLYTIC	1 μ F	$\pm 20\%$	DC50V
C713	0276259F	POLYESTER FILM	0.1 μ F	$\pm 10\%$	DC50V
C714	0276261F	POLYESTER FILM	4700PF	$\pm 10\%$	DC50V
C715	0276253F	POLYESTER FILM	0.01 μ F	$\pm 10\%$	DC50V
C716	0252974F	ELECTROLYTIC	1 μ F	$\pm 20\%$	DC50V
C717	0299619F	POLYPROPYLENE FILM	5600PF	$\pm 5\%$	DC630V
C718	0252945F	ELECTROLYTIC	47 μ F	$\pm 20\%$	DC16V
C719 	0276266F	POLYESTER FILM	0.033 μ F	$\pm 5\%$	DC50V
C721 	0299993F	POLYPROPYLENE FILM	0.018 μ F	$\pm 5\%$	DC630V
C722	0299994F	POLYPROPYLENE FILM	0.022 μ F	$\pm 5\%$	DC630V
C724	0259192	ELECTROLYTIC (BP)	6.8 μ F	$\pm 20\%$	DC50V
C725	0253978F	ELECTROLYTIC	2.2 μ F	$\pm 20\%$	DC350V

Components marked with a  have special characteristics important to safety

ISSUE

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DWN.

K. TAKAHASHI Feb 9 90

CHKD.

T. Takahashi

TITLE CDU-12XX61
REPLACEMENT
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Tokyo Japan

YOKOHAMA WORKS DWG NO

DR10

27

CAPACITORS

SYMBOL	STOCK NO.	DESCRIPTION			
C726	0244501F	CERAMIC	1000PF	±10%	DC500V
C729	0252949F	ELECTROLYTIC	470 μ F	±20%	DC16V
C730	0252950F	ELECTROLYTIC	1000 μ F	±20%	DC16V
C738	0244171F	CERAMIC	0.01 μ F	±20%	DC50V
C751	0244213	CERAMIC	1500PF	±10%	DC2KV
C752	0249462	CERAMIC	1000PF	±10%	DC1KV
C771	0252974F	ELECTROLYTIC	1 μ F	±20%	DC50V
C781	0276267F	POLYESTER FILM	0.047 μ F	±10%	DC50V
C782	0244139F	CERAMIC	1000PF	±10%	DC50V
C783	0244501F	CERAMIC	1000PF	±10%	DC500V
C791	0276262F	POLYESTER FILM	6800PF	±10%	DC50V
C901	0252946F	ELECTROLYTIC	100 μ F	±20%	DC16V
C951	0252945F	ELECTROLYTIC	47 μ F	±20%	DC16V

Components marked with a  have special characteristics important to safety

ISSUE	6
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DWN. K. TAKAHASHI Feb. 9, '90 TITLE CDU-12XX61
CHKD T. Z. L. 1 REPLACEMENT

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YOKOHAMA WORKS DWG. NO.

27

DR11

MISCELLANEOUS

SIMBOL	STOCK NO.	DESCRIPTION	
T701	2165441	HOR. DRIVE TRANSFORMER	
T702 \triangle	Y261701	FRYBACK TRANSFORMER	
L302	2122237T	PEAKING COIL	4.7 μ H
L705	2163861	HOR. ADJUSTABLE LINEARITY COIL	
FB701	2123851	FERRITE BEAD	
F901 \triangle	1J00041	FUSE	1.6A
NE301 \triangle	2340741-	NEON GAP	
SG251 \triangle	2340871	SPARK GAP	
SG751 \triangle	2340871	SPARK GAP	
SG752 \triangle	2340871	SPARK - GAP	
	2661756	PLUG(1P)	
	2668601	PLUG(2P)	
	2668602	PLUG(3P).	
	2954851	CRT SOCKET	
	2950821	TEST POINT PIN	
	4210626	TR HEAT SINK	
	4336401	TR HEAT SINK	
	3C03231	DIODE HEAT SINK	
	2721351	FUSE HOLDER	
	1601081	CRT GROUND WIRE	
	1601551	DEFLECTION YOKE	

Components marked with a \triangle have special characteristics important to safety

ISSUE	7
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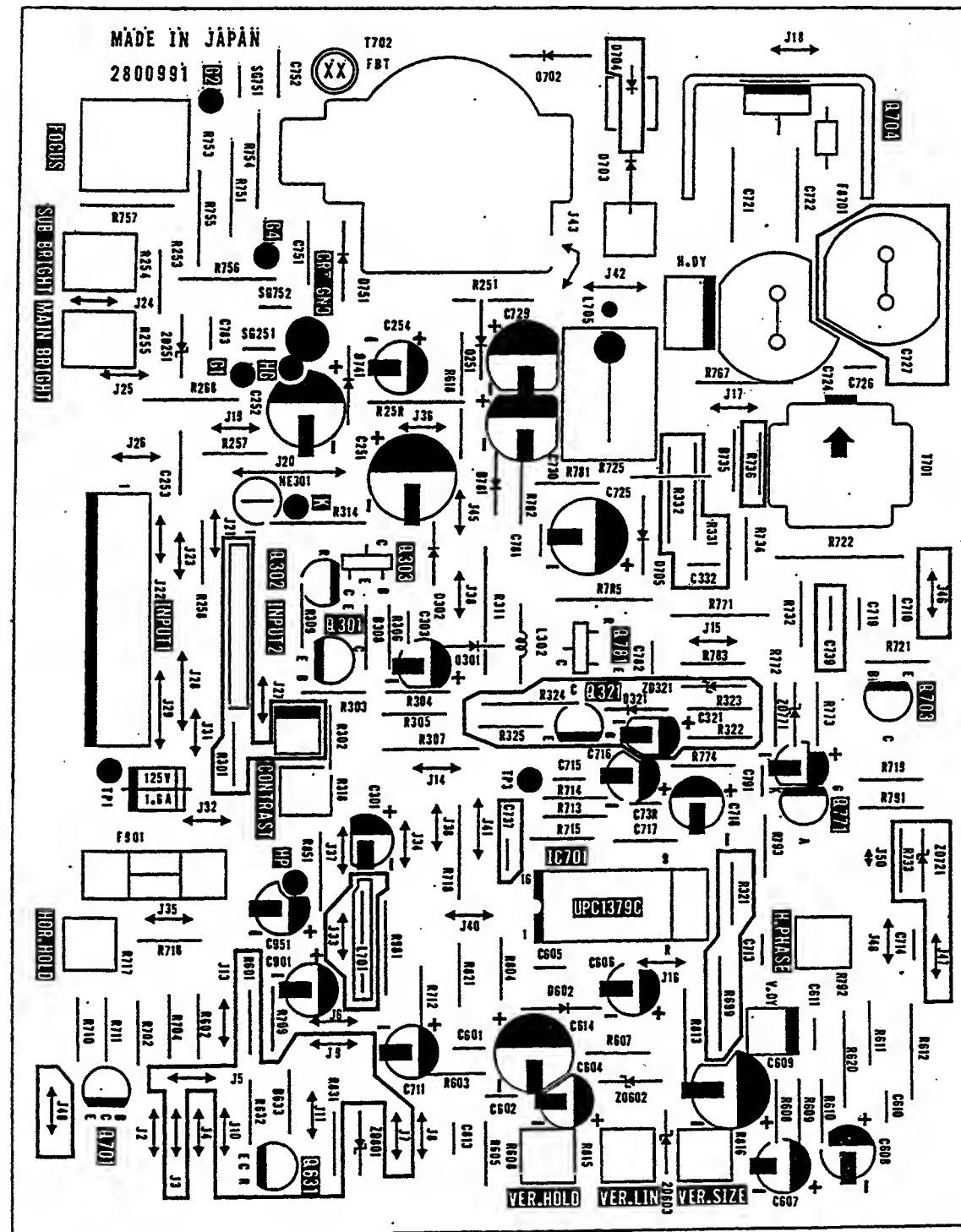
DWN.	K. BAKAHI	Feb 9, 90
CHKD.	T. Takahashi	
APPD.	K. W. L.	

TITLE	CDU-12XX61
REPLACEMENT	PARTS LIST
	(110-11-1151)

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YOKOHAMA WORKS DWG. NO

27



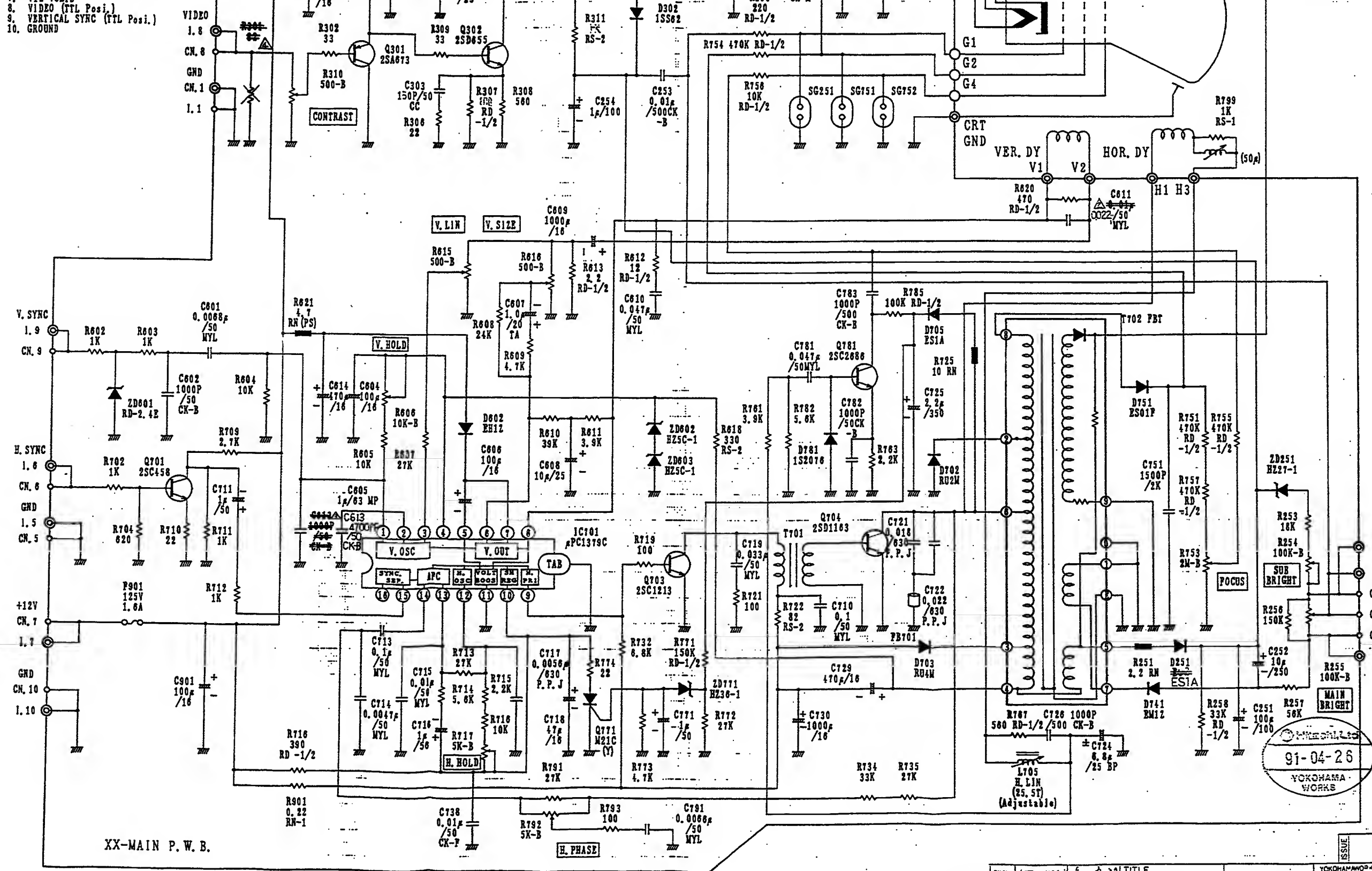
08680M2Z

- (Both connector 1 CN)
Pin# SIGNAL NAME
1. GROUND
 2. REMOTE BRIGHTNESS (LOW)
 3. REMOTE BRIGHTNESS (HIGH)
 4. REMOTE BRIGHTNESS (WIPER)
 5. GROUND
 6. HORIZONTAL SYNC (TTL Posi.)
 7. +12 VOLTS
 8. VIDEO (TTL Posi.)
 9. VERTICAL SYNC (TTL Posi.)
 10. GROUND

CRT
CE810M12P31GR
CLINTON

REV	REVISIONS	DATE	BY	CHKD	APPD
1	RENEW	12/28/81	Y. T.		
2	Change C611 0.0022 to 0.0025 and R751 value	1/15/82	Y. T.		

REV	REVISIONS	DATE	BY	CHKD	APPD
1	C6A Change 1000P to 1000P R301 Delete	DEC. 1981	Y. T.		
2	32	1/11/82	Y. T.		



91-04-26
YOKOHAMA WORKS

OWN	Y. T.	DATE	12/28/81	TITLE	3-12-81
CHKD	Y. T.	DATE	1/15/82	TITLE	Schematic
APPD	Y. T.	DATE	1/15/82	TITLE	Schematic

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W083930

Section 10

1711A/AA Communication/Measurement System

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10-1. INTRODUCTION

In function, the 1711A/AA is very similar to the 1752A. Most of the same internal optional assemblies can be used, and most programming commands and responses are the same. Unlike the 1752A, the 1711A/AA is not equipped with its own display, keyboard, or floppy drive. This configuration allows the user added flexibility in using any of a variety of terminals, located at any desired location relative to the mainframe (or no terminal at all.) Compatible terminals include the Fluke 10XX series and 1780A, or VT-100/ANSI equivalents. An external floppy drive unit (Model 1760A/AA) is available if desired. The 1711A/AA has five more option slots than the 1752A (total of 10), offering more memory and I/O option space. The User Defined output, which does not occupy an option slot, offers eight general-purpose output bits.

The 1711A/AA uses the 1752A SBC (Single Board Computer) along with specialized BOOT chips that recognize the special nature of the 1711A/AA and its configuration file, CONFIG.SYS. In theory, a 1752A can become functionally similar to a 1711A/AA by simply operating without the VGK board, in which case the serial port automatically becomes the console. However, without the 1711A/AA BOOT chips, operational abilities would be limited, and the touch screen and display would be unusable.

FDOS is similar for the 1752A and the 1711A/AA. However, with the VGK left out and the User Defined Board added in the 1711A/AA, the distribution floppies differ in the programs and drivers included. The System Diagnostic (SD) disk is significantly different from the 1752A SD disk because of the heavy use of graphics in the program displays. Whereas the 1752A uses the internal VGK and display, the 1711A/AA SD uses only the 102X, 103X, and 105X series Touch Sensitive Displays (TSD). The 1711A/AA SD will not function with 1780A, VT-100, or other ANSI terminals.

The 1711A/AA can use the following optional assemblies:

- **1760A/AA Floppy Drive**

The 1760A/AA is an optional floppy drive for the 1711A/AA. It uses a longer cable, but is otherwise connected to the SBC in the same manner as the floppy drive in the 1752A. The 1760A/AA is powered by its own dual range ac power supply. This power supply is a standard linear supply using common three-terminal regulators to supply +5V and +12V power to the floppy drive.

- **1711A/AA-440 40M-Byte Hard Disk**

The 1711A/AA-440 is an optional 40M-byte hard disk. It is operationally identical to the 1722A-440

and differs only in its physical arrangement. The 1711A/AA motherboard does not accommodate the SCSI bus. Therefore, the interface card, the hard drive, and an interconnecting SCSI cable are all contained on one slide-in module. This "sandwich" requires 3 slots. For further details, refer to 1722A/1752A-440 information in Section 6.

The information presented here primarily describes the items that are unique to the 1711A/AA. Refer to the following other manuals for additional information:

- 1752A System Guide (descriptions of common features and components)
- 1711A/AA System Guide (Section 0) for other operational details

10-2. THEORY OF OPERATION

Refer to Section 2 of this manual.

10-3. MAINTENANCE

Refer to Section 3 of this manual.

10-4. LIST OF REPLACEABLE PARTS

Refer to Section 4 for parts lists of the 1711A/AA-440, options, and the A3 and A4 modules. Parts lists for the 1711A/AA, A2 module, A5 module, A19 module, and the 1760A/AA are included here in Section 10.

10-5. Manual Status Information

Assembly revision levels are documented in the "Manual Status Information" table later in this section. To identify the configuration of the pca's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pca.

10-6. Newer Instruments

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

10-7. SCHEMATIC DIAGRAMS

Schematic diagrams unique to the 1711A/AA are included at the end of this section. Refer to Section 5 for schematics that are used in common.

1711A/AA Communication/Measurement System**PARTS LIST****Manual Status Information**

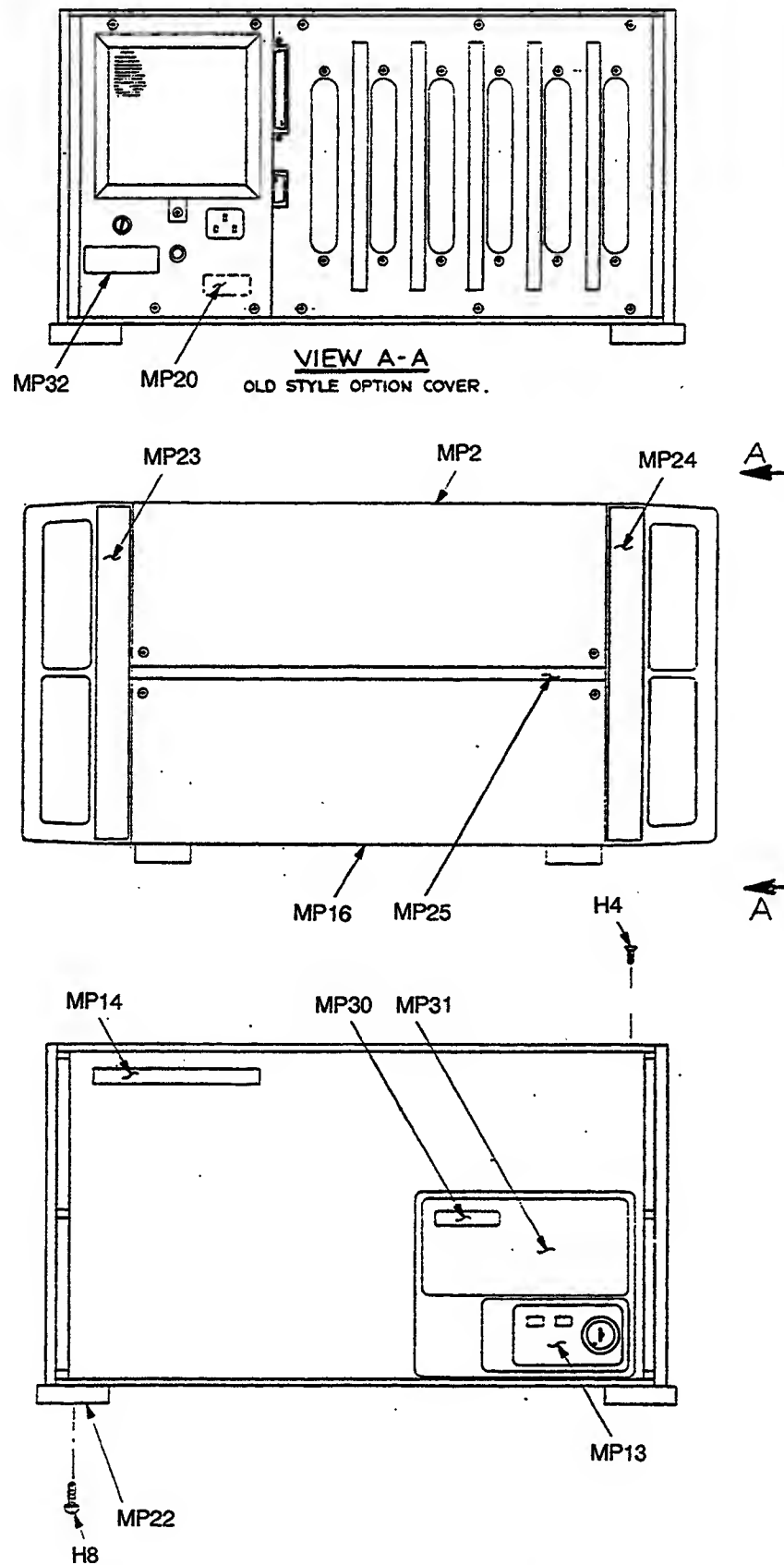
REF	ASSEMBLY NAME	FLUKE P/N	REVISION LEVEL
A1	Video/Graphics/Keyboard (VGK) Interface Module	897483	M
A2	Motherboard PCA	699066	J
A3	Power-Up (PUP) PCA	704353	B
A4	Single-Board Computer (SBC) Module	805002 804997	N
002	Parallel Interface	717397	
004	Magnetic Bubble Memory	777235	
005	Magnetic Bubble Memory	777391	
006	256K RAM Expansion Module	718684	F
007	512K RAM Expansion Module	718692	F
008	IEEE-488/RS-232-C Interface Module	718221	F
009	Dual Serial Interface	718734	B
010	Analog Measurement Processor	736876	F
011	Analog Output Module	610329	H
012	Counter Totalizer Module	630186	E
013	1752A-013 Mainframe Interface Assembly	749242	
016	1M RAM Expansion Module	794727	C
017	2M RAM Expansion Module	794735	C
018	256K Non-Volatile Memory (NVRAM)	804088	-
019	512K Non-Volatile Memory (NVRAM)	804096	-
020	1M Non-Volatile Memory (NVRAM)	819045	C
440	1722A-440 Winchester Hard Disk, 40M-Byte	862412	(all)
V7800	Multifunction Board	882303	
V7800-002W	Wide Slot Analog Output Expansion	882402	
V7800-004W	Wide Slot Digital Output Expansion	882407	
V7800-040W	Wide Slot Analog Input Multiplexer Master	882410	
V7800-041	Analog Input Multiplexer Slave	882360	

Table 10-1. 1711A/AA Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 2	MOTHERBOARD PCA	825331	89536	825331	1	
A 3	⚡ POWER-UP (PUP) PCA	704353	89536	704353	1	1
A 4	⚡ SINGLE BOARD COMPUTER (SBC) PCA		89536		1	2
A 5	⚡ FRONT PANEL PCA	801506	89536	801506	1	
A 19	⚡ USER DEFINED DRIVER PCA	825257	89536	825257	1	
B 1	FAN, AXIAL, 24VDC, 80 CFM, 120MM, LO NOISE	615021	0J468	FBH12G24H	1	
BT 1	PWR SUP, 150W, +5V, ±12V, +24V	805135	89536	805135	1	
E 1	GROUNDING CONTACT STRIP	580779	89536	580779	1	
E 2	BINDING POST, PLATED	102707	89536	102707	1	
E 3	BINDING HEAD, PLATED	102889	89536	102889	1	
E 4	TERM, FASTON, TAB, .250, SOLDER	422790	00779	42822-4	1	
F 1	FUSE, .25X1.25, 3A, 250V, FAST	109199	71400	AGC-3	1	
FL 1	FILTER, LINE, 115V/2.5A, 220V/2.5A	806885	0GV52	FN680-2.5/06	1	
H 1	WASHER, LOCK, INTRNL, STL, .150ID	110338	73734	1304	4	
H 2	SCREW, PH, P, THD CUT, STL, 6-32, .250	114942		COMMERCIAL	4	
H 3	SCREW, PH, P, LOCK, STL, 4-40, .375	276709	74594	276709	6	
H 4	SCREW, PH, P, LOCK, SS, 6-32, .250	320093	74594	320093	26	
H 5	SCREW, PH, P, LOCK, STL, 6-32, .312	152157	73734	19043	22	
H 6	SCREW, PH, P, SEMS, STL, 6-32, .375	177022		COMMERCIAL	8	
H 7	WASHER, FLAT, MYLAR, .165, .285, .010	197426	86928	5622-68-10	3	
H 8	SCREW, PH, P, SEMS, STL, 6-32, .500	177030		COMMERCIAL	10	
H 9	SCREW, PH, P, LOCK, STL, 8-32, .375	114124	89536	114124	8	
H 10	SCREW, PH, P, LOCK, STL, 8-32, .375	114116	89536	114116	14	
H 11	SCREW, PH, P, LOCK, STL, 8-32, .500	114355	19451	114363	6	
H 12	SCREW, PH, P, LOCK, STL, 8-32, .625	114983	73734	19067	4	
H 13	SCREW, CAP, SCKT, STL, 8-32, .625	448431	6W060	10097-98-C-10	8	
H 14	RIVET, PUSH, NYLON, 0.187X0.312-0.440	820597	89536	820597	2	
H 15	NUT, CAP, EXT LOCK, STL, 4-40	195255	78189	501-040800-00	16	
H 16	NUT, EXT LOCK, STL, 6-32, .3440D	152819	78189	501-060800-00	4	
H 17	NUT, HEX, LOCK, SS, 8-32	542969	72962	RM52LH3324-82	4	
H 18	NUT, HEX, BR, 1/4-28	110619		COMMERCIAL	4	
H 19	NUT, HEX, STL, 3/8-32	110510		COMMERCIAL	1	
H 20	NUT, SELF-THD, STL, .187 STUD	529347		COMMERCIAL	4	
H 21	WASHER, FLAT, SS, .125, .317, .030	146225	86928	5710-18-30-P	2	
H 22	WASHER, FLAT, SS, BLK, .171, .312, .030	474650	89536	474650	12	
H 23	WASHER, FLAT, SS, .174, .375, .030	176743	86928	5710-31-30-P	4	
H 24	WASHER, LOCK, SPLIT, STL, .168, .307, .040	111070	86928	5850-8-3	12	
H 25	WASHER, LOCK, INTRNL, STL, .387ID	129957	78189	1220-05	1	
H 26	CONN ACC, D-SUB, JACK SCREW, 4-40	448092	08718	D-20418-2	2	
H 27	FAN ACC, FILTER, AL W/FOAM	542118	31522	T-3500	1	
H 28	WASHER, LOCK, INTRNL, STL, .123ID	110403		COMMERCIAL	2	
H 29	NUT, HEX, STL, 4-40	184044		COMMERCIAL	2	
J 1	PWR PLUG PART, HOUSING	474668	27264	15-04-0703	1	
J 2	SOCKET, 1 ROW, 0.100 CTR, 2 POS	602706	00779	640442-2	1	
MP 1	REAR PANEL, FAN MOUNTING	801555	89536	801555	1	
MP 2	TOP COVER	801480	89536	801480	1	
MP 3	BULKHEAD	801530	89536	801530	1	
MP 4	FRONT BEZEL BRACKET	801548	89536	801548	1	
MP 5	EMI SHIELD	801449	89536	801449	1	
MP 6	CARD CAGE COVER	825026	89536	825026	1	
MP 7	SPACER PLATE	801456	89536	801456	2	
MP 8	CHROMATED SS FILLER PLATE	872804	89536	872804	10	
MP 9	PLATE, BLANK, .70 X 7.32	802603	89536	802603	10	
MP 10	FRONT BEZEL	801571	89536	801571	1	
MP 11	CARD GUIDE, MODIFIED	801563	89536	801563	2	
MP 12	PANEL, CABLE ACCESS	848882	89536	848882	1	
MP 13	FRONT PANEL DECAL	801597	89536	801597	1	
MP 14	DECAL, NAMEPLATE	825018	89536	825018	1	
MP 15	CHASSIS SIDE	486712	89536	486712	2	
MP 16	COVER, BOTTOM	486738	89536	486738	1	
MP 17	FILTER, HOUSING	718353	89536	718353	1	
MP 18	VENTED BRACKET, CARD TRAY	826578	89536	826578	1	
MP 19	PANEL, FRONT	717553	89536	717553	1	
MP 21	CORNER HANDLE, FRONT 8.75 INCH,	656199	89536	656199	4	
MP 22	FOOT, SINGLE BAIL TYPE (DARK UMBER)	653923	89536	653923	4	
MP 23	DECAL, FRONT CORNER	659243	89536	659243	2	
MP 24	DECAL, REAR CORNER	685180	89536	685180	2	
MP 25	SIDE TRIM-15"	525980	89536	525980	2	
MP 26	PLATE, BLANK	849240	89536	849240	5	
MP 27	LOCK & KEY, MODIFIED	655670	89536	655670	1	
MP 28	HLDR PART, FUSE, BODY 1/4X1-1/4, 5X20MM	460329	61935	031.1673	1	
MP 29	HLDR PART, FUSE, CAP, 1/4X1-1/4	460238	61935	031.1666	1	
MP 30	NAMEPLATE, FLUKE (DARK PEWTER)	728055	89536	728055	1	
MP 31	DECAL, FRONT PANEL	722215	89536	722215	1	
MP 32	DECAL, POWER REQUIREMENTS	897665	89536	897665	1	

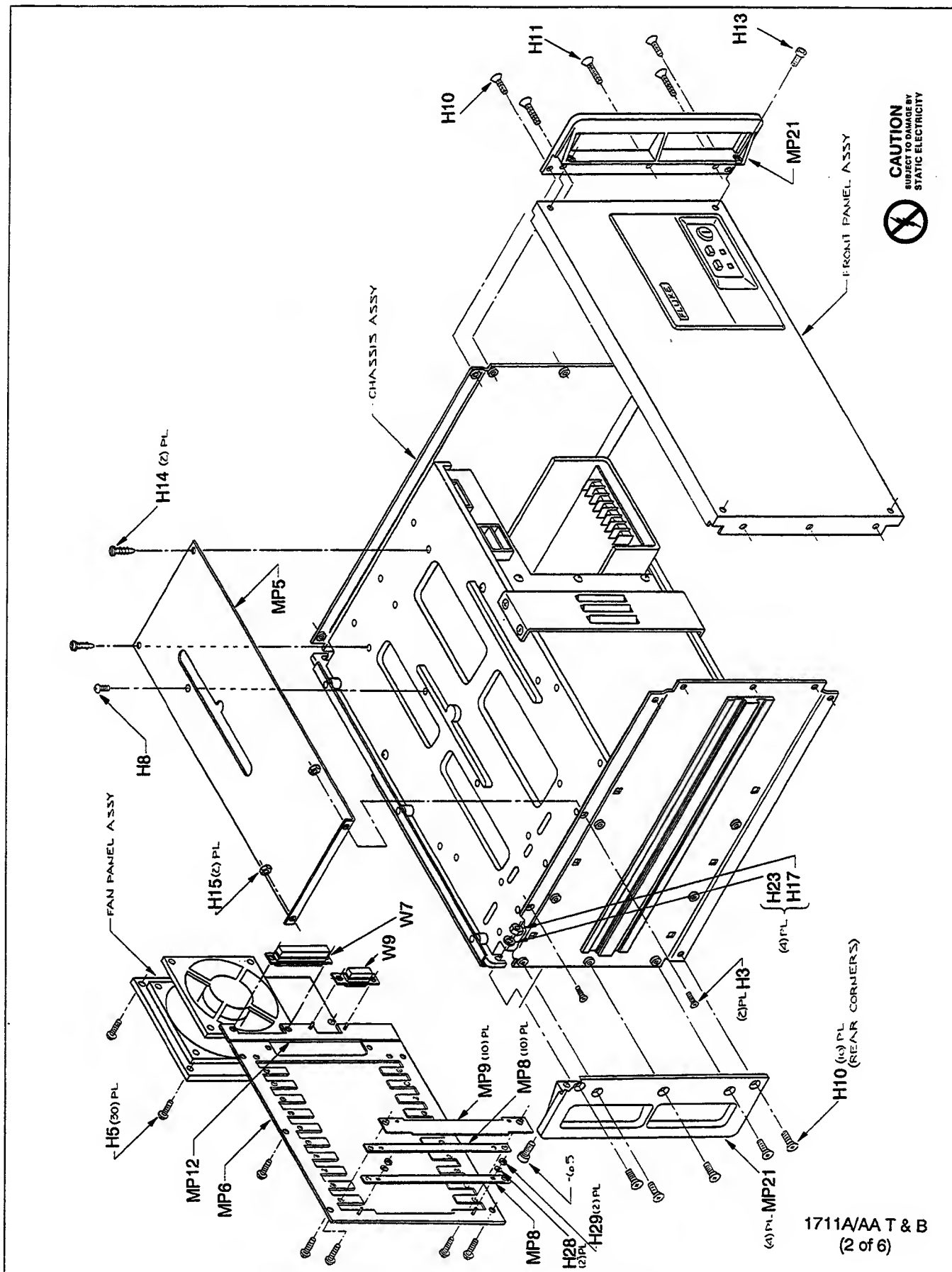
Table 10-1. 1711A/AA Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NO TE S
MP 33	SPACER, SNAP, FWB, NYL, .250	649723	89536	649723	4	
MP 34	GROMMET, SLOT, RUBBER, .625, .062	100073	83330	2149	1	
MP 35	CABLE TIE ANCHOR, ADHSV, .160TIE	407908	06383	ABMM-A-C	3	
MP 36	CABLE ACCESS, TIE, 4.00L, .10W, .75 DIA	172080	06383	SST-1M	3	
MP 37	SLEEV, POLYOL, SHRINK, .750-.375ID, BLACK	226365	88690	AF	1	
MP 38	FILLER PLATE, TOP WING	882477	89536	882477	10	
MP 39	FILLER PLATE, BOTTOM WING	884684	89536	884684	10	
MP 40	TAPE, FOAM, ADHSV, 1"W, 1/2 THK	229005	73734	117208	17	
MP 41	LABEL, RESTRICTED RIGHTS	722819	89536	722819	2	
MP 42	LABEL, SYSTEM DISK	707794	89536	707794	1	
MP 43	LABEL, DIAGNOSTIC DISK	707802	89536	707802	1	
MP 44	TLC FLOPPY DISK POCKET	650473	89536	650473	1	
MP 45	GROUND STRIP, BECU, SPRING FINGER	807891	34641	97-521-17	1	
MP 46	DISK, SYSTEM	835033	89536	835033	1	
MP 47	DISK, DIAGNOSTIC	826628	89536	826628	1	
S 1	ROTARY SWITCH	604488	34114	604488	1	
TM 1	DATA ACQUISITION & CONTROL MANUAL	826438	89536	826438	1	
TM 2	1711A/AA SYSTEM GUIDE MANUAL	825380	89536	825380	1	
U 1	PROGRAMMED PAL	805036	89536	805036	1	
W 1	WIRE HARNESS, POWER SUPPLY	804229	89536	804229	1	
W 2	CABLE, AC KEYSWITCH-POWER SUPPLY	804633	89536	804633	1	
W 3	CABLE, AC LINE FILTER-KEYSWITCH	804658	89536	804658	1	
W 4	CABLE SET, REAR PANEL	804674	89536	804674	1	
W 5	CABLE ASSY., FRONT PANEL	804880	89536	804880	1	
W 6	WIRE SET	804989	89536	804989	1	
W 7	CABLE, DISK DRIVE	824979	89536	824979	1	
W 8	FLOPPY DISK DRIVE TERMINATOR	825000	89536	825000	1	
W 9	CABLE, INTERNAL USER DEFINED	825240	89536	825240	1	
W 10	WIRE, PVC, UL1007, 22AWG, BTIN, YEL	115758	04946	22 AWG UL1007	1	
W 11	CORD, LINE, 5-15/IEC, 3-18AWG, SVT, 7.5 FT	284174	70903	17239	1	
NOTES:	‡ Static sensitive part. 1. SEE A3 SECTION 4. 2. SEE A4 SECTION 4.					



1711A/AA T & B
(1 of 6)

Figure 10-1. 1711A/AA Final Assembly



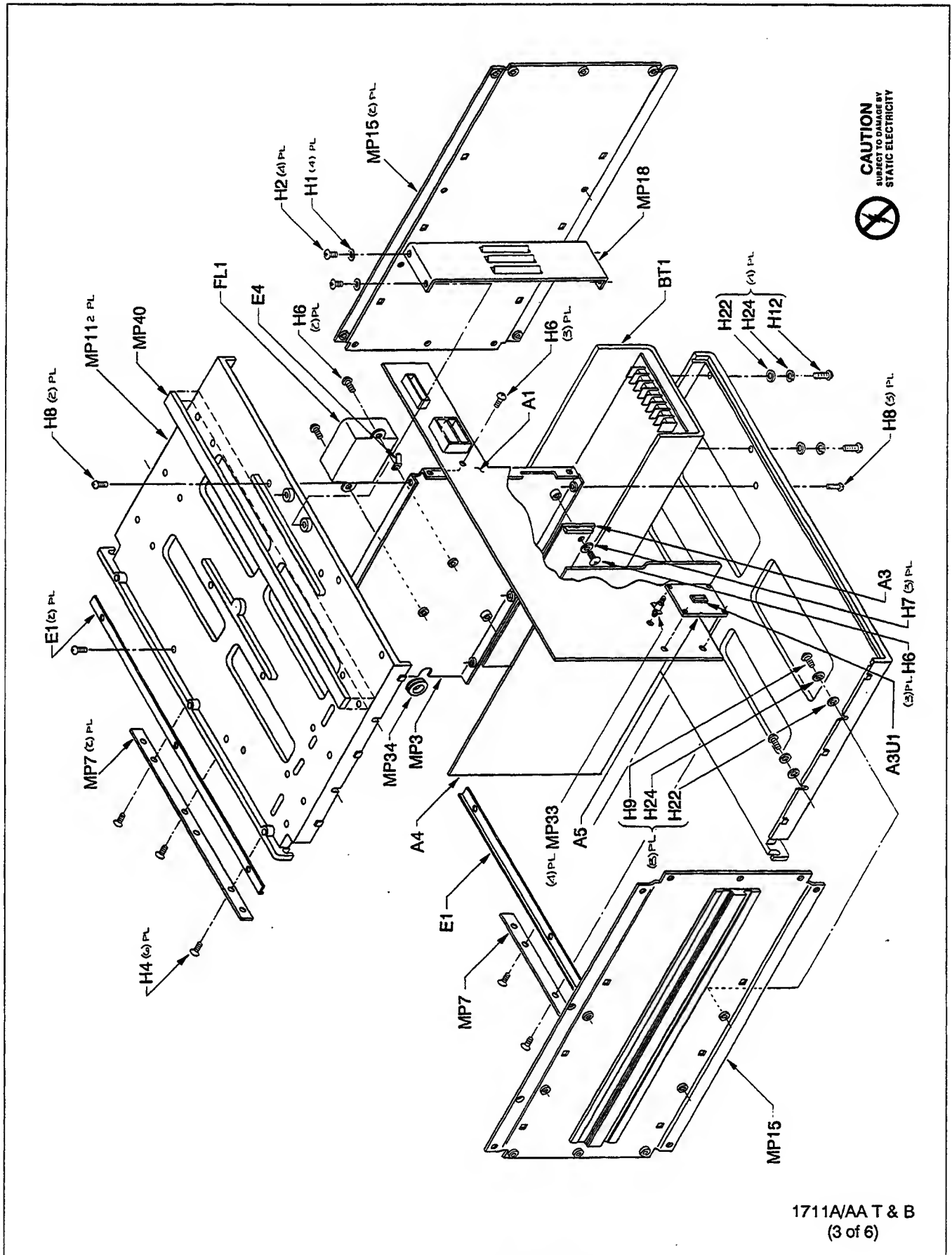
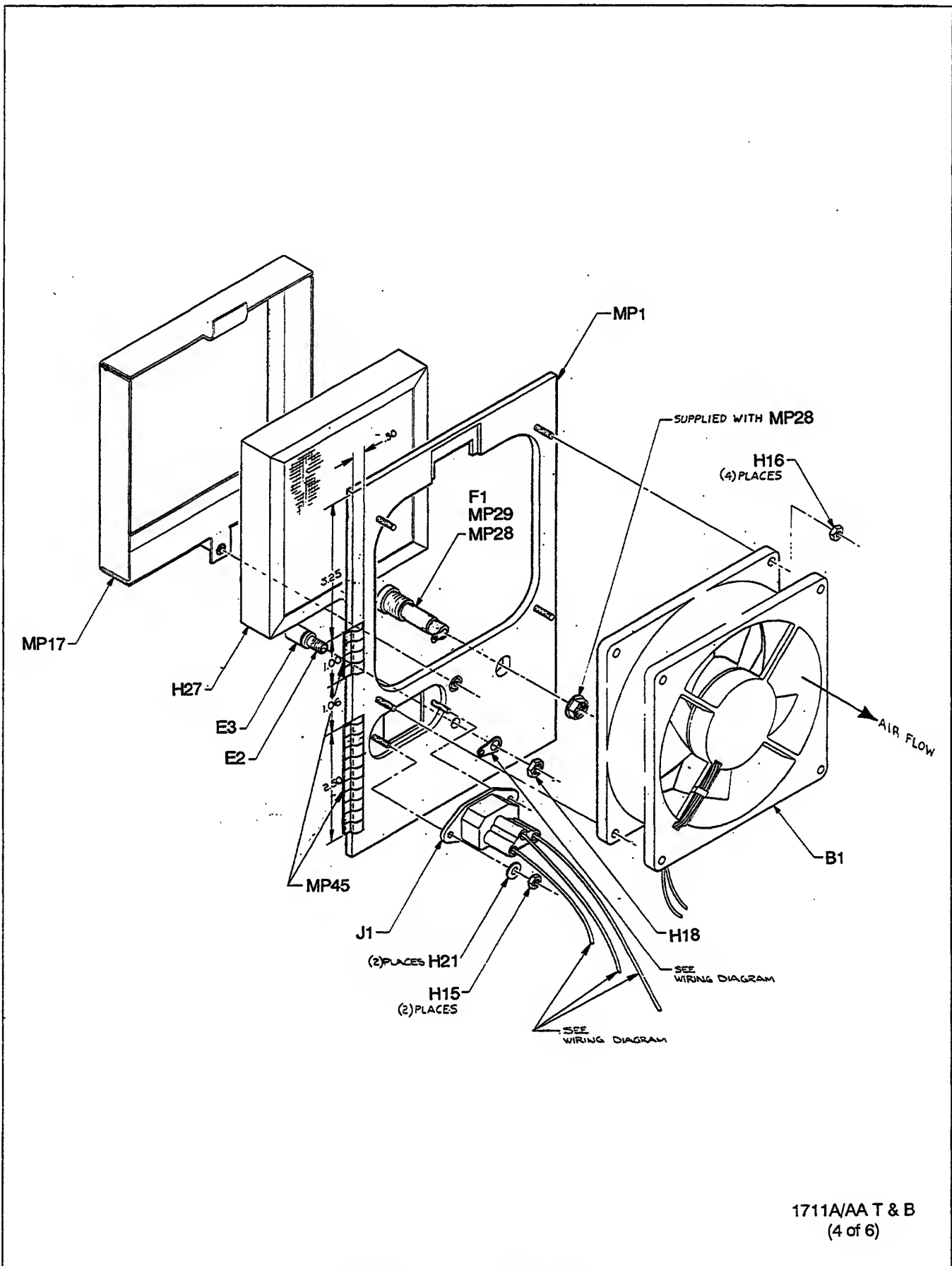


Figure 10-1. 1711A/AA Final Assembly (cont)



1711A/AA T & B
(4 of 6)

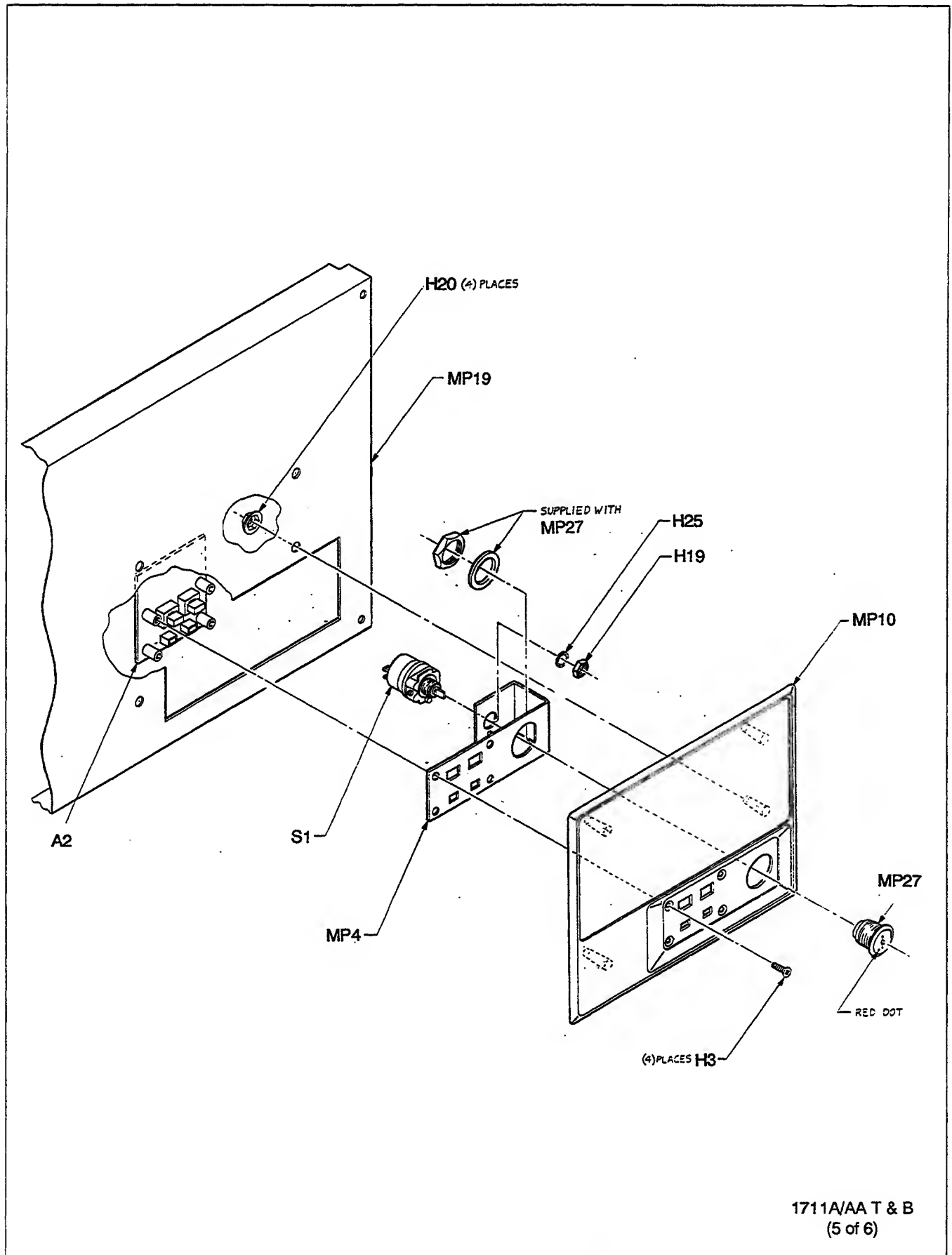


Figure 10-1. 1711A/AA Final Assembly (cont)

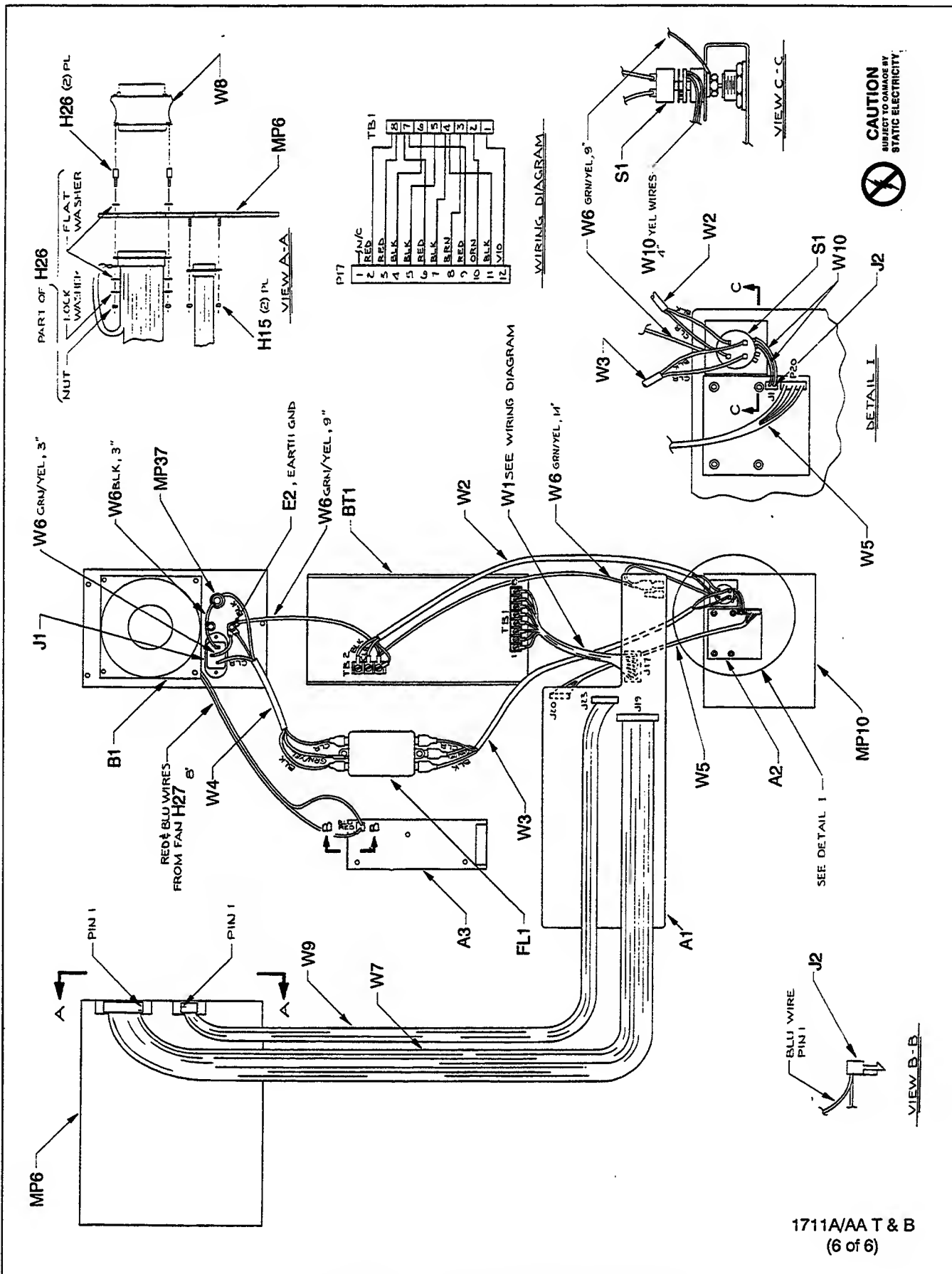
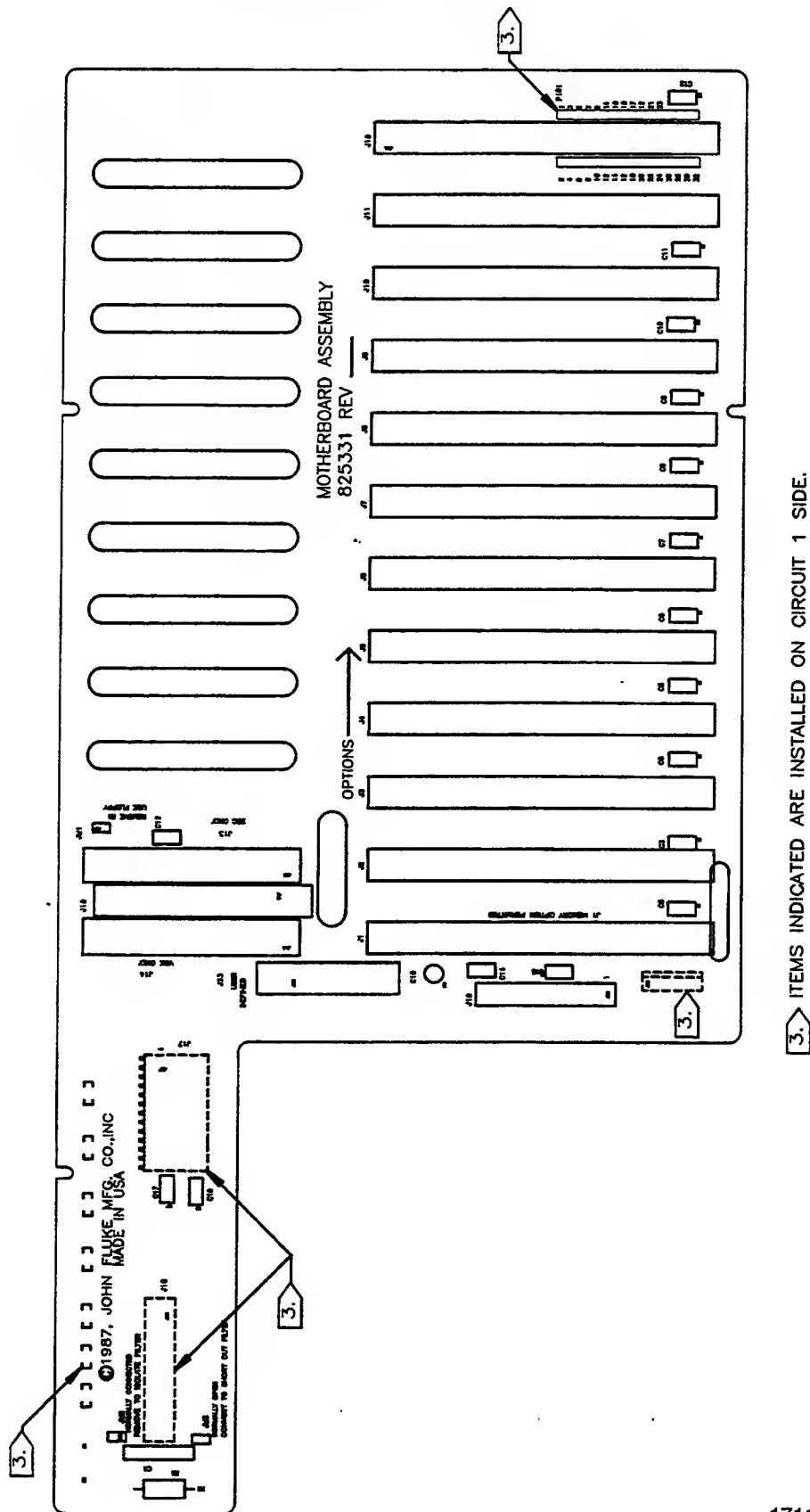


Table 10-2. A2 Motherboard PCA

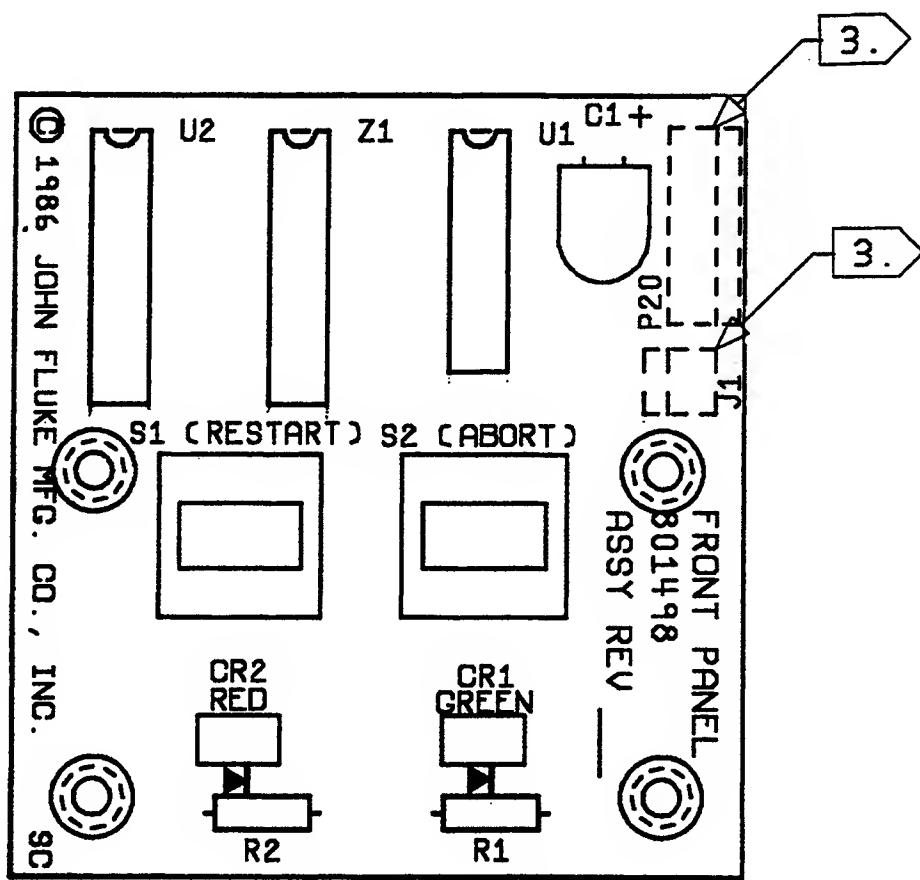
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
C 1	CAP,CER,0.1UF,+80-20%,500V,Z5U	105684	60705	565CZ5UBA501EY104Z	1	
C 2- 17	CAP,CER,1UF,+20%,50V,Z5U	436782	04222	SR305E105MAA	16	
C 18	CAP,TA,150UF,+20%,15V	422576	56289	199D157X0015FA1	1	
E 1, 2	TERM,FASTON,TAB,.250,SOLDER	422790	00779	42822-4	2	
E 4- 10	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	7	
H 1	SCREW,PH,P,LOCK,STL,6-32,.375	152165	73734	19044	2	
H 2	WASHER,FLAT,STL,.149,.375,.031	110270	86928	5202-12-31	2	
H 3	WASHER,LOCK,SPLIT,STL,.141,.266,.031	110692	86928	5850-6-3	2	
H 4	NUT,HEX,STL,6-32	110551		COMMERCIAL	2	
J 1- 12	CONN,PWB EDGE,REC,.100CTR,72 POS	520155	00779	1-530843-9	12	
J 13, 14	CONN,PWB EDGE,REC,.100CTR,44 POS	520148	00779	1-530843-5	2	
J 15	HEADER,1 ROW,.156CTR,10 PIN	376400	27264	26-60-0100	1	
J 17	CONN,MATE-N-LOK,HEADER,12 PIN	706010	00779	350220-1	1	
J 18	HEADER,2 ROW,.100CTR,26 PIN	570846	00779	103308-6	1	
J 19	HEADER,2 ROW,.100CTR,34 PIN	643239	00779	102321-8	1	
J 20	HEADER,1 ROW,.100CTR,6 PIN	631176	00779	640456-6	1	
J 23	HEADER,2 ROW,.100CTR,16 PIN	696906	28213	3408-6322	1	
JM 1- 3	HEADER,1 ROW,.100CTR,2 PIN	643916	00779	103747-2	3	
JM 4- 6	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	757294	00779	850108-1	3	
P 101,102	HEADER,1 ROW,.100CTR,16 PIN	806869	28213	929647-04-16	2	
R 1	RES,CC,1K,+20%,1W	109371	01121	GB1021	1	
NOTES:	† Static sensitive part.					



1711A/AA-1606

Table 10-3. A5 Front Panel PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
C 1	CAP,TA,68UF,+/-20%,6V	519702	56289	199D686X0006DA2	1	
DS 1	LED,GREEN,RECTANGULAR,PCB MOUNT	650879	0MS63	MV54124	1	
DS 2	LED,RED,RECTANGLE,PCB MOUNT	504761	0MS63	MV57124A	1	
J 1	HEADER,1 ROW,.100CTR,2 PIN	602698	00779	640456-2	1	
J 20	HEADER,1 ROW,.100CTR,6 PIN	631176	00779	640456-6	1	
MP 1	SPACER,SWAGE,.250 RND,BR,4-40,.340	380329	55566	3045B-44-B-14-MOD.=.340	4	
MP 2	SPACER L.E.D	541284	89536	541284	2	
MP 3	PUSHBUTTON, SMALL RECT. DK ORANGE	420620	89536	420620	1	
MP 4	PUSHBUTTON, RECT. LIGHT BLUE	406876	89536	406876	1	
R 1, 2	RES,CF,180,+/-5%,0.25W	441436	59124	CF1/4 181J	2	
S 1, 2	SWITCH,PUSHBUTTON,SPNO MOMENTARY	507319	31918	MD DISC	2	
U 1	IC,TTL,QUAD 2 INPUT OR GATE	342709	01295	SN7432N	1	
U 2	IC,ARRAY,7 TRANS,NPN,COMMON EMITTER	407866	56289	ULN2081A	1	
Z 1	RES,CERM,DIP,16 PIN,8 RES,22K,+/-5%	376962	91637	MDP16-03-223J	1	
NOTES:	† Static sensitive part.					

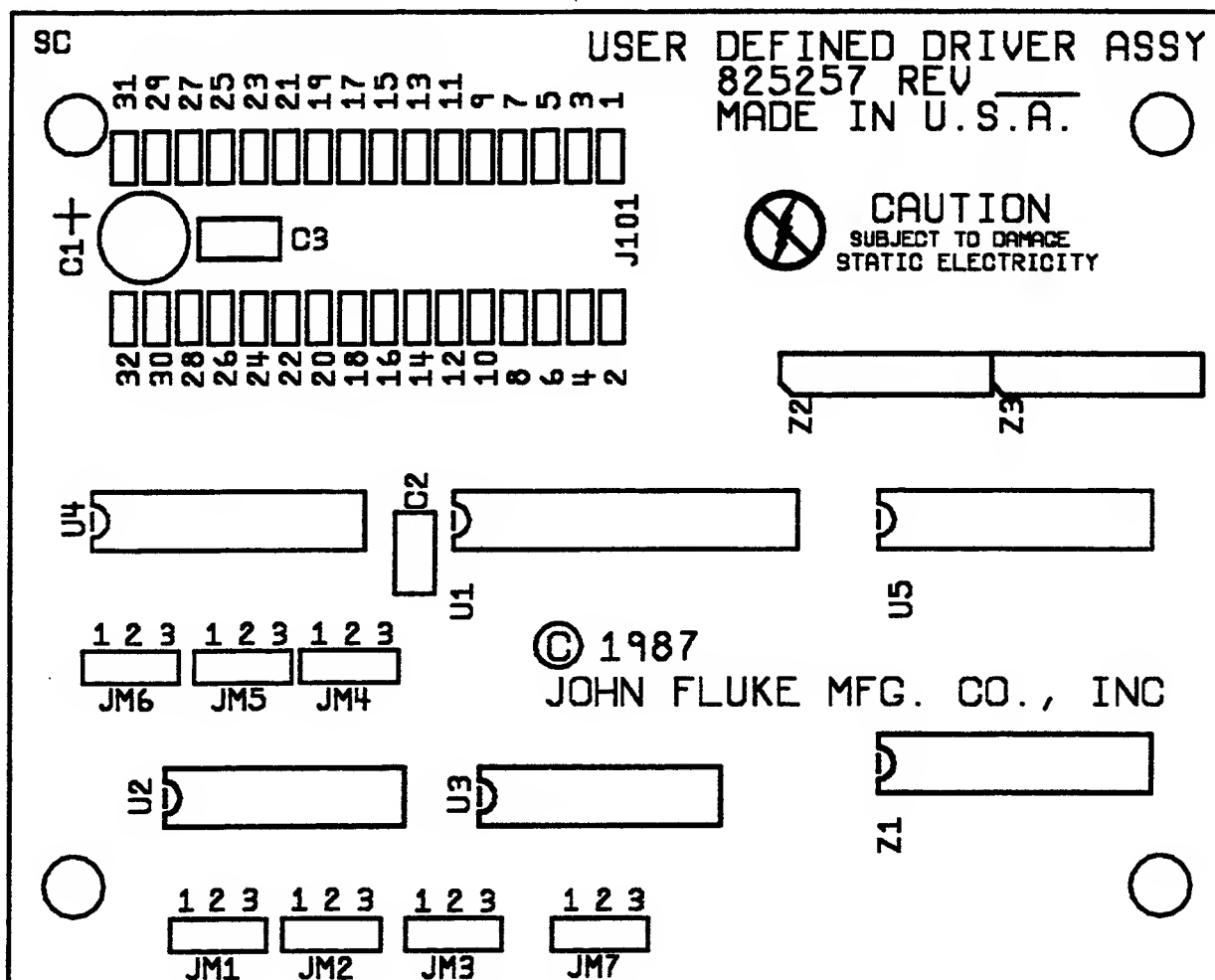


3. PARTS INSTALLED ON CIRCUIT 1 SIDE.

1711A/AA-1602

Table 10-4. A19 User Defined Driver PCA

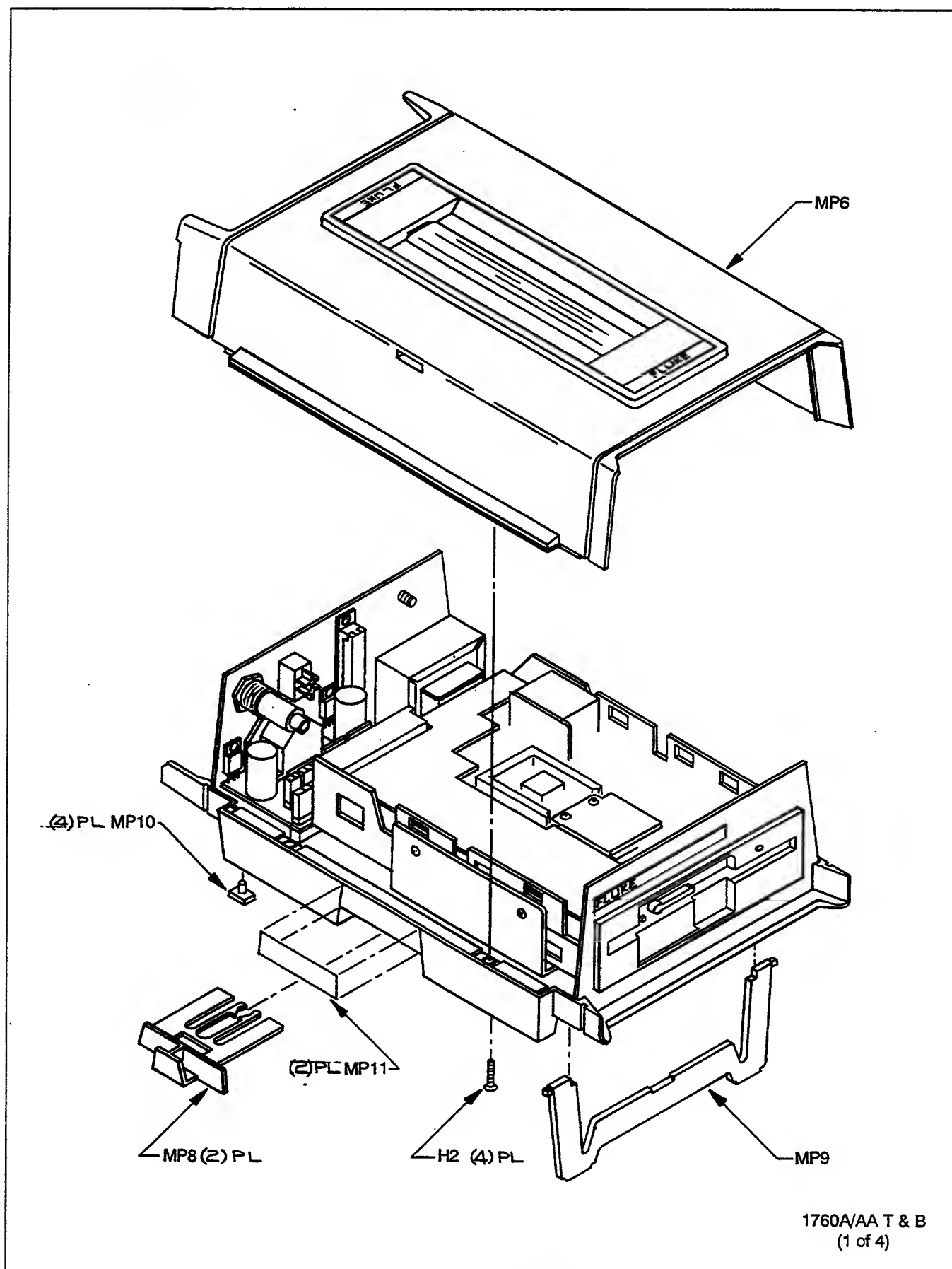
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
C 1	CAP,TA,68UF,+20%,6V	519702	56289	199D686X0006DA2	1	
C 2	CAP,CER,0.22UF,+20%,50V,Z5U	519157	04222	SR205E224MAT	1	
C 3	CAP,CER,330PF,+5%,100V,C0G	528620	04222	SR201A331JAT	1	
J 1- 32	SOCKET,SINGLE,PWB,FOR 0.025 PIN	267476	00779	85861-4	32	
JM 1- 7	HEADER,1 ROW,.100CTR,4 PIN	417329	00779	103747-4	7	
JM 8	JUMPER,REC,2 POS,.100CTR,.025 SQ POST	757294	00779	850108-1	1	
U 1	PROGRAMMED PAL	805036	89536	805036	1	
U 2, 3	† IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	2	
U 4	† IC,LSTTL,8BIT ADDRESSABLE LATCH,W/CLR	419242	01295	SN74LS259N	1	
U 5	† IC,ARRAY,7 TRANS,NPN,COMMON EMITTER	407866	56289	ULN2081A	1	
XU 1	SOCKET,IC,20 PIN	454421	00779	2-640464-1	1	
Z 1	RES,CERM,DIP,16 PIN,8 RES,10K,+5%	500710	91637	MDP16-03-103J	1	
Z 2, 3	RES,CERM,SIP,6 PIN,5 RES,330,+2%	408302	91637	CSC06A-01-331G	2	
NOTES:	† Static sensitive part.					

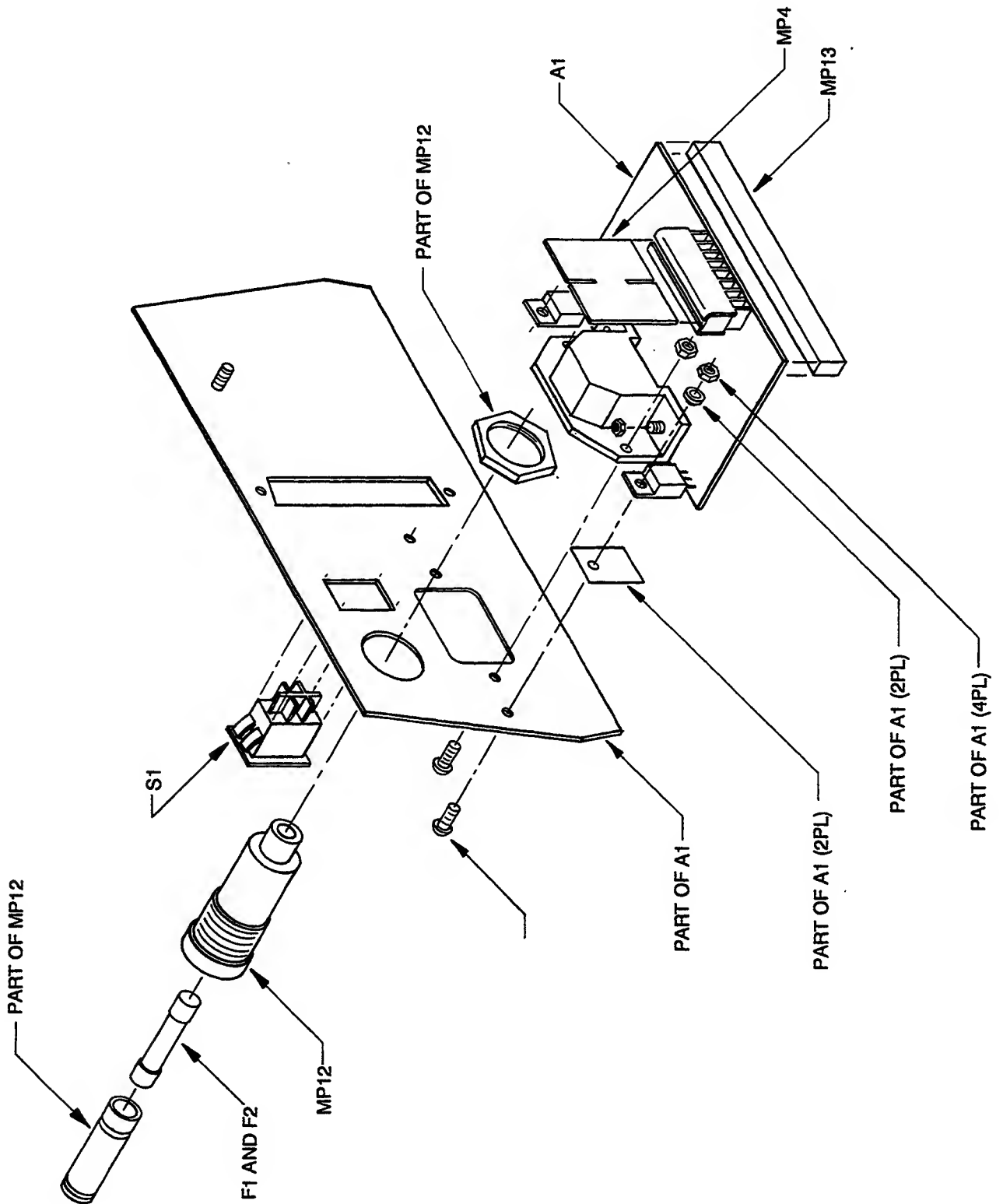


1711A/AA-1605

Table 10-5. 1760A/AA External Floppy Drive

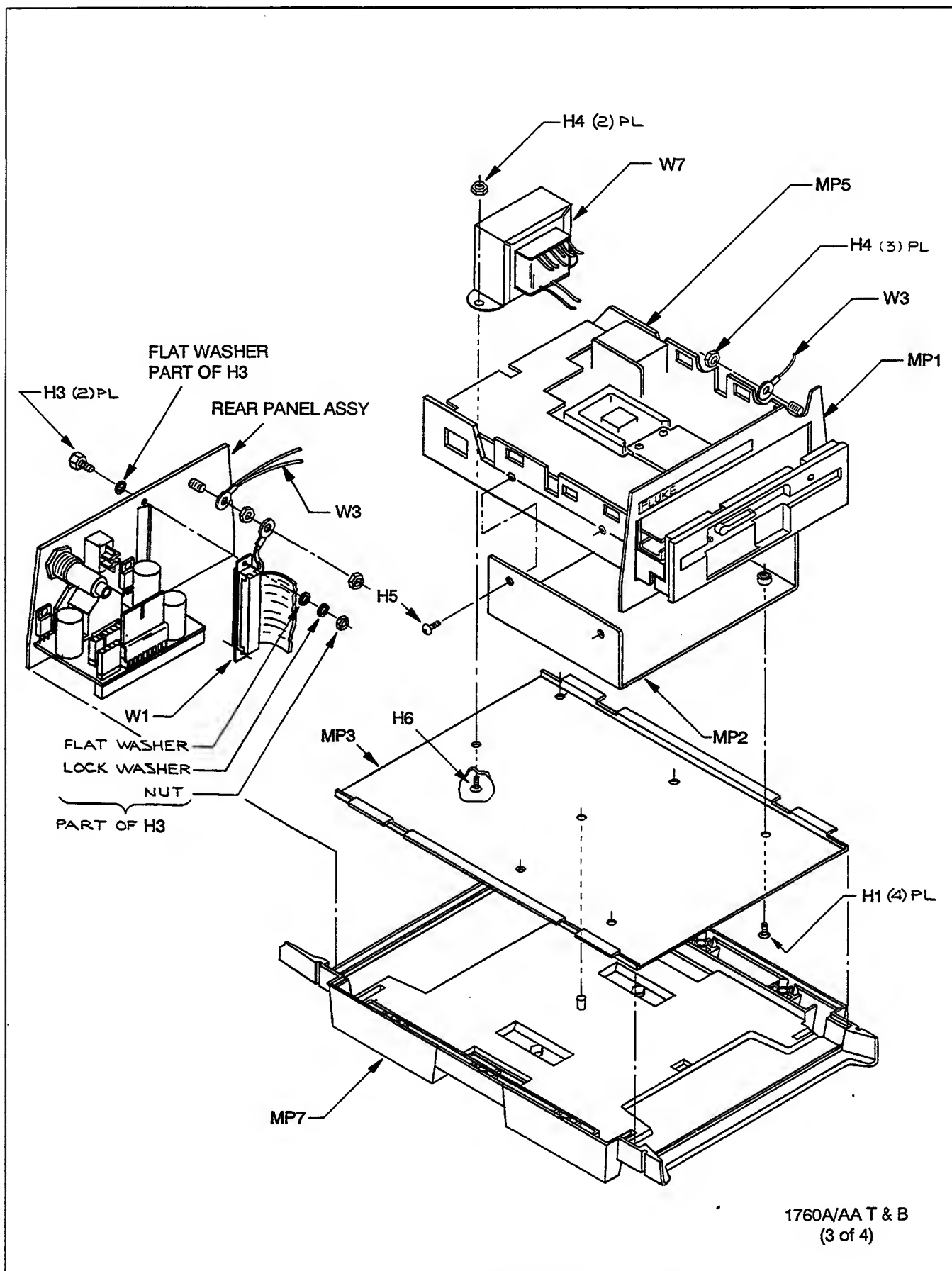
REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
A 1	POWER SUPPLY PCA	919878	89536	919878	1	1
A 9	DISK DRIVE,FLOPPY,5.25IN.,HALF HEIGHT	825356	89536	825356	1	
H 1	SCREW,FHU,P,LOCK,SS,6-32,.250	320093	74594	320093	4	
H 2	SCREW,PH,P,LOCK,STL,6-32,.625	114876	73734	22247	4	
H 4	NUT,EXT LOCK,STL,6-32,.3440D	152819	78189	501-060800-00	3	
H 5	SCREW,FIH,P,STL,M3X10	886973		COMMERCIAL	4	
H 6	SCREW,PH,P,LOCK,STL,6-32,.375	114363	73734	23044	2	
MP 1	FRONT PANEL	824896	89536	824896	1	
MP 2	FLOPPY SUPPORT	824912	89536	824912	1	
MP 3	SHIELD, BOTTOM	824920	89536	824920	1	
MP 7	BASE-STANDARD	454702	89536	454702	1	
MP 8	LATCH	467548	89536	467548	2	
MP 9	BAIL	467555	89536	467555	1	
MP 10	FOOT,NONSKID	467571	89536	467571	4	
MP 11	DECAL,BASE SIDES	473652	22670	473652	2	
MP 12	‡ DISK,SYSTEM	835033	89536	835033	1	
MP 13	‡ DISK,DIAGNOSTIC	826628	89536	826628	1	
W 2	CABLE, DATA, EXTERNAL	824987	89536	824987	1	
W 5	WIRE ASSY, POWER OUTPUT	825315	89536	825315	1	
W 7	TRANSFORMER AND CONNECTOR ASSY.	825273	89536	825273	1	
NOTES:	‡ Static sensitive part. 1. DOCUMENTED IN SECTION 9.					

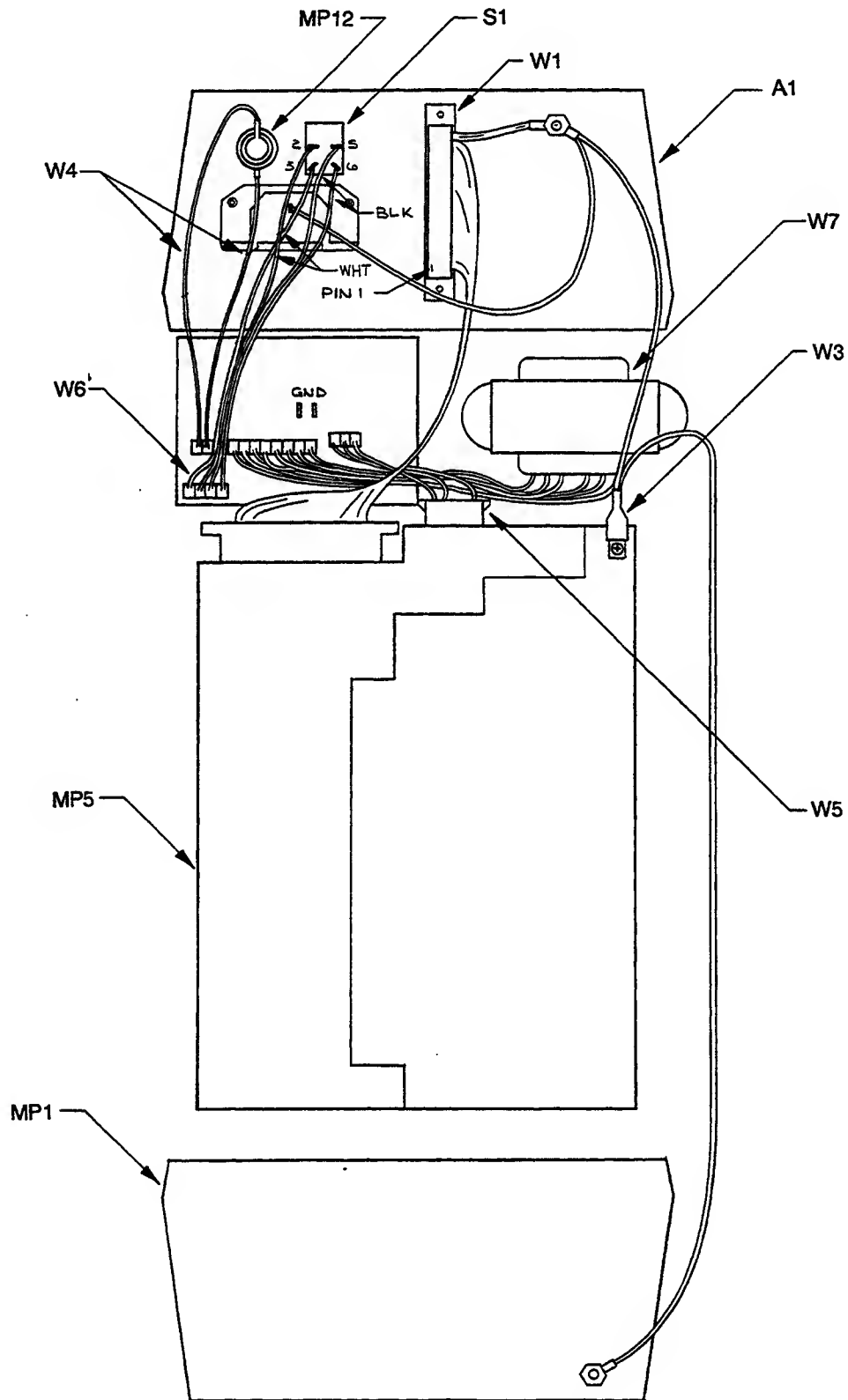




1760A/AA T & B
(2 of 4)

Figure 10-5. 1760A/AA External Floppy Drive (cont)



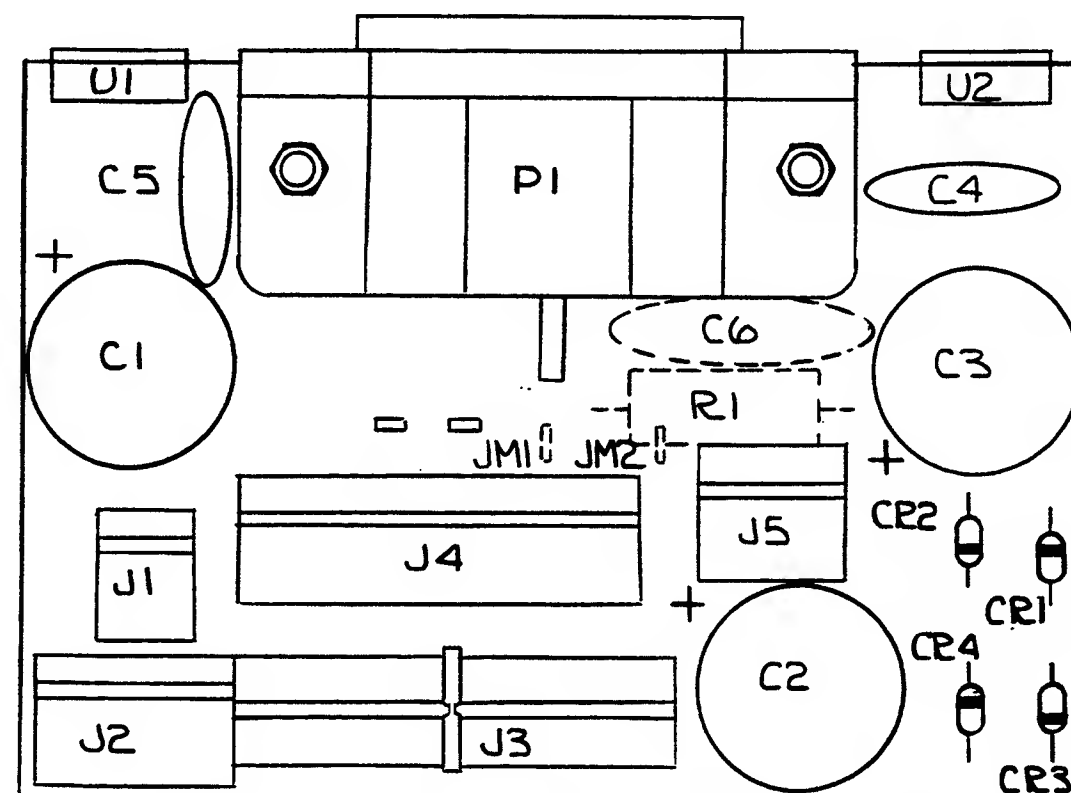


1760A/AA T & B
(4 of 4)

Figure 10-5. 1760A/AA External Floppy Drive (cont)

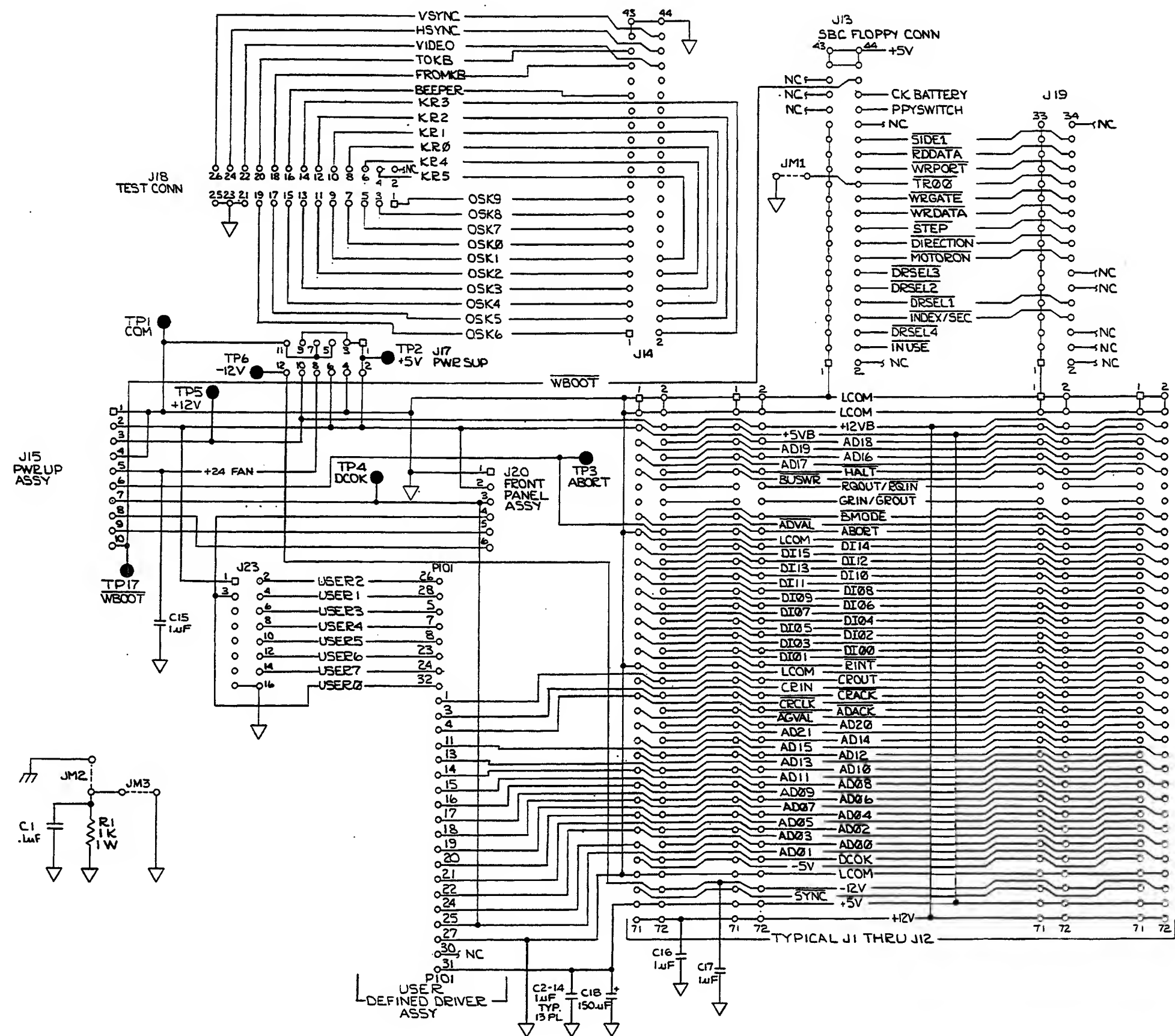
Table 10-6. 1760A/AA A1 Power Supply

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
C 1- 3	CAP,AL,1000UF,+50-20%,35V	641217	62643	SM35VB-1000	3	1
C 4, 5	CAP,CER,5000PF,+/-20%,250V,X7R	485839	4U402	WY12-5000PF/250V 20%-1	2	
CR 1- 4	DIODE,SI,100 PIV,2.5 AMP	495739	12969	UES1102	4	
E 1, 2	TERM,FASTON,TAB,.110,SOLDER	512889	00779	62395-1	2	
F 1	FUSE,.25X1.25,0.375A,250V,SLOW	109264	71400	MDA-3/8	1	
H 1	NUT,HEX,STL,4-40	110635		COMMERCIAL	2	
H 2	NUT,CAP,EXT,LOCK,STL,4-40	195255	78189	501-040800-00	4	
H 3	CONN AC,D-SUB,JACK SCREW,4-40	448092	08718	D-20418-2	2	
H 4	NUT,EXT LOCK,STL,6-32,.3440D	152819	78189	501-060800-88	2	
H 5	WASHER,SHLDR,NYLON,.113,.245	485417	86928	5607-50	2	
H 6	SCREW,PH,P,LOCK,STL,4-40,.375	152124	73734	19024	4	
J 1	HEADER,1 ROW,.156CTR,2 PIN	641647	00779	640388-2	1	
J 2	HEADER,1 ROW,.156CTR,4 PIN	385443	00779	640388-4	1	
J 3	CONN,PWB EDGE,REC,.150CTR,16 POS	408484	00779	583407-9	1	
J 4	HEADER,1 ROW,.156CTR,8 PIN	385435	00779	1-640388-8	1	
J 5	HEADER,1 ROW,.156CTR,3 PIN	380022	00779	640388-3	1	
J 6	CONN ACC,PWB EDGE,POLARIZING INSERT	424572	00779	530286-2	1	
MP 1	REAR PANEL	824904	89536	824904	1	
MP 2	STUD,BROACH,PH HRNZ,4-40,.375	603894	24347	KFH-440-6	2	
MP 3	INSUL PART,POWER,SI,.750,.500	534453	55285	7403-09FR-54	2	
MP 4	PCB, LINE VOLTAGE SELECTOR	824946	89536	824946	1	
MP 12	HLD, FUSE, 1/4 X 1-1/4, LOPROFILE, PNLMT	424416	61935	FEKO31.1631/FEKO31.1613	1	
MP 13	TAPE,FOAM,POLYUR,W/LINER,0.3125X0.250	603134	2K262	4701-01-15-312-1604PSA1	1	
P 1	PWR PLUG,PWB,6A,250V,3 WIRE	461806	82389	EAC-303	1	
S 1	SWITCH,ROCKER,DPST	615054	55224	JWZ2120-0301	1	
U 1	IC,VOLT REG,FIXED,+12 VOLTS,1.5 AMPS	413195	04713	MC7812CT	1	
U 2	IC,VOLT REG,FIXED,+5 VOLTS,1.5 AMPS	355107	04713	MC7805CT	1	
W 1	CABLE, DATA, INTERNAL	824995	89536	824995	1	
W 3	WIRE SET, GROUND	825265	89536	825265	1	
W 4	WIRE ASSY, FUSE HOLDER	825307	89536	825307	1	
W 6	WIRE ASSY, POWER SWITCH	825323	89536	825323	1	
NOTES:	‡ Static sensitive part. 1. FOR 220-240V OPERATION ORDER FLUKE STOCK NUMBER 501098, 3/16A FUSE.					



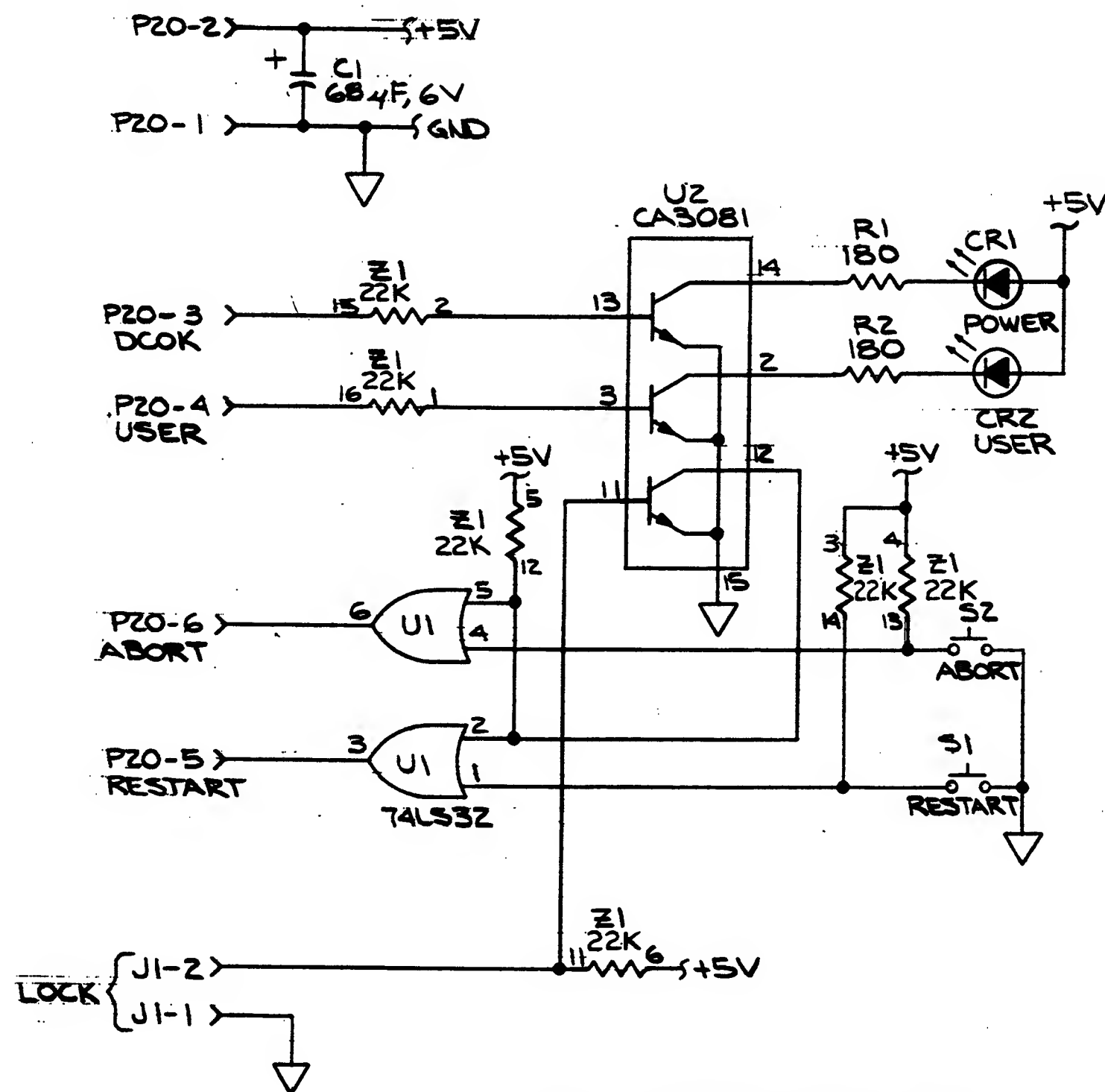
1760A/AA-1601

Figure 10-6. 1760A/AA A1 Power Supply



1711A/AA-1006

Figure 10-7. 1711A/AA A2 Motherboard PCA

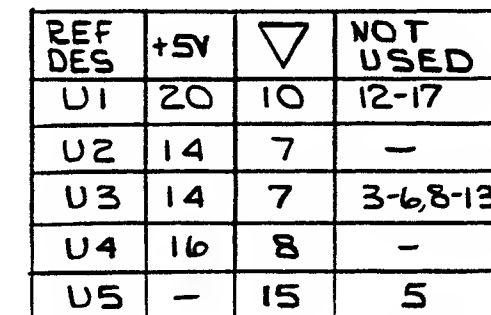


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE IS IN OHMS.
2. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 & Y32.14

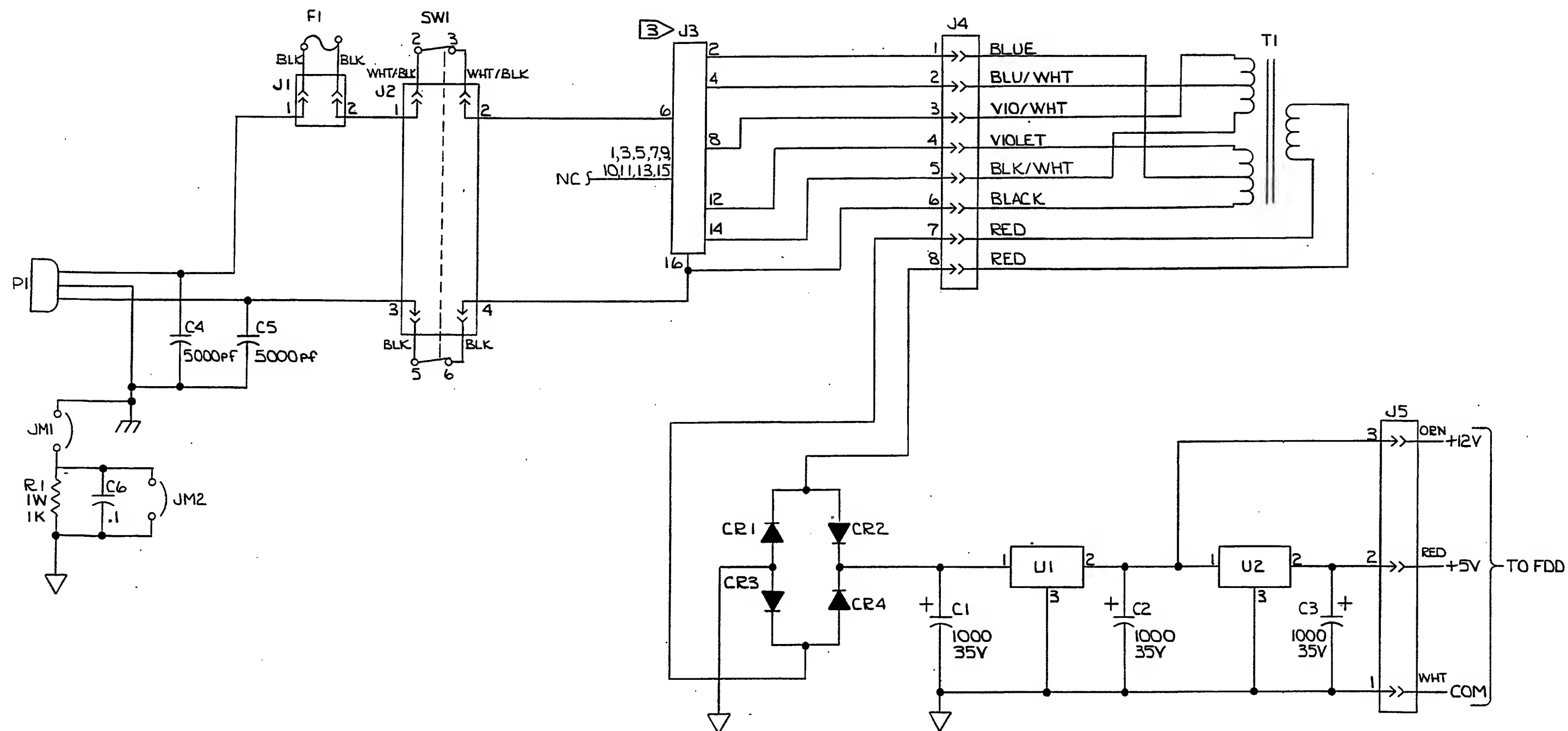
1711A/AA-1002

Figure 10-8. A5 Front Panel Display



1711A/AA-1005

10-28



NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTANCE IN OHMS.
2 ALL CAPACITANCE IN MICROFARADS.

1760A/AA-1001

Figure 10-10. 1760A/AA A1 Power Supply

Section 11

1722A/AP Instrument Controller

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11-1. INTRODUCTION

The 1722A/AP Instrument Controller is a modified version of the Model 1722A Instrument Controller. In addition to the standard 1722A, the 1722A/AP includes a 17XXA-006 256K-Byte Memory Expansion Module and a 17XXA-008 IEEE-488/RS-232 Interface Option. It also has a side carrying handle and front and rear dust covers. The Programmers Keyboard has been replaced by a Handheld Remote Control Unit (RCU). The standard 1722A Boot PROMs and Character PROM have been modified to provide a special boot sequence and character set.

11-2. Port Configuration

The 1722A/AP provides two IEEE-488 Standard ports for instrument control and two RS-232-C ports for serial communication. The IEEE-488 ports are designated PORT 0 and PORT 1 from within an application program when used for instrument control. When used as pseudo-serial devices (output only, for output to an IEEE-488 compatible printer for example), the ports are designated GP0: and GP1:. The RS-232-C ports are designated KB1: and KB2:.

Figure 11-1 shows the rear panel configuration of the 1722A/AP. The connectors for PORT 0 and KB1: are on the Single-Board Computer (SBC) and the connectors for PORT 1 and KB2: are on the IEEE-488/RS-232-C Interface Module.

11-3. Remote Control Unit (RCU)

The RCU takes the place of the Programmers Keyboard and is connected to the front panel keyboard connector. Together, the RCU and the Touch Sensitive Display serve as the operator interface to the 1722A/AP.

The RCU is shown in Figure 11-2. It has three momentary-contact push buttons labeled UP/PASS, DOWN/FAIL, and CONTINUE. The RCU contains a microprocessor and generates a code corresponding to a CTRL-SHIFT key sequence when a push button is pressed. There are also five LEDs labeled UP-DOWN, PASS-FAIL, PASS, FAIL-LO, and FAIL-HI. They may be turned on and off by sending codes from within a user program. Table 11-1 lists the codes generated by the push buttons, and Table 11-2 list the codes required to control the LEDs from a user program. A schematic diagram for the RCU is shown in Figure 11-3.

11-4. THEORY OF OPERATION

The following information describes the theory of operation for the 1722A/AP Handheld Remote Control Unit (RCU). Refer to Section 2 of the 1722A Service Manual for the theory of operation for the rest of the 1722A/AP.

The 1722A/AP RCU uses the Intel 8048 Family Microcomputer to generate character codes in a bit-serial format. The RCU communicates directly with the Video/Graphics/Keyboard interface (VGK). Characters received by the VGK are passed on to the SBC.

11-5. Communication Protocol

Communication between the RCU and VGK uses the bit-serial format used between RS-232-C devices.

The format is as follows:

- One start bit
- Eight data bits
- One stop bit

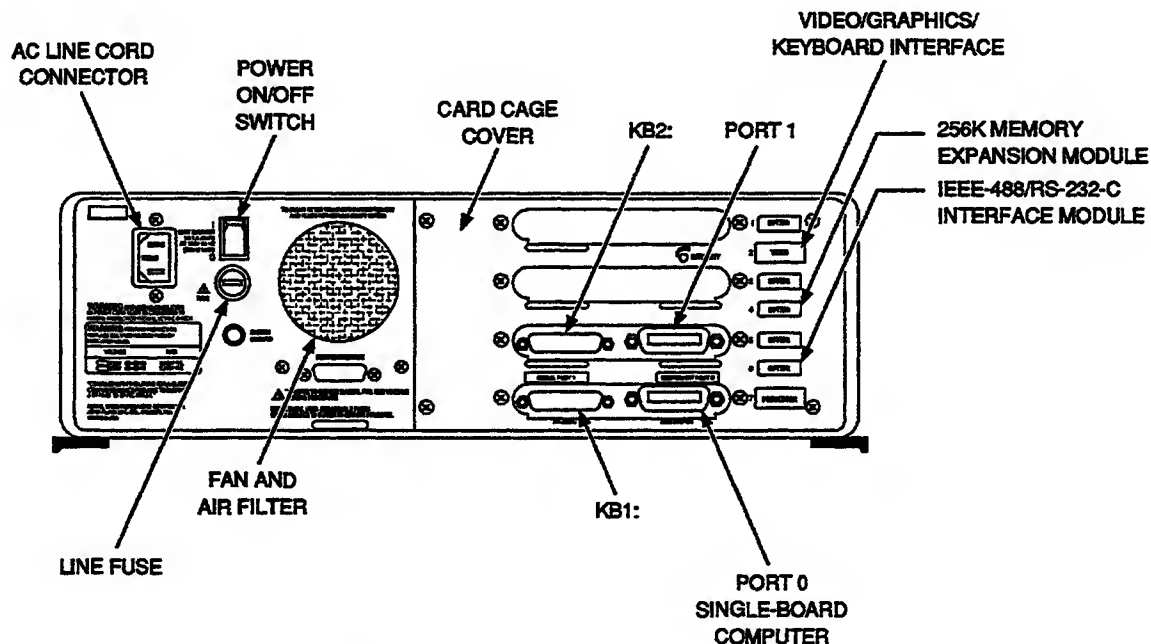


Figure 11-1. The 1722/AP Rear Panel

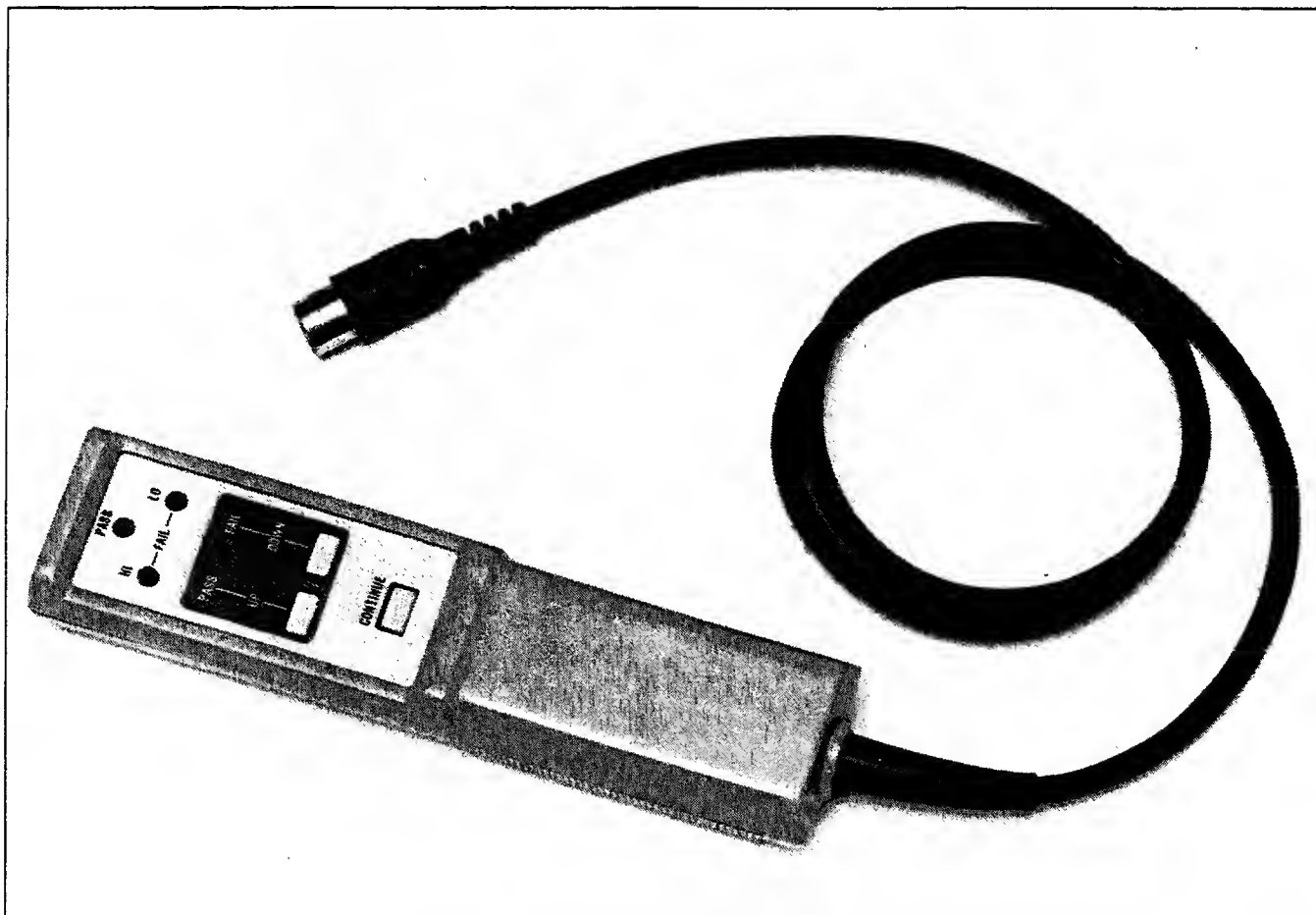


Figure 11-2. Handheld Remote Control Unit

Table 11-1. RCU Push Button Codes

BUTTON	LABEL	CODE
1	UP/PASS	CTRL-SHIFT/2
2	DOWN/FAIL	CTRL-SHIFT/4
3	CONTINUE	CTRL-SHIFT/6

- 1200 baud
- Signal lines = FROM KB and TO KB
- Space = Logic 0 = 0V dc
- Mark = Logic 1 = 5V dc

11-6. Switch Configuration

1722A/AP switch settings are identical to the settings for the 1722A. See Section 2 for correct switch settings. Switch configurations for 1722A options may be found in Section 6.

11-7. Operation

11-8. POWER-UP SEQUENCE

On power-up, and every 175 scans of the keys, the states of the left-shift and control keys are sampled and trans-

mitted to the VGK. For the handheld RCU, these keys are wired closed enabling the VGK to distinguish the RCU from the Programmers Keyboard. A 1-second lamp test is executed on power-up.

11-9. SCANNING

The three push buttons on the RCU are a subset of the key matrix on the Programmers Keyboard. The RCU microcomputer (U1) outputs a column address to the decoder (U2), which selects one side of a push button. A selected push button allows one bit of data to be gated onto the microcomputer data bus. The microcomputer then reads the data bus and forms a key code according to Table 11-1. If one push button is closed for four scans the key code is transmitted to the VGK. If the push button remains pressed for over half a second, the key code is retransmitted once every sixteen scans until it is released.

Table 11-2. RCU LED Codes

LED	LABEL	CODE ON	CODE OFF
All	-	-	ESC[0q
1	UP-DOWN	ESC[1q	ESC[11q
2	PASS-FAIL	ESC[2q	ESC[12q
3	PASS	ESC[3q	ESC[13q
4	FAIL-LO	ESC[4q	ESC[14q
5	FAIL-HI	ESC[5q	ESC[15q

If more than one push button is pressed, no key codes are transmitted until only one push button remains pressed.

11-10. DATA TRANSMISSION

Key code information is transmitted between a software-implemented UART in the RCU microcomputer (U1) and a hardware UART on the VGK. When the VGK UART receives a key code from the RCU, it generates an interrupt, informing the VGK microprocessor that the data is available. Since the RCU firmware does not use interrupts, it must check the TO KB line periodically to see if a BREAK condition (logic 0) exists. If it does, the VGK has a command to send to the RCU. The RCU microcomputer waits for the BREAK to clear and samples the TO KB line for data bits after detecting a start bit. The RCU microcomputer will continue scanning if the BREAK has not cleared within a prespecified time.

11-11. LED CONTROL

The LEDs are driven by a latch (U3) and controlled by special codes sent by the VGK. The codes turn the LEDs on or off as specified in Table 11-2.

11-12. MAINTENANCE

The following information describes troubleshooting for the 1722A/AP Handheld Remote Control Unit (RCU). Refer to Section 3 of the 1722A Service Manual for system diagnostics and additional maintenance information.

11-13. Remote Control Unit Fault Analysis

SYMPTOM:

LEDs on the RCU do not light on power-up.

POSSIBLE CAUSES:

- No power to RCU circuitry
 - Bad connection in cabling between Motherboard and RCU
- Microcomputer (U2).
 - Bad crystal.
 - Bad level on Reset pin.

- U3 is nonfunctional.

SYMPTOM:

Some push buttons work and others do not.

POSSIBLE CAUSES:

- Dirty switch contacts.
- Output driver in U1 is bad.

SYMPTOM:

The RCU LEDs come on, but no keys on the RCU work.

POSSIBLE CAUSES:

- Two or more key contacts are stuck closed.
- An output of the decoder (U2) or data bus line DB6 is shorted high or low.

11-14. LIST OF REPLACEABLE PARTS

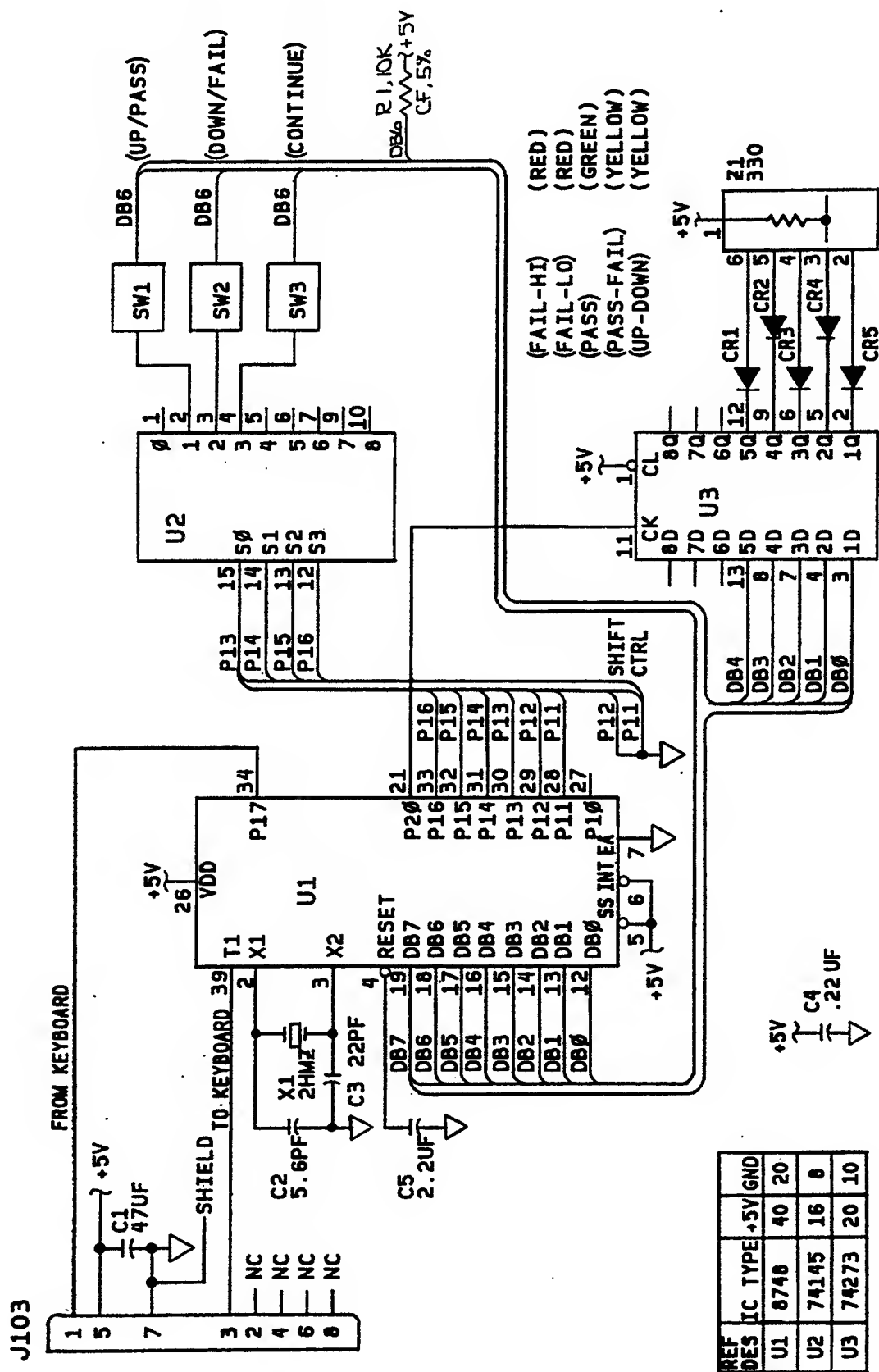
This section provides information to adapt the 1722A parts list to the 1722A/AP.

11-15. Module Revision Information

Assembly revision levels are documented in the "Manual Status Information" table later in this section. To identify the configuration of the pca's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pca.

11-16. NEWER INSTRUMENTS

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.



Manual Status Information

REF	ASSEMBLY NAME	FLUKE P/N	REVISION LEVEL
A1	Video/Graphics/Keyboard (VGK) Interface Module	744284 897488	M
A2	Motherboard PCA	699066	J
A3	Power-Up (PUP) PCA	704353	B
A4	Single-Board Computer (SBC) Module (1722A)	744318	N
A5	Front Panel Assembly	704296	E
A7	Keyboard Filter	849252	
006	256K RAM Expansion Module	718684	F
008	IEEE-488/RS-232-C Interface Module	718221	F

Table 11-3. 1722A/AP Alignment Kit

DESCRIPTION	FLUKE PART NUMBER
1722A-7603K Kit Power-Up Assembly (PUP)	704353
1722A-7620 Kit Power Supply	718064
1722A-7636K Kit, 17XXA Floppy Disk Drive	825356
1722A-7604 Kit, Single-Board Computer Replacement	744318
1722A-7601 Kit Video/Graphics/Keyboard Interface	744284
1722A-7625K CRT and Video Electronics	884697
1780A-4206 Touch-Sensitive Overlay	705301
Cable, Assy, Nul Mod, 9 Cond, Shlded, 1ft	909932
Cable, Assy, IEEE-488, 24 Cond, Shlded, 1m	658526
1720A-4011 PCA Extender, 172XA	496745
1722A-7608-1K Kit, 256K byte RAM Expansion Assy	718684
1722A-7609K Kit, IEEE-488/RS-232 Interface Option	718221
1722-4015T Remote Control Unit (RCU)	732198
System Diagnostic Disk	718080
Anti-Static Field Work Station	583211
1722A Service Manual	909932
Alignment Tool	572321
Alignment Gauge	535864
IC Extraction Tool	572339
Air Filter	605899

Table 11-4. Replacement PROMs and PALs

ASSEMBLY	REV	DESCRIPTION	REF DES	VER	JF/PN
Single Board Computer	All	EPROM odd boot	U68	1.0	736942
	All	EPROM even boot	U81	1.0	736959
	All	PAL, AGGIE bus	U20	1.0	712711
	All	PAL, AGGIE state	U22	1.0	712729
	All	PAL, DRAM	U33	1.0	712737
	All	PAL, exception	U18	1.0	712745
	D-F	PAL, floppy	U14	1.0	712752
	G-H		U14	1.1	736975
	All	PAL, postmap	U50	1.0	712760
	All	PAL, premap	U34	1.0	712778
	D	PAL, ras	U66	1.0	712786
	E-F		U66	1.1	718825
	G-H		U66	1.2	737031
	All	PAL, register control	U29	1.0	712794
	D-F	PAL, waitgen	U31	1.0	712802
	G-H		U31	1.1	736983
Video/ Graphics/ Keyboard (VGK)	All	EPROM, character	U32	1.0	712615
	All	EPROM, firmware	U29	1.2	712615
	All	PAL, argus	U11	1.0	712646
	All	PAL, Address	U18	1.0	712653
	All	PAL, double size	U40	1.0	712661
	All	PAL, clock	U22	1.0	712679
	All	PAL, attribute	U54	1.1	712687
256K Memory Expansion Module	All	PAL, translation	U86	1.0	716480
	All	PAL, status decode	U92	1.0	716498
	All	PAL, error	U75	1.0	716506
	All	PAL, refresh control	U82	1.0	716514
IEEE-488/ RS-232-C	All	PAL, address	U3	1.0	711622
	All	PAL, logic	U4	1.0	711630

Table 11-5. 1722A/AP Final Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	VIDEO/GRAPHICS/KEYBOARD (VGK) IF PCA		89536		1	1
A 2	MOTHERBOARD PCA	699066	89536	699066	1	2
A 3	POWER-UP (PUP) PCA	704353	89536	704353	1	3
A 4	SINGLE BOARD COMPUTER (SBC) PCA		89536		1	4
A 5	FRONT PANEL PCA	704296	89536	704296	1	5
A 7	TOUCH PANEL ASSEMBLY	705301	89536	705301	1	6
A 8	VIDEO MON., 5X9IN., MONOCHROME, KIT	884697	0CXF1	884697	1	7
A 9	DISK DRIVE, FLOPPY, 5.25IN., HALF HEIGHT	825356	89536	825356	1	7
A 10	PWR SUP, 200W, 5V@30A, -12V@4A, +12V@8/4A	718064	89536	718064	1	7
A 14	KEYBOARD FILTER PCA	849252	89536	849252	1	8
A 15	ASSY, INSTRUMENT COVERS (FRONT & BACK)	760454	89536	760454	1	
A 16	HANDHELD ASSEMBLY	717371	89536	717371	1	
A 17	256K MEMORY EXPANSION PCA	718684	89536	718684	1	9
A 18	IEEE/RS-232-C INTERFACE PCA	718221	89536	718221	1	10
B 1	FAN, 12VDC, 34CFM, 3.15" SQ	776278	89536	776278	1	
E 1	TERM, FASTON, REC., .187, 18-22 AWG, INSUL	747485	06383	DNF18-187	1	
E 2	BINDING POST, METAL, PLATED	225623	89536	225623	1	
E 3	BINDING POST HEAD, PLATED	225615	89536	225615	1	
E 4	TERM, RING 1/4 & 1/32, SOLDR	102566	79963	813	1	
F 1	FUSE, .25X1.25, 3A, 250V, FAST	109199	71400	AGC-3	1	
FL 1	FILTER, LINE, 115V/3A, 250V/1.5A, W/CONN	706697	23880	STE8-3	1	
H 1	AIR FILTER	605899	25099	605899	1	
H 2	WASHER, FLAT, SS, .125, .317, .030	146225		COMMERCIAL	3	
H 3	WASHER, LOCK, SPLIT, STL, .115, .223, .025	110395	86928	5850-4-3	2	
H 4	WASHER, LOCK, SPLIT, STL, .168, .307, .040	111070	86928	5850-8-3	4	
H 5	WASHER, FLAT, STL, .149, .375, .031	110270		COMMERCIAL	9	
H 6	SCREW, PH, P, SEMS, STL, 6-32, .313	530287		COMMERCIAL	6	
H 7	SCREW, PH, P, LOCK, STL, 4-40, .375	152124	73734	19024	2	
H 8	SCREW, FHU, P, LOCK, SS, 6-32, .250	320093	74594	320093	28	
H 9	SCREW, PH, P, SEMS, STL, 6-32, .250	178533		COMMERCIAL	11	
H 10	SCREW, PH, P, SEMS, STL, 6-32, .375	177022		COMMERCIAL	22	
H 11	SCREW, PH, P, SEMS, STL, 6-32, .500	177030		COMMERCIAL	9	
H 12	SCREW, CAP, SCKT, SS, 8-32, .375	295105	74445	295105	4	
H 13	SCREW, PH, P, LOCK, STL, 8-32, .375	114116	89536	114116	10	
H 14	SCREW, PH, P, SEMS, STL, 8-32, .375	436030		COMMERCIAL	8	
H 15	SCREW, PH, P, THD CUT, SS, 4-24, .375	183574		COMMERCIAL	5	
H 16	NUT, HEX, BR, 1/4-28	110619		COMMERCIAL	2	
H 17	SCREW, PH, P, STL, M3X6	854034		COMMERCIAL	6	
H 19	WASHER, FLAT, BRASS, #6, 0.028 THK	111310		COMMERCIAL	4	
H 20	SCREW, PH, P, SEMS, STL, 6-32, .750	309963		COMMERCIAL	4	
H 21	SCREW, PH, P, LOCK, STL, 8-32, .250	228890	73734	19062	2	
H 22	SCREW, PH, P, LOCK, SS, 4-40, .312	335141	74594	335141	3	
H 23	SCREW, PH, P, LOCK, STL, 8-32, .625	114983	73734	19067	2	
H 24	WASHER, FLAT, MYLAR, .165, .285, .010	197426	86928	5622-68-10	3	
J 1	SOCKET, 1 ROW, 0.100 CTR, 2 POS	602706	00779	640442-2	1	
MP 1	RIGHT SIDE CHASSIS	749374	89536	749374	1	
MP 2	LEFT SIDE CHASSIS	749382	89536	749382	1	
MP 3	BRACKET, POWER SUPPLY	749275	89536	749275	1	
MP 4	COVER, POWER SUPPLY	749366	89536	749366	1	
MP 5	PLATE, REMOTE OPTION	762559	89536	762559	1	
MP 6	COVER CRT ELECTRONICS	884692	89536	884692	1	
MP 7	FLOPPY SUPPORT	759118	89536	759118	1	
MP 8	CARD CAGE	749390	89536	749390	1	
MP 9	FLOPPY DIVIDER (B)	749283	89536	749283	1	
MP 10	REAR PANEL	749341	89536	749341	1	
MP 11	CORNER, FRONT, MED PEWTER	630723	89536	630723	2	
MP 12	CORNER, REAR	630764	89536	630764	2	
MP 13	BRACKET, FAN	760470	89536	760470	1	
MP 14	COVER, FILLER PANEL	897538	89536	897538	1	
MP 16	PLAS PART, HOLE PLUG, NYL, DOME, BLK, .250	854299	28520	2603	1	
MP 17	CRT ALIGNMENT INSERT	711325	89536	711325	4	
MP 18	DECAL, FRONT PANEL	849195	89536	849195	1	
MP 20	HLDR, FUSE, 1/4 X 1-1/4, LOPROFILE, PNLMT	424416	61935	FEC031.1631/FEK031.1613	1	
MP 21	BEZEL, HALF HEIGHT, PAINTED DK UMBER	824847	89536	824847	1	
MP 22	TOUCH PANEL FRONT GASKET	604272	2K262	604272	1	
MP 23	CARD GUIDE	749358	89536	749358	6	
MP 24	CABLE ACCESS, TIE, 4.00L, .10W, .75 DIA	172080	06383	SST-1M	6	
MP 25	CABLE TIE ANCHOR, ADHSV, .160TIE	407908	06383	ABMM-A-C	2	
MP 26	DECAL, IMPLSION PROTECTION	577387	89536	577387	2	
MP 27	FOOT, RUBBER, ADHES, BLK, .50 DIA, .14 THK	513820	28213	SJ-5012	2	
MP 28	LABEL, ADHESIVE, IC, HIGH TEMPERATURE	720904	85480	DAT-1-637-10	25	
MP 29	COVER, REAR CARD CAGE W/O VIDEO ACCESS	897512	89536	897512	1	
MP 30	PLATE, BLANK	777250	89536	777250	2	
MP 31	COVER, TOP	754663	89536	754663	1	
MP 32	COVER, BOTTOM	754671	89536	754671	1	

Table 11-5. 1722A/AP Final Assembly (cont)

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
MP 33	SIDE EXTRUSION	859947	89536	859947	2	
MP 34	INSERT EXTRUSION	859942	89536	859942	1	
MP 35	4 BAIL, INSTRUMENT	707877	95080	707877	2	
MP 36	FOOT, SINGLE BAIL TYPE (DARK UMBER)	653923	89536	653923	4	
MP 37	DECAL, TITLE	744409	22670	744409	1	
MP 38	DECAL, FRONT CORNER 5 1/4, MED PEWTER	685289	22670	685289	2	
MP 39	DECAL, REAR CORNER 5 1/4, MED PEWTER	685297	22670	685297	2	
MP 40	DECAL, TRIM	707810	22670	707810	2	
MP 41	GROUND STRIP, BECU, SPRING FINGER	370619	34641	97-500-01	9	
MP 42	SHIPPING DISKETTE	707984	89536	707984	1	
MP 43	4 1722A/AP DISK SET	897504	89536	897504	1	
MP 45	MAGNET, FERRITE, 4 GAUSS	876032	OCXF1	130102-004	2	
MP 47	DECAL CSA	525527	22670	525527	1	
MP 48	FOAM, BOARD RETENTION	897525	89536	897525	2	
MP 53	HANDLE EXTRUSION, MODIFIED	699009	89536	699009	1	
MP 54	HANDLE RETAINER	579052	89536	579052	2	
MP 55	BRACKET, HANDLE SUPPORT	632414	89536	632414	2	
MP 56	CATCH, LATCH, LEVER/SPRING, SS, W/KEEPER	740332	94222	97-50-134-11	2	
MP 57	GROMMET, SLOT, RUBBER, .875, .062	380782	2K262	380782	4	
MP 58	GASKET, NEOPRENE, SELF-ADHES, 3/16X1/2	740373	2K262	B42N	4	
MP 59	STRAP, HANDLE	698993	89536	698993	1	
MP 60	DECAL, SERIAL PORT	707554	22670	707554	1	
MP 61	DECAL, INSTRUMENT PORT	707562	22670	707562	1	
MP 62	DECAL, INSTRUMENT/SERIAL I/O	707604	22670	707604	1	
MP 63	DECAL, 256K MEMORY	707570	22670	707570	1	
MP 64	TAPE, FRICTION LOCK, 400 STEMS/SQ. IN.	641290	89536	641290	8	
MP 65	TAPE, FRICTION LOCK, 170 STEMS/SQ. IN.	641308	89536	641308	8	
MP 66	COVER, INNER	759209	89536	759209	2	
MP 67	GROMMET, SLOT, RUBBER, .875, .062	380782	2K262	380782	4	
P 1	MOUNTING STRAP, CRT (WIRE)	650630	89536	650630	1	
S 1	SWITCH, ROCKER, DPST	615054	55224	JWZ2120-0301	1	
TM 2	1722A/1752A SERVICE MANUAL	909932	89536	909932	2	
TM 4	1722A OPERATORS QUICK REFERENCE CARD	718163	89536	718163	1	
W 1	SUPPORT BRACKET CRT MTG (WIRE)	650515	89536	650515	1	
W 2	CABLE, POWER	644120	89536	644120	1	
W 3	CABLE, POWER SUPPLY	705343	89536	705343	1	
W 4	CABLE, VIDEO POWER SIGNAL	712836	89536	712836	1	
W 5	1722A, CABLE, CRT GROUND	843201	89536	843201	1	
W 6	CABLE, FUSE	762500	89536	762500	1	
W 7	CABLE, CHASSIS GROUND	762518	89536	762518	1	
W 8	CABLE, SLACK POWER SWITCH	762542	89536	762542	1	
W 9	CABLE, WHITE POWER SWITCH	762526	89536	762526	1	
W 10	CORD, LINE, 5-15/IEC, 3-18AWG, SVT, 7.5 FT	284174	70903	17239	1	
W 11	CABLE ASSY, IEEE488, 24 COND, SHLDED, 2M	682401	00779	553577-3	1	
NOTES:	4 Static sensitive part. 1. SEE A1 SECTION 4. 2. SEE A2 SECTION 4. 3. SEE A3 SECTION 4. 4. SEE A4 SECTION 4. 5. SEE A5 SECTION 4. 6. NO PARTS BREAKDOWN FOR THIS ASSEMBLY. 7. SEE SECTION 9. 8. SEE A14 SECTION 4. 9. SEE OPTION -006 SECTION 4. 10. SEE OPTION -008 SECTION 4.					

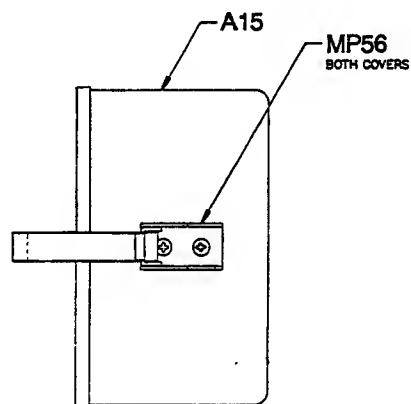
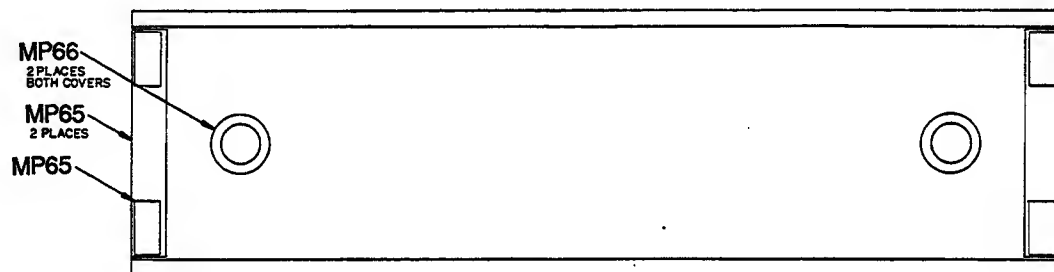
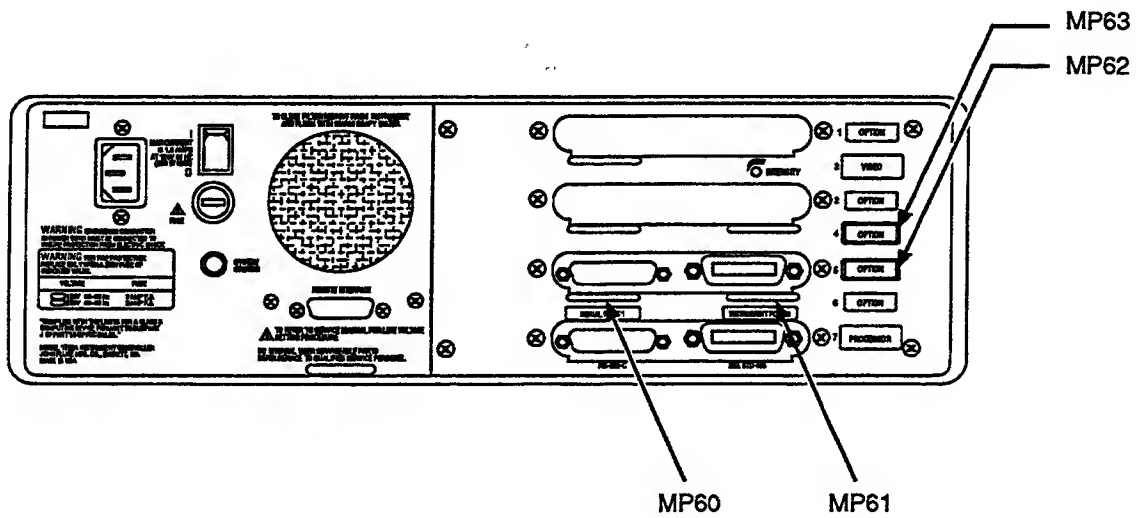


Figure 11-4. 1722A/AP Final Assembly

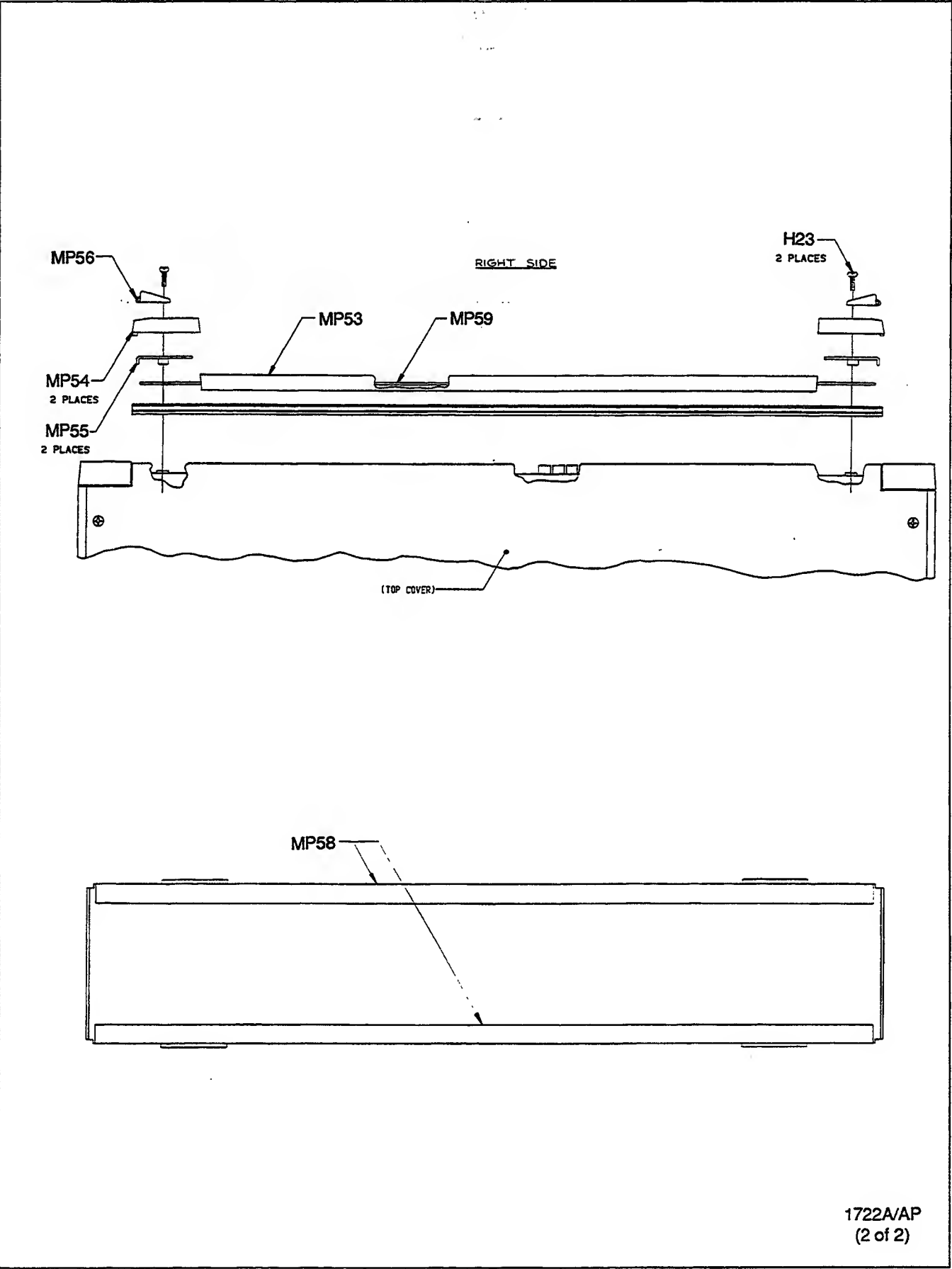
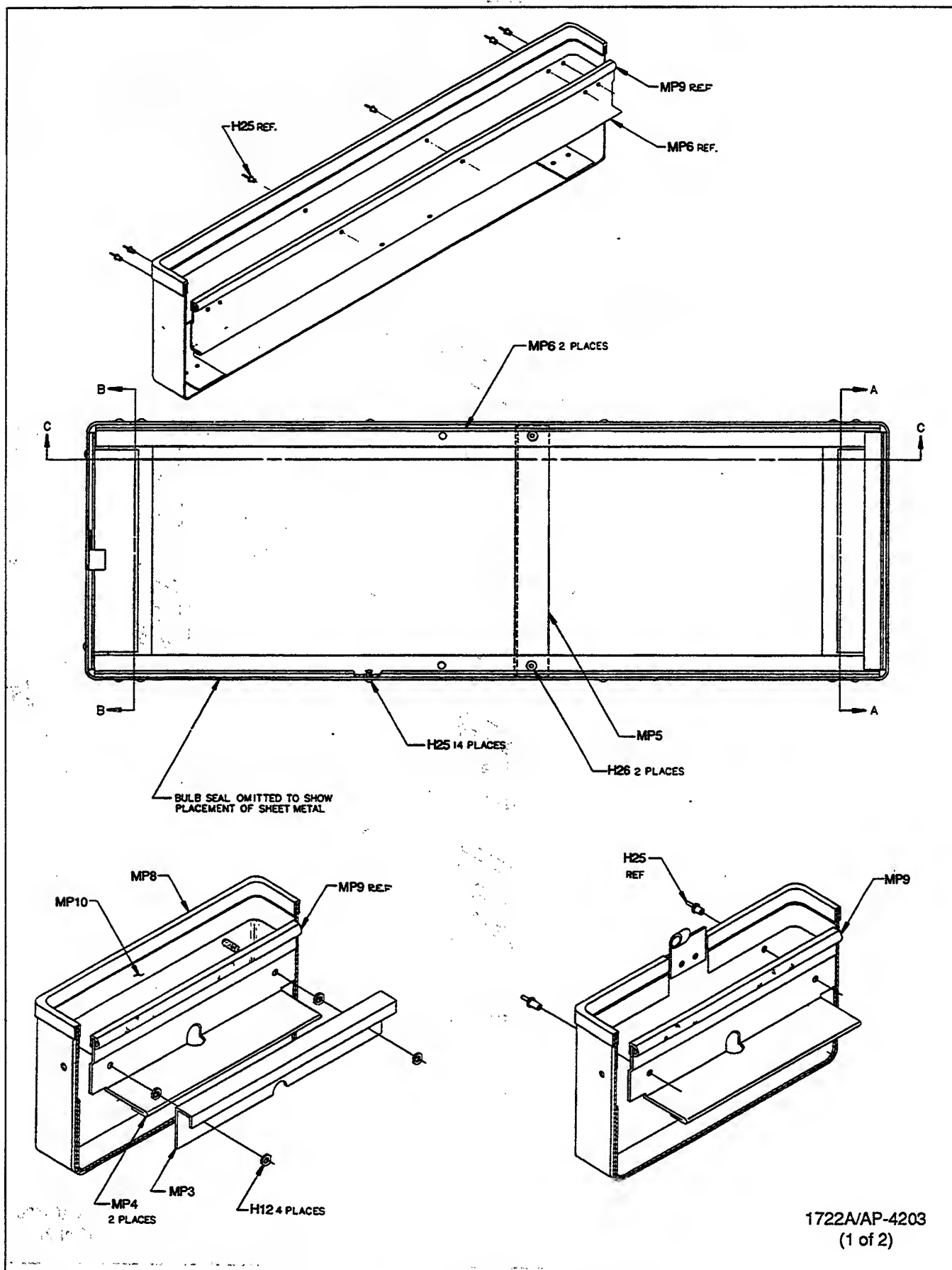


Table 11-6. A15 Instrument Covers (Front & Back) Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
H 1	SCREW, PH, P, SEMS, STL, 6-32, .500	177030		COMMERCIAL	4	
H 2	NUT, HEX, STL, 4-40	110635		COMMERCIAL	4	
MP 1	SUBASSEMBLY, COVER	717363	89536	717363	1	
MP 2	COVER, INNER SIDE	717306	89536	717306	1	
MP 3	INSTRUMENT SUPPORT	759183	89536	759183	2	
MP 4	INNER END PIECE	759191	89536	759191	4	
MP 5	DIVIDER	759217	89536	759217	2	
MP 6	INNER SIDE PIECE	759225	89536	759225	4	
MP 7	FOOT, SINGLE BAIL TYPE (DARK UMBER)	653923	89536	653923	4	
MP 8	RUBBER, CHANNEL, NEOPRENE	529362	83478	896	8	
MP 9	GASKET, BULB-SEAL, NEOPRENE, EXTRUSION	740381	56524	778	8	
MP 10	TAPE, FOAM, NEOPRENE, DBL COAT, 1/2W	592618	89536	592618	8	
NOTES:	† Static sensitive part.					



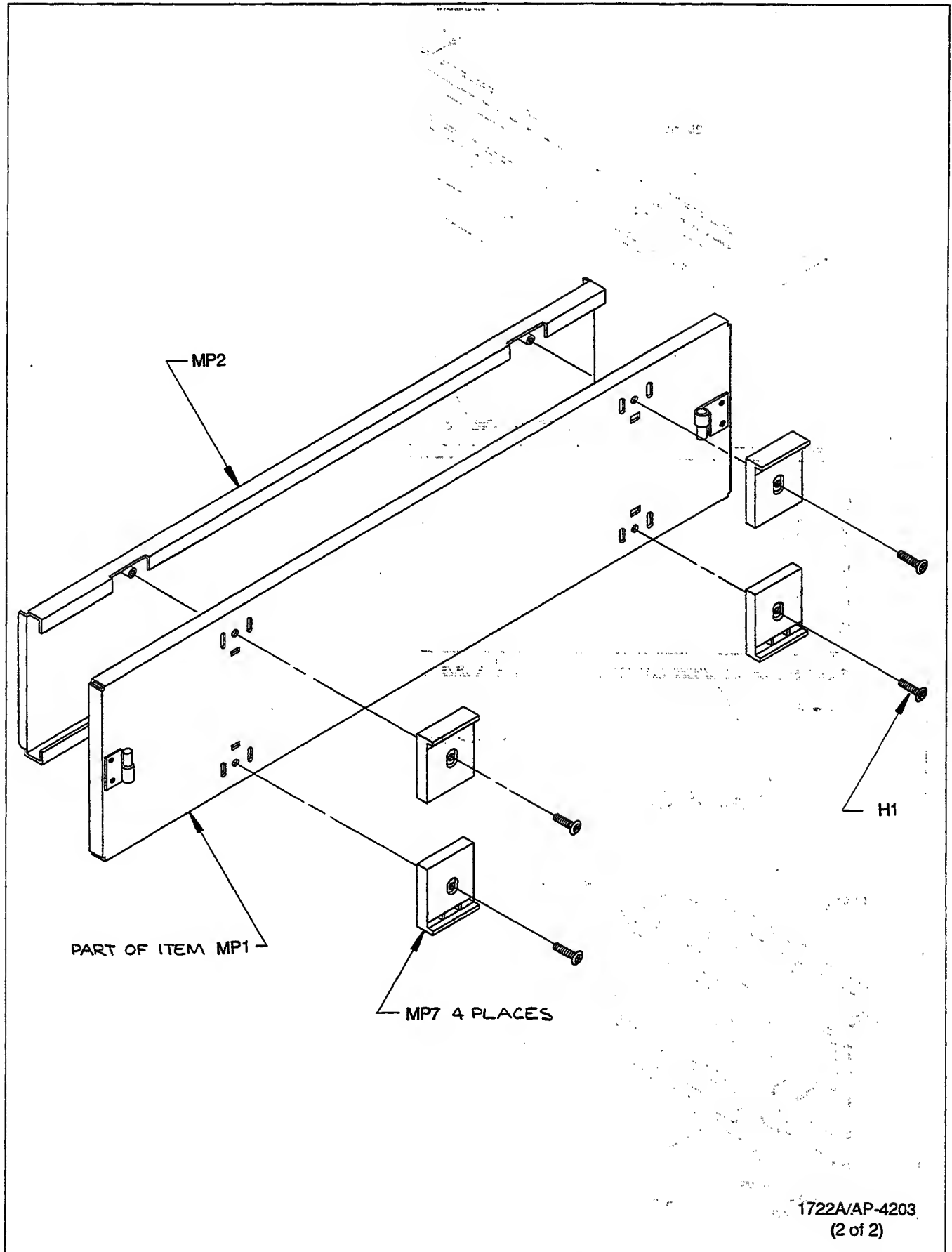
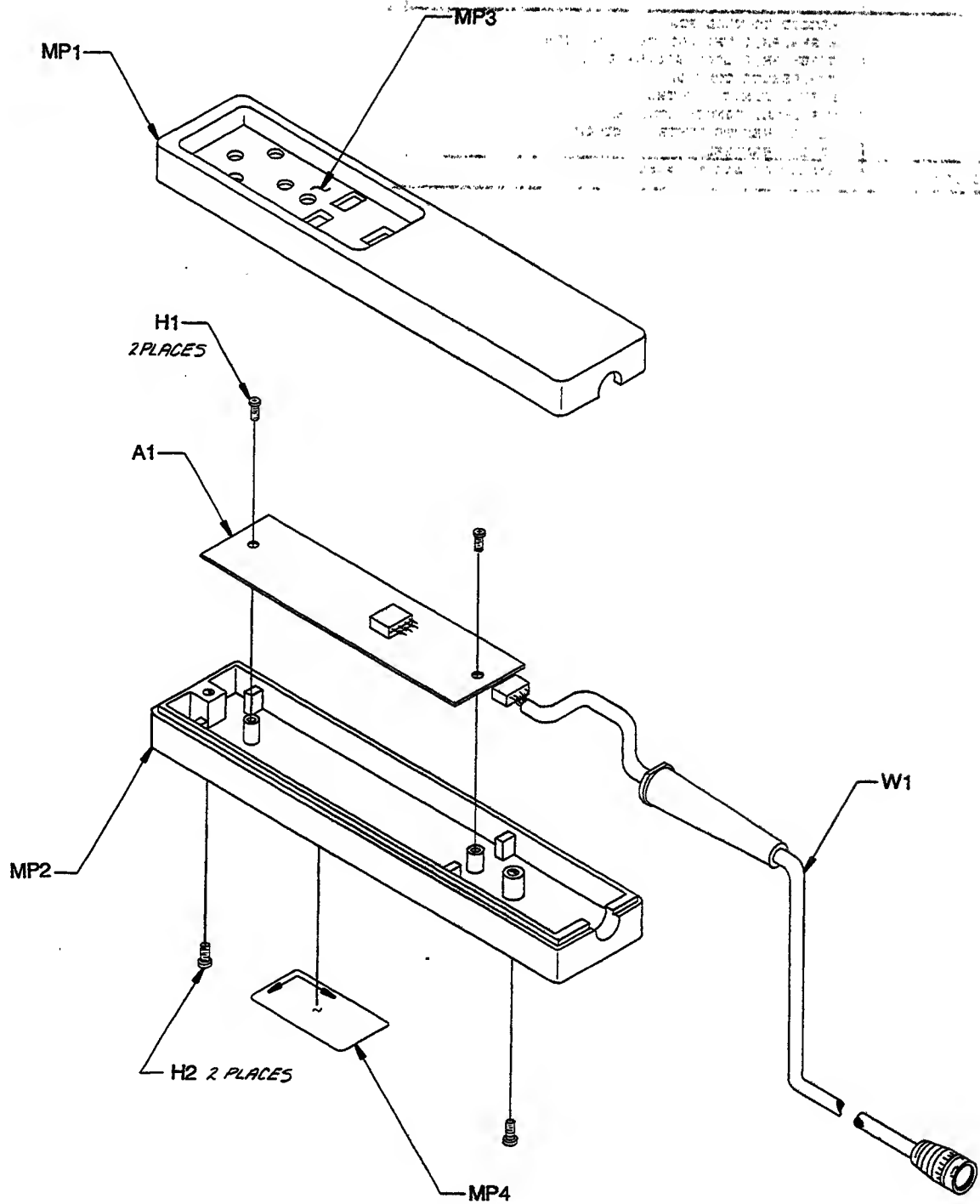


Figure 11-5. A15 Instrument Covers (Front & Back) Assembly (cont)

Table 11-7. A16 Handheld Assembly

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	NOTES
A 1	‡ REMOTE CONTROL PCA	732206	89536	732206	1	
H 1	SCREW, PH, P, THD CUT, SS, 4-24, .375	183574		COMMERCIAL	2	
H 2	SCREW, PH, P, LOCK, STL, 6-32, .625	152181	19451	152181	2	
MP 1	TOP, REMOTE CONTROL	657304	89536	657304	1	
MP 2	BOTTOM, REMOTE CONTROL	657312	89536	657312	1	
MP 3	TOP DECAL, REMOTE CONTROL	534891	22670	534891	1	
MP 4	DECAL, REMOTE CONTROL BOTTOM	737015	22670	737015	1	
W 1	CABLE, HANDHELD	744268	89536	744268	1	
NOTES:	‡ Static sensitive part.					



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Figure 11-6. A16 Handheld Assembly

Table 11-8. A16A1 Remote Control PCA

REFERENCE DESIGNATOR	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	N O T E S
C 1	CAP, AL, 47UF, +50-20%, 16V	436006	62643	SM16VB-47	1	
C 2	CAP, CER, 5.6PF, +-0.25PF, 100V, COH	512954	51406	RPE110C0H5R6C1	1	
C 3	CAP, CER, 22PF, +-2%, 100V, COG	512871	04222	SR151A220GAA	1	
C 4, 6, 7	CAP, CER, 0.22UF, +-20%, 50V, Z5U	519157	04222	SR205E224MAT	3	
C 5	CAP, TA, 2.2UF, +-10%, 15V	364216	56289	199C225X9015AA2	1	
CR 1, 2	LED, RED, PCB MOUNT, LUM INT=2.0MCD	534859	53184	XC-5059R-2	2	
CR 3	LED, GREEN, PCB MOUNT, LUM INT=1.0MCD	534842	28480	HLMP-3502	1	
CR 4, 5	LED, YELLOW, PCB MOUNT, LUM INT=6.0MCD	413849	14936	MV6353	2	
J 103	HEADER, 2 ROW, .100CTR, RT ANG, 8 PIN	424200	00779	87230-4	1	
MP 1	PUSHBUTTON, -RECT.- LIGHT PUTTY GREY	406819	89536	406819	3	
R 1	RES, CF, 10K, +-5%, 0.25W	348839	59124	CF1/4 102J	1	
SW 1- 3	SWITCH, PUSHBUTTON, SPNO MOMENTARY	507319	31918	MD DISC	3	
U 1	† IC, MICROCOMPUTER, KEYBOARD, (V1.1)	718171	89536	718171	1	
U 2	† IC, LSTTL, BCD-DEC DCDR/DRVR 15V OUT	419192	01295	SN74LS145N	1	
U 3	† IC, LSTTL, OCTAL D F/F, +EDG TRG, W/CLEAR	454892	01295	SN74LS273N	1	
X 1	CRYSTAL, 2.0000MHZ, +-0.003%, HC18U	733352	61429	FOX-20S	1	
Z 1	RES, CERM, SIP, 6 PIN, 5 RES, 330, +-2%	408302	91637	CSC06A-01-331G	1	
NOTES:	† Static sensitive part.					

